A Nonpiecewise Model for Long-Channel Junctionless Cylindrical Nanowire FETs

Juan P. Duarte, Sung-Jin Choi, Dong-Il Moon, and Yang-Kyu Choi

***Abstract*—A nonpiecewise drain current model is formulated for long-channel junctionless (JL) cylindrical nanowire (CN) FETs. It is obtained by using the Pao–Sah integral and a continuous charge model, which is derived by extending the parabolic potential approximation in all regions of the device operation. The proposed nonpiecewise model analytically describes the bulk and surface current mechanisms in JL CN FETs from the subthreshold region through the linear region to the saturation region without any fitting parameters. In addition, for each of these operation regions, the model reduces to simple expressions that explain the working principle of JL CN FETs. The model is compared with numerical simulations and shows good agreement.**

***Index Terms*—Bulk current, compact model, cylindrical nanowire (NW) FET, junctionless (JL) transistor, semiconductor device modeling, surface current.**

A JUNCTIONLESS (JL) transistor has been recently demonstrated [1] as an alternative device for alleviating process challenges such as large doping concentration gradients and low thermal budget. It is composed of source, drain, and channel regions of homogeneous doping polarity and uniform doping concentration; therefore, it demands more simple fabrication processes than conventional inversion mode (IM) FETs [1], which are composed of heterogeneous doping regions such as p-n junctions. The main conduction mechanism in JL FETs relies not on the surface but on the bulk current; moreover, it turns off by making the channel fully depleted [2]. Surface current is dominant for gate voltages (V_G) higher than the flatband voltage $(V_{\rm FB})$ [2]. Among all transistor architectures, cylindrical nanowire (CN) FETs show the highest robustness against short-channel effects [3]. Hence, JL CN FET is a strong candidate for nanoscale transistor scaling and 3-D stacked devices.

Compact models are crucial for understanding the device properties and performance dependence on device parameters. They are also needed for fast circuit simulation. Several compact models have been reported for JL FETs [2], [4]–[9]. Models based on the abrupt-depletion approximation have been proposed for pinchoff CN FETs [4]–[6]. Their piecewise approach [4]–[6], i.e., discontinuity among each operation domain, may cause convergence problems [10]. In addition, a piecewise model based on the linearization of the electric potential was developed in [7]. It is continuous among each operation domain; however, it uses a numerical integration, which is not practical for compact modeling [10]. A model that covers every operation region continuously and can also be explicitly expressed would overcome these difficulties. In this letter, a nonpiecewise drain current model is proposed for long-channel JL CN FETs. It is based on the Pao–Sah integral [11] with a charge model obtained from the extension of the parabolic potential approximation in all regions of the device operation [9]: fully depleted, semidepleted, and accumulated. For each operation region, the charge and the drain current models reduce to simple expressions. Moreover, they explain the behavior and parameter dependence of JL CN FETs. The proposed model also clarifies the differences with respect to conventional IM FETs [3]. Our model is verified by numerical simulations [12] that show good agreement. The proposed model requires iterative procedures; however, it can be explicitly expressed using a well-known method used to obtain explicit formulas for IM transistors [10].

In a doped CN FET, a direct solution of Poisson's equation is difficult to obtain because of its high-order nonlinearity [7]. In this context, a simple way to represent the potential in the channel is given by the parabolic potential approximation [13]

$$\varphi(r) = \frac{r^2}{R^2}(\varphi_s - \varphi_o) + \varphi_o. \tag{1}$$

Here, r is the spatial distance in the radial direction, R is the channel radius, and φ_s and φ_o are the surface and center potentials in the channel, respectively. Using Gauss' law and the boundary condition at the interface, it is possible to obtain

$$C_{\rm ox}(V_G - V_{\rm FB} - \varphi_s) = 2\pi R\varepsilon_{\rm si}\left.\frac{d\varphi}{dr}\right|_{r=R} = -4\pi\varepsilon_{\rm si}\Delta\varphi \tag{2}$$

which relates φ_s and φ_o with V_G. In (2), $\Delta\varphi$ is the potential difference $\varphi_o - \varphi_s$ between the center and surface of the channel, and $C_{\rm ox}$ is the oxide capacitance represented by $2\pi\varepsilon_{\rm ox}/\ln(1 + t_{\rm ox}/R)$, where $t_{\rm ox}$ is the gate dielectric thickness. The right part of (2) assumes a uniform charge distribution in the channel, i.e., $4\pi\varepsilon_{\rm si}\Delta\varphi \approx Q_t = (Q_m + qN_{\rm si}\pi R^2)$, where Q_t and Q_m are the total and mobile charge densities per unit length and $N_{\rm si}$ is the doping concentration of the channel. The threshold voltage $(V_{\rm TH})$ can be obtained from (2) by assuming a fully depleted channel and approximating φ_o to zero at $V_{\rm TH}$, i.e., $V_{\rm TH} = V_{\rm FB} - qN_{\rm si}\pi R^2/C_{\rm eff}$ [7], where $1/C_{\rm eff} = 1/4\pi\varepsilon_{\rm si} + 1/C_{\rm ox}$. An additional equation is needed to obtain φ_s and φ_o.

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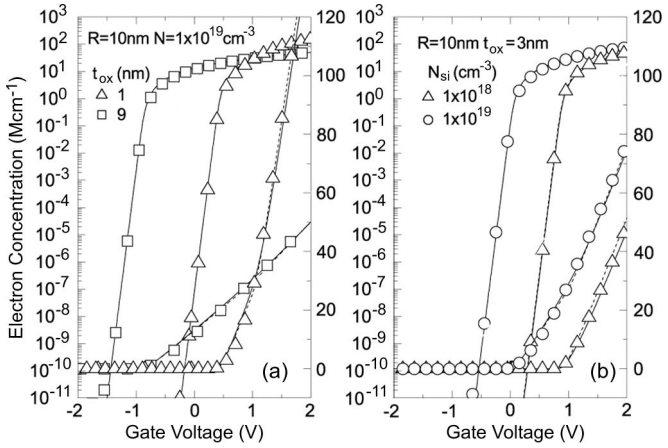

Fig. 1. Electron density per unit length as a function of V_G for (a) different $t_{\rm ox}$'s and (b) different $N_{\rm si}$'s, obtained from (symbols) simulations [12], (solid line) (4) of the proposed model, and (dotted line) (5) and (6) of the proposed model. p^+ polysilicon gate and $V_{\rm DS} = 0$ V are used for the simulations and model.

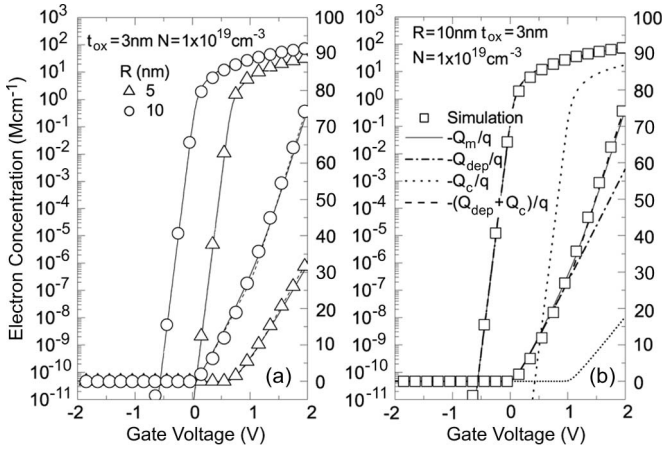

Fig. 2. (a) Electron density per unit length as a function of V_G for different R's obtained from (symbols) simulations [12], (solid line) (4) of the proposed model, and (dotted line) (5) and (6) of the proposed model. (b) $-Q_m/q$, $-Q_{\rm dep}/q$, $-Q_c/q$, and $-(Q_{\rm dep}+Q_c)/q$. p^+ polysilicon gate and $V_{\rm DS} = 0$ V are used for the simulations and model.

It can be obtained by integrating the charge density in the entire channel with the potential given by (1)

$$Q_t = qN_{\rm si}\pi R^2\left[1-\left(v_T e^{(\varphi_o - V)/v_T}/\Delta\varphi\right)\left(1-e^{-\Delta\varphi/v_T}\right)\right] \tag{3}$$

where V is the electron quasi-Fermi potential and v_T is the thermal voltage, kT/q. In order to obtain Q_m, (2) coupled with (3) should be solved. However, replacing φ_s [obtained from (3)] in (2) and exchanging $\Delta\varphi$ by $Q_t/4\pi\varepsilon_{\rm si}$ in (2) as well, a single equation can be obtained to represent Q_m

$$V_G - V_{\rm TH} - V = v_T\ln(-Q_m/4\pi\varepsilon_{\rm si}v_T) - Q_m/C_{\rm eff} + v_T\ln \times\left[(1+Q_m/qN_{\rm si}\pi R^2)/\left(1-e^{-(Q_m+qN_{\rm si}\pi R^2)/4\pi\varepsilon_{\rm si}v_T}\right)\right]. \tag{4}$$

Figs. 1 and 2 show the electron density per unit length $(-Q_m/q)$ as a function of V_G for different device parameters. The charge model expressed by (4) is in complete agreement with numerical simulations [12] for all regions of the device operation: fully depleted, semidepleted, and accumulated. In the right side of (4), the first term is dominant in the fully depleted region ($V_G < V_{\rm TH}$); thus, $Q_m \approx -4\pi\varepsilon_{\rm si}v_T\exp[(V_G - V_{\rm TH})/v_T]$. In the semidepleted region ($V_G > V_{\rm TH}$ and $V_G < V_{\rm FB}$), only the second term is dominant in the right side of (4), giving $Q_m \approx -C_{\rm eff}(V_G - V_{\rm TH})$. $C_{\rm eff}$ represents an effective gate capacitance in the semidepleted region. It controls the bulk charge [7]. In the flatband condition ($V_G = V_{\rm FB}$), the mobile charge is given by $-qN_{\rm si}\pi R^2$. In the accumulated region ($V_G > V_{\rm FB}$), the second and third terms in the right side of (4) are dominant. Moreover, for this region, the third term reduces to $(Q_m + qN_{\rm si}\pi R^2)/4\pi\varepsilon_{\rm si}$; therefore, $Q_m \approx -C_{\rm ox}(V_G - V_{\rm on})$ with $V_{\rm on} = V_{\rm FB} - qN_{\rm si}\pi R^2/C_{\rm ox}$.

An analytical drain current expression cannot be obtained by integrating the current continuity equation $I_{\rm DS}dz = -\mu Q_m dV = -\mu Q_m(dV/dQ_m)dQ_m$ from the source to the drain region due the last term in (4). In order to obtain an analytical drain current model, Q_m can be decoupled as $Q_m = Q_{\rm dep} + Q_c$, where $Q_{\rm dep}$ is the mobile charge in the fully depleted and semidepleted regions ($V_G < V_{\rm FB}$) and Q_c is a complementary mobile charge added to $Q_{\rm dep}$. $Q_{\rm dep}$ alone underestimates the total mobile charge for $V_G > V_{\rm FB}$ [see Fig. 2(b)]; therefore, Q_c acts as a correction term for $Q_{\rm dep}$. $Q_{\rm dep}$ and Q_c are independently obtained from the asymptotic behavior of (4)

$$V_G - V_{\rm TH} - V = v_T\ln(-Q_{\rm dep}/4\pi\varepsilon_{\rm si}v_T) - Q_{\rm dep}/C_{\rm eff} \tag{5}$$

$$V_G - V_{\rm FB} - V = v_T\ln(-Q_c/4\pi\varepsilon_{\rm si}v_T) - Q_c/C_c \tag{6}$$

where $C_c = C_{\rm ox} - C_{\rm eff}$. In the fully depleted region, $Q_{\rm dep}$ is larger than Q_c and is given by $Q_{\rm dep} \approx -4\pi\varepsilon_{\rm si}v_T\exp[(V_G - V_{\rm TH})/v_T]$. In the semidepleted region, $Q_{\rm dep}$ is also larger than Q_c and is represented by $Q_{\rm dep} \approx -C_{\rm eff}(V_G - V_{\rm TH})$. Finally, in the accumulated region, $Q_{\rm dep} + Q_c$ is given by $Q_{\rm dep} + Q_c \approx -C_{\rm eff}(V_G - V_{\rm TH}) - C_c(V_G - V_{\rm FB}) = -C_{\rm ox}(V_G - V_{\rm on})$. Therefore, $Q_{\rm dep} + Q_c$ is equivalent to Q_m in all regions of the device operation, as shown in Figs. 1 and 2. Equations (5) and (6) can be expressed in an explicit form using the method proposed in [10]. Following [10], the charge error obtained is lower than 0.1% with a second-order correction for the explicit forms of (5) and (6).

Using (5) and (6), the drain current can be expressed by $I_{\rm DS} = I_{\rm dep} + I_c$, where $I_{\rm dep}$ is the drain current in the fully depleted and semidepleted regions and I_c is a complementary current that, together with $I_{\rm dep}$, represents the drain current in the accumulated region. They are obtained using the Pao–Sah integral [11]

$$\begin{aligned} I_{\rm dep} + I_c &= -\frac{\mu}{L}\int_0^{V_{\rm DS}}(Q_{\rm dep}+Q_c)dV \\ &= -\frac{\mu}{L}\left(\frac{Q_{\rm dep}^2}{2C_{\rm eff}} - v_T Q_{\rm dep}\right)\Bigg|_{Q_{S_{\rm dep}}}^{Q_{D_{\rm dep}}} \\ &\quad -\frac{\mu}{L}\left(\frac{Q_c^2}{2C_c} - v_T Q_c\right)\Bigg|_{Q_{S_c}}^{Q_{D_c}} \end{aligned} \tag{7}$$

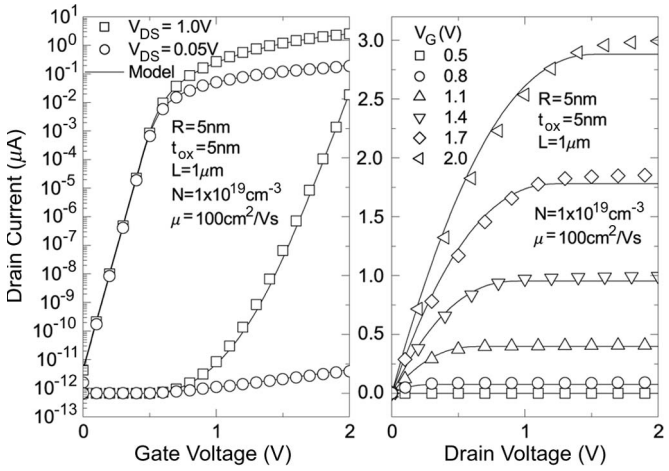

Fig. 3. Drain current as a function of (a) V_G and (b) $V_{\rm DS}$ obtained from (symbols) simulations [12] and (continuous line) (7) of the proposed model. p^+ polysilicon gate is used for the simulations and model.

where μ is the effective mobility and L is the gate length of the device. Q_D and Q_S are obtained from (5) and (6) by replacing V with $V_{\rm DS}$ for Q_D and V with zero for Q_S. Fig. 3 shows the drain current as a function of V_G and $V_{\rm DS}$. The proposed model shows good agreement with numerical simulations for all bias conditions. It continuously represents the drain current from the subthreshold region through the linear region to the saturation region.

In the subthreshold region, the proposed model reduces to $I_{\rm DS} \approx 4\pi\varepsilon_{\rm si} v_T^2(\mu/L)\exp[(V_G - V_{\rm TH})/v_T][1 - \exp(-V_{\rm DS}/v_T)]$. It is the same as in [5, eq. (7)]. Note that it is not proportional to R as in IM FETs [3] because, in JL FETs, there is no volume inversion for the subthreshold region. For a gate voltage lower than $V_{\rm FB}$, the bulk current mechanism governs the total drain current, and two types of behavior can be found. First, in the linear region $(V_G - V_{\rm TH} > V_{\rm DS})$, the model reduces to $I_{\rm DS} \approx (\mu C_{\rm eff}/L)(V_G - V_{\rm TH} - V_{\rm DS}/2)V_{\rm DS}$. Second, in the saturation region $(V_G - V_{\rm TH} < V_{\rm DS})$, it reduces to $I_{\rm DS} \approx (\mu C_{\rm eff}/2L)(V_G - V_{\rm TH})^2$. $V_G - V_{\rm TH}$ is the drain voltage needed to pinch off the channel in the drain region, and it determines the saturation condition in JL FETs [2], [5]. For a small $V_{\rm DS}$ and in the flatband condition, the drain current is approximately given by $I_{\rm DS} \approx \mu q N_{\rm si}\pi R^2 V_{\rm DS}/L$. This is the current expression for a resistor $(I = V/R)$, which is independent of $t_{\rm ox}$ [1]. This is different from the case of IM FETs, where the current depends on $t_{\rm ox}$ for any bias conditions [3]. In the saturation region and in the flatband condition, the drain current is given by $I_{\rm DS} \approx \mu(qN_{\rm si}\pi R^2)^2/(2C_{\rm eff}L)$, which depends on $t_{\rm ox}$. Its dependence at this bias is opposite to that of conventional IM FETs [3]. For a gate voltage higher than $V_{\rm FB}$, the bulk and surface current mechanisms govern the total drain current, and three types of behavior can be found. First, for $V_G - V_{\rm TH} > V_{\rm DS}$ and $V_G - V_{\rm FB} > V_{\rm DS}$, the drain current is given by $I_{\rm DS} \approx (\mu C_{\rm ox}/L)(V_G - V_{\rm on} - V_{\rm DS}/2)V_{\rm DS}$. Note that, at this bias, the charge is accumulated on the surface of the channel from the source to the drain region. Second, for $V_G - V_{\rm TH} > V_{\rm DS}$ and $V_G - V_{\rm FB} < V_{\rm DS}$, the drain current is given by $I_{\rm DS} \approx (\mu C_{\rm ox}/L)(V_G - V_{\rm on} - V_{\rm DS}/2)V_{\rm DS} + (\mu C_c/2L)(V_G - V_{\rm FB})^2$. At this bias, a semidepletion condition occurs near the drain side, and accumulation occurs in the source side. Third, for $V_G - V_{\rm TH} < V_{\rm DS}$ and $V_G - V_{\rm FB} < V_{\rm DS}$, the drain current is given by $I_{\rm DS} \approx (\mu C_{\rm eff}/2L)(V_G - V_{\rm TH})^2 + (\mu C_c/2L)(V_G - V_{\rm FB})^2$. Here, the channel at the drain side experiences a pinchoff condition, and it is accumulated at the source region. These six types of behavior are also found in accumulation mode FETs [14].

In conclusion, a nonpiecewise drain current model for long-channel JL CN FETs has been proposed. It continuously represents both the bulk and surface currents without any fitting parameters for all regions of the device operation, including the subthreshold, linear, and saturation regions. In addition, the model was reduced to simple expressions that explain the working principle of JL CN FETs for each operation region. JL CN FETs showed different behaviors from those of conventional IM FETs. The presented model is well suited to be a core model for JL CN FETs, which can be expressed in an explicit form and be further improved by adding more physical effects such as short-channel effects, mobility field dependence, quantum effects, parasitic resistance effects, thermal noise, etc.

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