# First Demonstration of a Wrap-Gated CNT-FET with Vertically-Suspended Channels

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***Abstract*—**Fully wrap-gated carbon nanotube (CNT) transistors with vertically suspended (VS) semiconducting single-walled CNTs, purified up to 99.9%, are demonstrated for the first time. Without a sacrifice of scalability, remarkably enhanced gate controllability and charge transport capabilities were achieved due to the geometrical advantage of the gate-all-around (GAA) structure with multiple channels. The VS channels were formed with the aid of a silicon-processed vertically integrated nanowire frame, offering high completeness and compatibility with silicon processes. This approach will increase the applicability of CNTs toward high-performance emerging materials.

## I. Introduction

Until recently, Moore's law has guided the development of MOSFETs. However, the down-scaling of the conventional MOSFETs now confronts fundamental limits. An alternative channel material or a novel device structure should be exploited to move beyond Moore's law. Under this circumstance, FETs based on single-walled carbon nanotubes (CNT) have shown attractive properties compared to a conventional silicon-based FET in terms of improved performance and energy efficiency in digital logic circuits [1] [2]. However, CNT-based FETs are associated with several problems. First, semiconducting CNTs should be highly purified to achieve a high on/off current ratio ($I_{ON}/I_{OFF}$). Second, minimization of the small inter-CNT spacing is necessary to attain a high $I_{ON}$ value. Finally, high gate controllability should be guaranteed for a low sub-threshold slope (SS). Regarding these requirements of highly purified semiconducting CNTs with increased packing density levels, earlier studies reported purity levels exceeding 99% and densities higher than 200 CNTs/μm (inter-CNT spacing $\leq$ 5 nm) [3-5]. From a structural standpoint, a three-dimensional gate-all-around (GAA) nanowire FET exhibits more desirable electrical characteristics compared to a conventional in-plane two-dimensional MOSFET. Hence, a GAA CNT-FET composed of a single CNT channel has been reported [6]. Nevertheless, the requirements of a high packing density levels for a proper $I_{ON}$ value and high purification to ensure a low $I_{OFF}$ value remain challenging. Moreover, wafer-scale compatibility with standard CMOS fabrication is another concern. Here, for the first time, a vertically suspended and wrap-gated CNT-FET (termed "VS-wrap-gated CNT-FETs" in this paper) is fabricated by CMOS-compatible processes. This VS-wrap-gated CNT-FET that consists of multiple suspended CNTs with high purity (99.9%) levels greater by one order of magnitude shows a high $I_{ON}$, a low $I_{OFF}$, a steep SS, and low hysteresis ($\Delta V_{HYS}$). Multiple vertically suspended CNT channels without agglomeration provide a remarkable increase in the CNT density per unit area as well as high gate controllability of the CNT channels. In addition to the CMOS standard processes, critical-point drying (CPD) and high-vacuum annealing (HVA) processes were utilized to prevent the stiction failure of the VS-CNT channels and to enable low hysteresis, respectively.

## II. Device Fabrication

The entire fabrication process of the VS-wrap-gated CNT-FETs is illustrated in Fig. 1. A bulk -Si wafer was used as the substrate. Prior to the formation of the CNT channels, five-story multi-stacked Si-nanowires (Si-NWs) were patterned without stiction problems via a previously reported one-route all-dry-etching process, as shown in Fig. 2 [7]. The five-story Si-NWs serve as a mechanical frame which firmly holds the vertically suspended CNTs. Afterwards, the Si-NWs were fully oxidized by a thermal oxidation process (100 nm of $SiO_2$). The fully oxidized Si-NWs were then functionalized with an amine-terminated group to support the CNTs, even at all sides of the NWs. Subsequently, the device was immersed in a highly purified, pre-separated 99.9% semiconducting enriched CNT solution (provided by NanoIntegris, Inc.) and dried at 60 °C for 7 hrs. To form the source and drain (S/D) electrodes, a photolithography process based on a negative photoresist (PR) was applied. Stacks composed of Ti (1 nm)/Pd (50 nm)/Au (50 nm) were sequentially deposited by thermal evaporation, followed by a lift-off process. An additional etching step using $O_2$ plasma was utilized selectively to remove the CNTs, which existed on the background bottom surface, so as to block a possible leakage path through the debris of the CNTs. The aforementioned fully oxidized Si-NW frame was partially etched away by HF (Fig. 3) and then completely eliminated by HF (Fig. 4), after which only the CNTs were left as the VS structure. To avoid stiction, which results in the bundling and collapse of the CNTs by surface tension, a critical-point drying (CPD) process was applied. Next, an $Al_2O_3$ gate dielectric (30 nm) was uniformly deposited by ALD, with the gate metal of Ni (20 nm) then deposited by ALD to realize a fully wrap-gated structure. Afterwards, Al (1 μm) was sputtered for an interconnection

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and probing pads. Finally, gate patterning was conducted via a positive PR-based photolithography process and a subsequent wet etching step using an Al etchant. The finalized cross-sectional structure as well as the individual components were verified by TEM analyses and energy-dispersive X-ray spectroscopy (EDS) mapping, respectively (Fig. 5). It was observed that the suspended CNTs collapsed and then became bundled (bottom of Fig. 6) when CPD was not utilized. With the CPD process, however, they were well separated without stiction (top of Fig. 6). Henceforth, the former was used as a control group (termed the bundled CNT-FET) and the latter was used as the experimental group (termed the V-suspended CNT-FET). The V-suspended CNT-FET showed a higher device yield than the bundled CNT-FET. There were approximately 20 CNTs in one vertical plane in the VS-wrap-gated CNT-FET, whereas fewer than 10 CNTs were noted in the bundled case due to the collapsed CNTs during the etching of the fully oxidized Si-NWs.

## III. Experimental Results and Discussion

Fig. 7 shows ultraviolet-visible near-infrared (UV-vis-NIR) spectroscopy absorption spectra of the 90% (blue trace) and the 99.9% semiconducting nanotube solution (red trace). Notably, the higher $S_{22}$ and $S_{33}$ peaks (semiconducting transition) as well as the lower $M_{11}$ peak (metallic transition) confirm the high-level purity of the 99.9% semiconducting CNT solution. The transfer characteristics ($I_D$–$V_G$) of three differently shaped CNT-FETs, a 2-D planar CNT-FET, the bundled CNT-FET, and the V-suspended CNT-FET, are compared in Fig. 8. The 3-D GAA CNT-FETs (bundled and V-suspended) exhibit a steeper SS and a lower $I_{OFF}$ value compared to those of the 2-D planar CNT due to the inherently high gate controllability, as expected. To ensure a practically useful prediction, $I_{ON}$ was normalized by $W_{footprint}$. Fig. 9 shows a comparison of $I_{ON}$ at an identical gate overdrive voltage considering the difference in the threshold voltage ($V_G$-$V_T$). The V-suspended CNT-FET shows five-fold increase in $I_{ON}$ due to the decreased inter-tube Coulomb interactions and increased number of CNT channels compared to the bundled CNT-FET (Fig. 9). The output characteristics ($I_D$–$V_D$) are also compared between the V-suspended CNT-FET and the bundled case, as shown in Fig. 10. The $I_{ON}$ value normalized in terms of the 2-D footprint width ($W_{footprint}$ in Fig. 6), i.e., $I_{measured}/W_{footprint}$, is 15.4 μA/μm. Compared with the SS of the bundled CNT-FET, the SS of V-suspended CNT-FET was reduced by 35%, i.e., 78 mV/dec. (Fig.11). Such an improvement in the SS is attributed to the better gate controllability of the GAA structure, which is an ideal geometry for electrostatics because it provides strong coupling of the gate bias to the CNT channels, and the screening effects arising from the bundled CNT-FET. Moreover, the hysteresis ($\Delta V_{HYS}$) was found to be approximately 30 mV in our V-suspended CNT-FET (Fig. 11 and Fig. 12). This value is much lower than those of other exploratory channel materials with $SiO_2$ or high-*k* gate dielectric materials and is even comparable to that extracted from an advanced MOSFET that consists of high-*k* gate dielectric and a Si channel. This notably small $\Delta V_{HYS}$ is attributed to the high-vacuum annealing (HVA) treatment, which reduces the number of interface traps [8]. For a more comprehensive understanding of the root cause of the improved electrical characteristics in the V-suspended CNT-FET compared to those in the bundled case, the electric field (*E*-field) distribution was simulated using a 3-D numerical simulator (COMSOL) (Fig. 13). All device dimensions used in the simulations were extracted from actual TEM images, as shown in Fig. 5. The detailed dimensions and parameters for the simulations are summarized in Fig. 14. In the simulation, a common gate voltage ($V_G$) of 2.5 V was applied to the gate electrode, and the peak *E*-field at the suspended CNTs was extracted. The *E*-field of the V-suspended CNT-FET is increased by a factor of 1.55 compared to that of the bundled CNT-FET. This is caused by the adjacent mutual interference of the neighboring CNTs, which increases the electrostatic coupling from the bundled CNTs. Table 1 summarizes the advantages of the proposed VS-wrap-gated CNT-FET compared to other types of CNT-FETs [3]-[6]. The VS-wrap-gated CNT-FET represents a simpler approach, which helps to realize a more tightly controlled GAA. In this work, it can be concluded that the improved SS and the significantly decreased area of the CNT-FETs increase the energy efficiency of circuit-level devices.

## IV. Conclusion

In summary, V-suspended and fully wrap-gated CNT-FETs were demonstrated. In order to improve the driving current, vertically suspended channels which occupy a small fraction of the footprint area due to the inherent vertical structure, were utilized. To suppress short-channel effects, a gate-all-around structure was used, which is possible because the CNTs were physically floated and suspended from the bottom substrate. To decrease the off-state leakage current, highly purified single-walled semiconducting CNTs with a purity level of 99.9% were used. VS-CNT channels were realized using multi-stacked Si-NWs, which served as a sacrificial layer to hold the CNTs with the aid of an overall wafer-scale CMOS compatible process. This led to a high driving current of 15.4 μA/μm normalized by the footprint channel width and a steep subthreshold slope of 78 mV/dec. In addition, critical-point drying (CPD) and a high-vacuum annealing (HVA) process provided stiction-free suspended CNTs and low hysteresis. This work demonstrates the feasibility of utilizing emerging low-dimensional materials as promising candidates for post-silicon transistors.


## Acknowledgments

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## References


[1] L. Wei, et al., *IEDM*, 917-920 (2009).
[2] L. Chang, et al., "IEDM Short Course," *IEDM* (2012).
[3] M. M. Shulaker, et al., *IEDM*, 839-842 (2015).
[4] M. M. Shulaker, et al., *IEDM*, 812-815 (2014).
[5] Q. Cao, et al., *Nat. Nanotech*., 180-186 (2013).
[6] A. D. Franklin, et al., *IEDM*, 84-87 (2012).
[7] B. H. Lee, et al., *Nano Letters*, 8056-8061 (2015).
[8] X. Hua, et al., *Small*, 2833-2840 (2012).

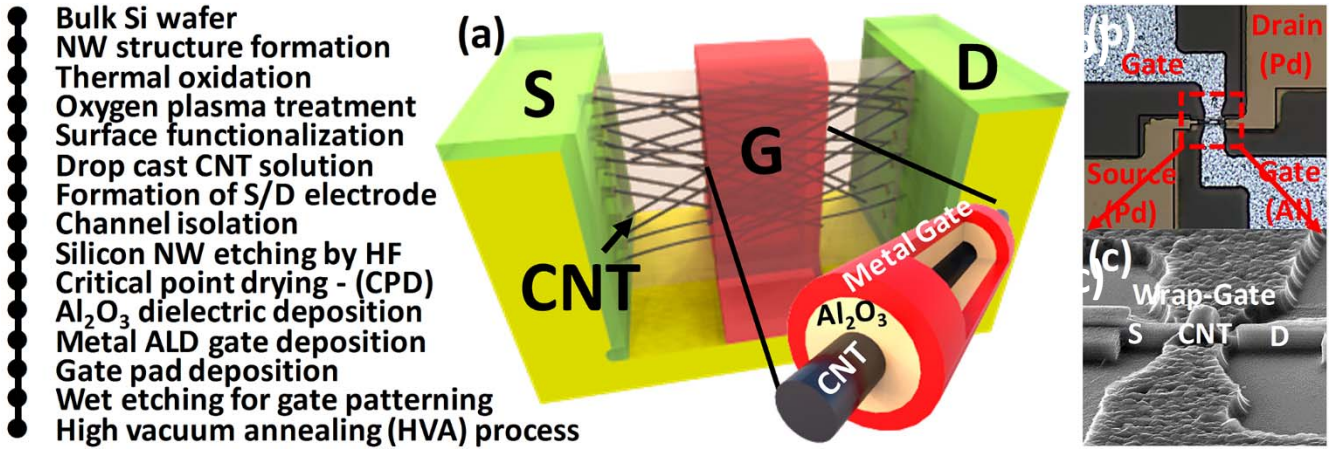



**Fig. 1.** Details of the VS-wrap-gated CNT-FETs, including the formation of a fabricated device: (a) Schematic illustration of the VS-wrap-gated CNT-FETs on a bulk silicon substrate. The entire process is fully compatible with the silicon-based CMOS process. The wrap-gated structure consists of $Al_2O_3$ dielectric layers and an ALD metal gate (Ni) surrounding the CNT channels. (b) Optical image of the fully fabricated devices. (c) A 25° tilted SEM image of a fully fabricated device is shown.

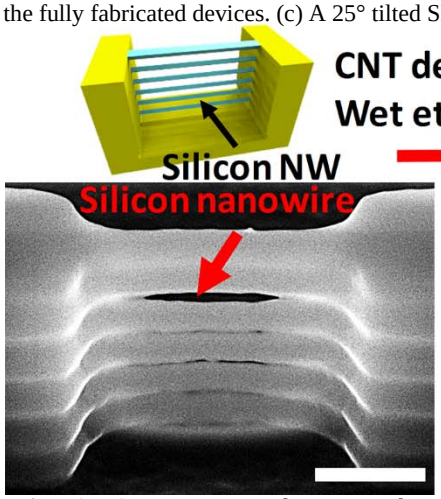



**Fig. 2.** Starting materials using the vertically stacked silicon nanowire frame. Fully oxidized ($SiO_2$) layer thickness of 100 nm. Scale bar: 500 nm

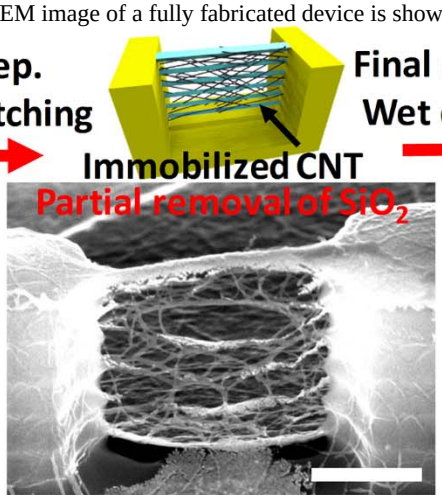



**Fig. 3.** Oxidized Si-NWs were etched away using a HF wet etching process. Middle stage of suspended CNTs by the partial removal of $SiO_2$.

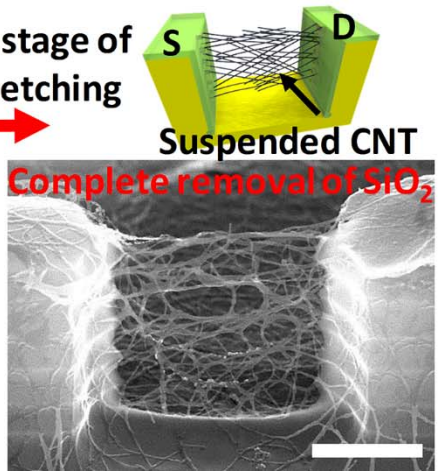



**Fig. 4.** Final stage of vertically suspended CNTs with the complete removal of $SiO_2$. Additionally, the CPD process reinforced the vertically suspended channels.

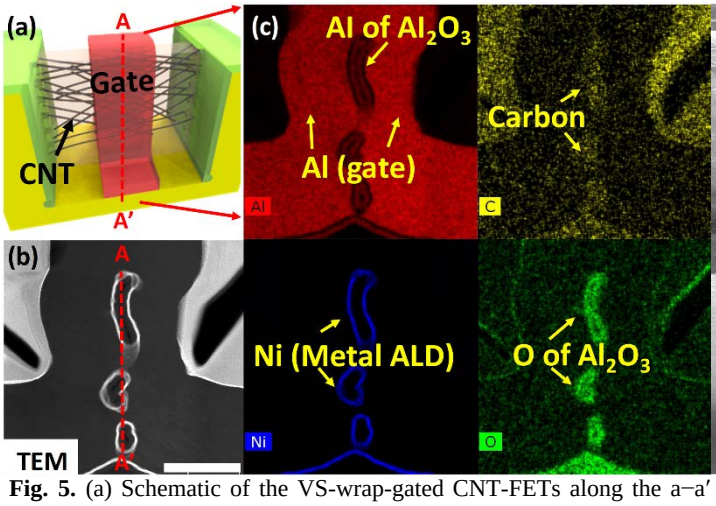



**Fig. 5.** (a) Schematic of the VS-wrap-gated CNT-FETs along the a–a′ direction. (b) Cross-sectional TEM images showing the well-defined dielectric and metal gate ($Al_2O_3$/Ni/Al) wrapping the CNT channels. Scale bar: 500 nm (c) EDS mapping analysis of the VS-wrap-gated CNT-FETs captured to analyze the "O" component of $Al_2O_3$, the "Al" of $Al_2O_3$, "Ni" and the "C" of carbon.

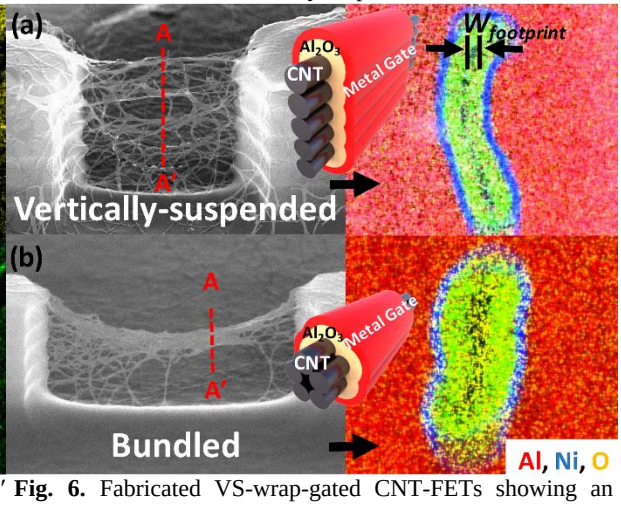



**Fig. 6.** Fabricated VS-wrap-gated CNT-FETs showing an ideal GAA structure geometry. (a) Cross-sectional TEM images showing the dielectric and metal gate (ALD-Ni), (Al) wrapping the CNT channel width of less than 5 nm. (b) A bundle-type CNT-FET is also shown as a control group (without the CPD process).

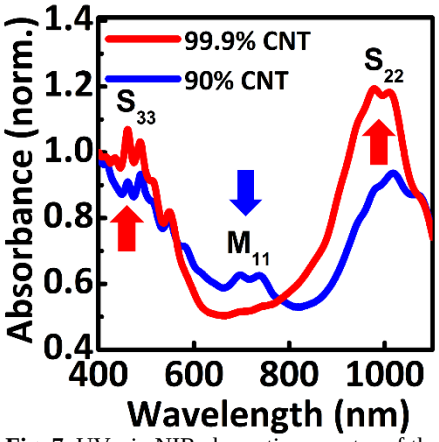



**Fig. 7.** UV-vis-NIR absorption spectra of the 90% semiconducting separated nanotubes (blue trace) and 99.9% semiconducting separated nanotubes (red trace).

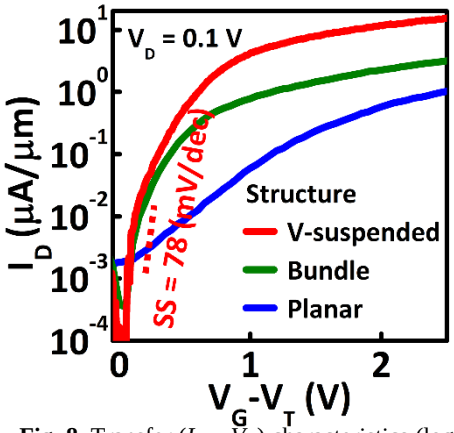



**Fig. 8.** Transfer ($I_D - V_G$) characteristics (log scale) of CNT-FETs with different geometric values, $L_{CH}$ = 1 μm and $W_{CH}$ = 5 nm at a drain voltage ($V_D$) of 0.1 V. $I_{ON}$ normalized by considering $W_{CH}$ as $I_{ON}/W_{CH}$.

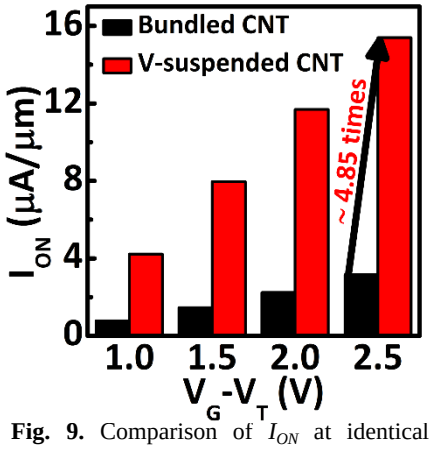



**Fig. 9.** Comparison of $I_{ON}$ at identical operation voltages but with a different threshold voltage for each device. The VS-wrap-gated CNT-FET shows that the current drivability is increased by nearly five-fold.

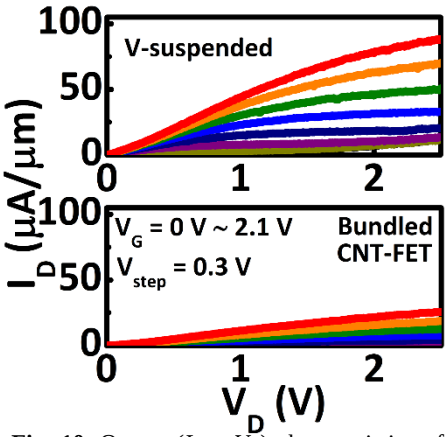



**Fig. 10.** Output ($I_D - V_D$) characteristics of the CNT-FETs for different gate voltages ranging from 0 V to 2.1 V in 0.3 V steps. That of the VS-wrap-gated CNT-FET is increased by a factor of nearly 5.

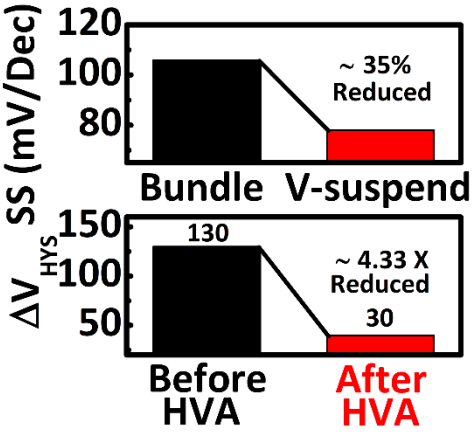



**Fig. 11.** Comparison of the SS levels for different structure geometries, and the hysteretic results of HVA treatments in CNT-FETs as measured under each condition.

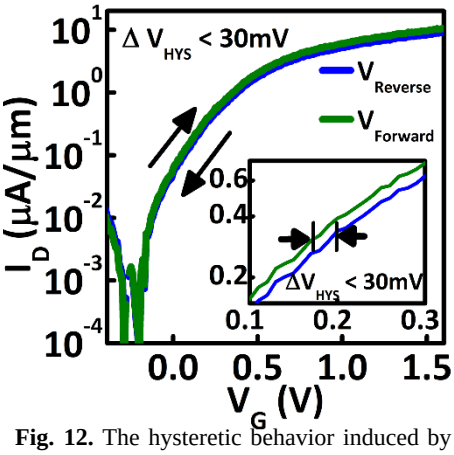
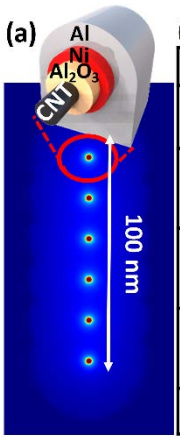



**Fig. 12.** The hysteretic behavior induced by gate bias sweeping showed a minimal value (inset = Δ $V_{HYS}$ < 30 mV), and exceptional stability was achieved. The HVA treatments enable a reduction of the number of interface traps.




(b)

| PARAMETER | VALUE |
|---|---|
| Gate | Ni (20 nm) |
| Structure (nm) | X = 50, Y = 100 |
| Channel Diameter | CNT (2 nm) |
| Dielectric Constant | $Al_2O_3$ Permittivity 7 |
| $V_G$ (V) | 2.5 V |

**Fig. 13.** (a) Cross-sectional geometry and 3-D module profile of simulated potential maps using a 3-D numerical simulator (COMSOL) (b) Simulation of the device parameters.

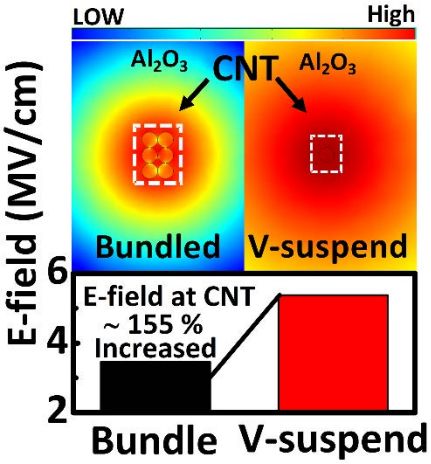



**Fig. 14.** Plot of the calculated electric field at single CNTs as a function of the geometric dependency. In the comparison of the E-field distribution, the VS-wrap-gated CNT-FET is increased by a factor of nearly 1.55.

| Ref. | IEDM 15 [3] | IEDM 14 [4] | Nat. Nano. [5] | IEDM 12 [6] | This work |
|---|---|---|---|---|---|
| SWNT purity | 99.99% | n/a | 98% | Single-CNT | 99.9% |
| S.S | n/a | n/a | 150 | 105 | 78 |
| $I_{ON}/I_{OFF}$ | $10^3$ | $5 \times 10^3$ | 600 | $10^4$ | $10^5$ |
| $W_{CH}$ / Density | 1 μm / 200 CNTs | 1 μm / 100 CNTs | 1 μm / 500 CNTs | 2 nm / Single-CNT | 5 nm / 20 CNTs |
| $V_D$ (V) | n/a | 1.0 | 0.8 | 0.5 | 0.1 |
| Feature | M-Removal | Repeat Transfer | Langmuir Schaefer | Single-GAA | Vertical-GAA |

**Table. 1.** Summary of the demonstrated advantages of the VS-wrap-gated CNT-FETs compared to those in previous reports.