Transformable Functional Nanoscale Building Blocks with Wafer-Scale Silicon Nanowires

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ABSTRACT: Through the fusion of electrostatics and mechanical dynamics, we demonstrate a transformable silicon nanowire (SiNW) field effect transistor (FET) through a wafer-scale top-down approach. By felicitously taking advantage of the proposed electrostatic SiNW-FET with mechanically movable SiNWs, all essential logic gates, including address decoders, can be monolithically integrated into a single device. The unification of various functional devices, such as pn-diodes, FETs, logic gates, and address decoders, can therefore eliminate the complex fabrication issues associated with nanoscale integration. These results represent a step toward the creation of multifunctional and flexible nanoelectronics.

KEYWORDS: Silicon nanowire, field effect transistor, logic gates, address decoders, nanoelectromechanical systems

The rapid miniaturization of electronic devices has been a key force in driving scientific and economic progress over the past 40 years in microelectronics. Nanoscale-electronics (nanoelectronics) is now a closely watched upcoming frontier. One-dimensional structures such as nanowires and carbon nanotubes, created through bottom-up approaches, are the ideal building blocks for nanoelectronics given their ability to function as both devices and wires. Previous methods regarding the formation of functional nanoscale building blocks, particularly those involving semiconductor nanowires, have focused mainly on bottom-up approaches that allow control of the carrier type (electrons in n-type; holes in p-type), the carrier concentration, and the wire diameter (near-atomic-scale precision) during the growth phase or during chemical synthesis. With bottom-up approaches, semiconductor nanowires have been used as building blocks in the assembly of various types of nanodevices, including field effect transistors (FETs), bipolar junction transistors (BJTs), and logic gates. Moreover, functional nanoscale electronic devices in the form of crossed nanowire pn-diodes and FETs have enabled bottom-up approaches to be used in the assembly of nanoelectronic circuits that can ultimately be integrated with memory arrays for read/write operations or can be used to manufacture stand-alone processors. However, currently, manufacturing methods relying on bottom-up approaches do not provide controllability that is precise enough to integrate high-density ordered arrays. Moreover, a specific transfer technique is typically required in the assembly of devices on a separate substrate, although bottom-up synthesized semiconductor nanowire devices have excellent electronics transport properties. Moreover, a reproducible means of creating high-quality electrical contacts remains a challenge. As noted in previous reports regarding semiconductor nanowire logic gates, they are often composed of significantly different structures based on crossed nanowires, such as pn-diodes and FETs; hence, the realization of cointegrated nanoelectronic circuits is difficult and the throughput of such devices raises serious questions regarding their configuration and architecture.

One important advantage of using top-down approaches is in the ability to control the position of functional device arrays precisely. Silicon technologies in top-down approaches are advantageous for other types of semiconductor technology due to the considerable research pertaining to the use of silicon and the many silicon-related materials and mature nanofabrication technologies available. As a solution to the questions posed above, we now report the “transformable” functional nanoscale devices created by the fusion of electrostatically operating silicon nanowires (SiNWs) building blocks and mechanically movable SiNWs using a wafer-scale top-down approach. This fused device has several noteworthy aspects. The properties are changeable and reconfigurable on the same SiNW-FET (i) by moving or bending the SiNWs and (ii) by modifying the threshold voltage. In other words, functional operations (i.e., logic gates: NOT; OR; AND; NOR; NAND gates and address decoders) with substantial gains can be implemented on the same single SiNW-FET through mechanical modifications. Hence, our approach introduces the nanoelectronics to wafer-scale mass production.
and thereby represents a step closer to the creation of multifunctional and flexible nanoelectronics.

The proposed transformable functional nanoscale device is very similar to a double-gate FinFET except for the separated gate consisting of the primary gate (gate1, G1) and the secondary gate (gate2, G2). They sit vertically on the sidewall of the SiNW and face each other through a chemical-mechanical polishing (CMP) process (Figure 1A and Supporting Information Figure S1). Conductance modulated by the tied gate voltage (i.e., \( V_G = V_{G1} = V_{G2} \)) (Figure 1B) shows the complementary switching behavior involving an n-channel FET (n-FET) and a p-channel FET (p-FET). Substantial gate controllability is demonstrated as the two gates give a strong response to the SiNW channel. Field-emission scanning electron microscopy (FESEM) was used to image the proposed device (Figure 1B, inset). As symmetric/asymmetric biases can be applied to the two separated gates, SiNW conductance is also controlled independently (Figure 1C).

The ability to control the SiNW conductance independently enables the SiNW-FET itself to be used as a logic gate. To demonstrate the flexibility of the proposed SiNW-FET elements, we investigated a single p-FET as a logic gate. A two-input NAND logic gate can be realized using a single SiNW p-FET with two separated gates (i.e., G1 and G2) as inputs and a highly p⁺-doped drain region as the output (Figure 2A). The highly p⁺-doped source region is biased at 5 V (\( V_{DD} \)), and the output node is connected to an off-chip bias resistor (300 MΩ). As a result, the pull-up and -down networks are comprised of the single SiNW p-FET and the resistor. In this device, the output depends on the resistance ratio between the conductance of the SiNW and the constant exterior resistor. A logic 1 state is observed when either one or both inputs are low. In this case, the p-FET is on and the channel resistances are much lower than that of the constant resistor. As a result, most of the voltage drops across the constant resistor. A logic 0 state can only be achieved when the p-FET is off, that is, when both inputs are high. The output-input (\( V_{OUT}-V_{IN} \)) relationship (Figure 2B, inset) shows a constant high \( V_{OUT} \) when the other input is set low. Analysis of the data demonstrates that these two-input NAND gates routinely exhibit gains larger than five, which can be increased with a thinner gate dielectric layer. Moreover, this type of single

Figure 1. Transformable functional SiNW-FETs from the top-down approaches. (A) Schematic illustrating the proposed SiNW-FET. The SiNW is in contact with two electrodes, the S and D, to measure the SiNW conductance. Two separated gates (G1, G2) sit vertically on the SiNW and face each other. (B) Conductance versus tied gate voltage (\( V_G = V_{G1} = V_{G2} \)) of the transformable SiNW p-FET and n-FET devices. The back-gate (silicon substrate) is grounded during all measurements. (Inset) An SEM image of a SiNW-FET. Scale bar, 300 nm. (C) Conductance versus the independent gate voltage (\( V_{G1} \) and \( V_{G2} \)) of a transformable SiNW p-FET and n-FET devices with a SiNW width of 50 nm.

Figure 2. (A) Symbol of the electronic circuit for electrical measurement of the NAND logic gate with a single SiNW p-FET. (B) The output voltage of the NAND logic gate with a single SiNW p-FET versus four possible logic address level inputs: (0, 0), (0, 1), (1, 0), and (1, 1), where the logic 0 input is 0 V and the logic 1 input is 5 V (identical to that shown in Figure 2). (Inset) The \( V_{OUT}-V_{IN} \) relationship. The solid (dashed) line shows the \( V_{OUT}-V_{IN} \) relationship when the other input is logic 1 (0).
SiNW-FET logic circuit can reduce the chip area, leakage current, and active power dissipation by reducing the number of transistors. We also note that the combination of a single n-FET and the constant resistor produces a NOR gate with a high gain. 19

Basically, the conducting path along the source-channel-drain in the FET structure cannot be turned on owing to the embedded back-to-back connected diodes, 20 i.e. n⁺(source)–p(channel)–n⁺(drain) for the n-FET and p⁺(source)–n(channel)–p⁺(drain) for the p-FET. Two back-to-back connected diodes are only used for the formation of the potential barriers in the initial state of the FETs. 21 Our transformable SiNW-FET was created based on the goal of independently utilizing embedded diodes in a single SiNW-FET. The SiNW formulated in this study was initially formed as a core/shell Si/SiO₂ structure in which the oxide shell serves to control the thickness of the gate dielectric, later to be subsequently removed through wet-etching of the SiO₂. Thus, the solid-state gate dielectric is replaced by an air-state nanogap (Supporting Information Figure S2). Negative voltage is then applied to one of the two gates (G1 or G2) for a p-FET SiNW-FET. The induced electrostatic force therefore attracts the SiNW. If the electrostatic force is larger than the elastic restoring force of the SiNW, the SiNW can mechanically adhere to the negatively biased gate (Figure 3A). High-resolution transmission electron microscopy (HRTEM) images do not show evidence of voids and asperities in the contacted interface (Figure 3B). At an air-gap thickness of approximately 20 nm, the voltage of the adhesion of the SiNW is relatively high (near 19 V) (Figure 3C). At the moment of adhesion, high forwarded diode current flows between the gate and the source/drain (S/D). Once the SiNW comes into contact with the gate, the state can be sustained due to the adhesion force that arises at the contact interface (i.e., Van Der Waals forces). 22 Because the gate materials consist of in situ n⁺-doped polycrystalline silicon (poly-Si) in this study, the contact between the SiNW channel (n-type for a p-FET) and the gate is easily produced. Hence, a pn-diode is created between the n-SiNW channel when it is in contact with the n⁺-doped poly-Si and p⁺-source or -drain. Current-voltage measurements show that the p⁺-source/n-SiNW or p⁺-drain/n-SiNW diode exhibits current rectification characteristics with a typical turn-on voltage of approximately 1 V (Figure 3D). The transformed nanoscale pn-diodes with reproducible and predictable electrical properties enable exploration of the assembly and properties of integrated pn-junction arrays in logic gates. Therefore, a two-input OR gate
is easily realized using two diodes embedded in a transformed single SiNW-FET with two highly p⁺-doped S/D as inputs and the gate (n⁺ poly-Si) as the output. In this device, the output is low (logic 0) when both input voltages are low (0 V), and the output is high (logic 1) when either or both of the input voltages is/are high (Figure 3E). It is noteworthy that a high input corresponds to the forward bias of the selected pn-junction.

The output–input (V_{OUT}–V_{INPUT}) voltage response (Figure 3E, inset) shows that V_{OUT} increases linearly with V_{INPUT} when one input is set low (0 V), except for the region near 0 V. The V_{OUT}–V_{INPUT} data also show a nearly constant high output when the second input is set high (5 V). It is important to note that AND gates can be implemented using an n-FET with a p⁺ poly-Si gate. However, these OR and AND logic gates cannot exhibit a voltage gain; they will show a gain if implemented by connecting the SiNW FET inverter to the output node (Supporting Information Figure S3).

The development of strategies of addressing the arrays of nanoscale devices is also important in the implementation of integrated nanosystems such as biological sensor arrays and nanocomputers. Our transformable SiNW-FET can function as an address decoder by modification of the gate dielectric, in which mechanically changing (or modifying) the thickness of the gate dielectric can serve to define an address code that enables the input lines (gates) to turn on and off specific output lines with the inherent gain of the SiNW-FET. We investigated these types of decoder functions based on a single-gate n-FET (i.e., using G1 or G2). After the etching SiO₂ (i.e., the gate dielectric), reoxidation was performed to form a thin gate dielectric (3 nm) on the SiNW and poly-Si surface. Positive gate voltage was then applied, allowing the SiNW to adhere mechanically to the biased gate electrode (Figure 4A, top). HRTEM images show the uniformly distributed gate dielectric layer after adhesion (showing no evidence of voids and asperities) (Figure 4A, bottom). Typical electrical transport data (Figure 4B) recorded on a single SiNW-FET before and after modification demonstrates the substantial effect that the modification has on the gate response. This suggests that this type of modification can be used to differentiate specific SiNW FET elements in an array to produce an address decoder circuit. The actuation voltage to modify the SiNW-FETs can be reduced as the SiNW becomes narrower and longer due to its low spring force (Figure 4C). Before modification (i.e., an
air-state nanogap as a gate dielectric), the SiNW-FET exhibited a threshold voltage that exceeded 9 V. After modification, however, this threshold shifted to approximately 2 V. Measurements made on more than 70 individual SiNW-FETs show that this large threshold voltage shift is reproducible. Specifically, a histogram (Figure 4D) summarizing the threshold voltages before and after modification of the SiNW-FET with the same geometrical parameters yielded average values of 9.2 and 2.3 V, respectively. In addition, the threshold voltage shift was found to be stable for at least a few months even in atmosphere (Supporting Information Figure S4). We also found that modified SiNW-FETs could be turned on and off at least hundreds of times without significant hysteresis behavior even at air-environment. Therefore, it is possible to turn on specific cross points that are modified in selected SiNW-FETs (1-hot code) by electrical modification of the permittivity and thickness of the gate dielectric. The response on a single SiNW-FET with and without modification of the gate dielectric assures this behavior (Figure 4E).

In summary, through mechanical modifications, the proposed predictable and reproducible SiNW-FETs demonstrated various transformable functions, such as critical logic gates and address decoders. This paves the way toward the creation of multifaceted and flexible nanoelectronics with the aid of wafer-scale top-down approaches that offer precise control of the carrier type, concentration, and position. Moreover, the unification of versatile functional devices, such as pn-diodes, FETs, and their gate logic gates, can eliminate the complex fabrication issues involved in monolithic nanoscale integration. We also note that the transformable SiNW-FET can function as a memory device involved SiNW-FETs (1-hot code) by electrical modification of the permittivity and thickness of the gate dielectric. The response on a single SiNW-FET with and without modification of the gate dielectric assures this behavior (Figure 4E).

ASSOCIATED CONTENT

Supporting Information. Detailed fabrication process of SiNW-FETs, an experimental section describing modification of gate dielectric layers for transformable operations, further applications of transformable logic gates, and measured sustainability of the modified SiNW-FETs. This material is available free of charge via the Internet at http://pubs.acs.org.

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REFERENCES

(19) By implementing an n-FET (i.e., highly n−doped source/drain (S/D) and p-SiNW as a channel) as a pull-down network on the proposed SiNW-FET, a NOR logic gate can be readily formed, similar to a NAND logic gate.
(21) The pn-diodes are generally used for the formation of potential barriers between the S/D and channel in a FET. However, this structure can be changed through the use of a structure without S/D junctions.
(23) This low response region is due to the finite turn-on voltage of the p-n junctions and produces a logitic output that is typically 0.4 to 2 V less than the input voltage. A small reduction in $V_{\text{OUT}}$ does not affect the operation of our logic gates because the low turn-on voltage contributions are reproducible and can be readily accounted for in defining the 0 and 1 states.
(24) An AND logic gate can also be implemented on the transformable SiNW-FET using an n-FET (i.e., highly doped n$^+$-S/D and p-SiNW) with p$^+$ polysi gates. Therefore, previous pull-up networks in complementary metal oxide semiconductor (CMOS) electronics can be transformed to OR logic gates (Figure 2), and pull-down networks can be transformed to AND logic gates. Also see Supporting Information, Figure S2.
(27) Cui, Y.; Wei, Q.; Park, H.; Lieber, C. M. Science 2001, 293, 1289–1292.
(28) The large threshold voltage difference is wholly due to the significantly changed thickness and material of the gate dielectric.
equivalent thickness of the gate dielectric before modification (i.e., 3 nm SiO$_2$ on the SiNW surface and 3 nm SiO$_2$ on the poly-Si gate with a 24 nm air-gap) is 62 nm when considering the permittivity of SiO$_2$ and air. However, after modification, the equivalent thickness of the gate dielectric is close to 6 nm. This difference in the thickness and permittivity of the gate dielectric layer can affect the gate capacitance value and in turn, significantly change the threshold voltage.