Modeling and Characterization of the Abnormal Hump in n-Channel Amorphous-InGaZnO Thin-Film Transistors After High Positive Bias Stress

Jungmin Lee, Sungju Choi, Seong Kwang Kim, Sung-Jin Choi, Dae Hwan Kim, Jisun Park, and Dong Myong Kim

***Abstract*— Hump characteristics of n-channel amorphous indium–gallium–zinc-oxide (a-InGaZnO) thin-film transistors (TFTs) after positive gate and drain bias stress (PGDBS) are investigated. With the increase of the PGDBS time, we observed not only a shift of the threshold voltage (V_T) but also a generation of the hump in the transfer characteristics. The hump is caused by the localized trapping of electrons in the gate insulator over the gate–source overlap region by the high vertical field during the PGDBS ($V_{GS} = 30$, $V_{DS} = 30$; $V_{GD} = V_{GS} - V_{DS} = 0$ V). The TFT with a hump after PGDBS is modeled as a series connection of main and parasitic TFTs. The parasitic TFT for the electron trapping at the gate–source overlap region has a higher threshold voltage (V_{Tp}) and a shorter effective channel length ($L_{chp} \cong L_{ov}$) compared with those (V_{Tm} and L_{ch}) of the main TFT.**

***Index Terms*— Positive bias stress, hump effect, a-IGZO TFTs, overlap region, charge trapping, modeling, parasitic TFT.**

I. Introduction

AMORPHOUS oxide semiconductors (AOS) are under active research and development as switching and driving thin film transistors (TFTs) in active matrix organic light-emitting diode (AMOLED) displays. Especially, the amorphous Indium- Gallium-Zinc Oxide (a-IGZO) TFT has been considered to be a promising device with high carrier mobility, good uniformity, and a low temperature fabrication process for high resolution AMOLED displays [1]–[3]. However, the instability in a-IGZO TFTs with bias, temperature, and illumination during long term operation still remains a critical issue [4], [5]. When a high gate and drain bias are applied in the driving TFTs, the electrical degradation by the high current causes deterioration of the pixel signal. One of the degradation phenomena is a hump effect observed in both sub- ($V_{GS} < V_T$) and above-threshold ($V_{GS} > V_T$) regions in the transfer curves (the drain current; I_D as a function of the gate bias; V_{GS} with the threshold voltage; V_T) caused by the high bias stress. Although there were reports on the hump effect under the subthreshold operation as an edge effect or back-channel conduction, [6]–[9] a hump effect in the above threshold has not yet been fully studied.

In this work, the hump effect after the positive gate and drain bias stress (PGDBS) in the above threshold region ($V_{GS} > V_T$) of n-channel a-IGZO TFTs is investigated. After positive gate and drain bias stress at $V_{GS} = 30$ V and $V_{DS} = 30$ V ($V_{GD} = V_{GS} - V_{DS} = 0$ V), the hump effect is observed both in the current-voltage (I-V) and capacitance-voltage (C-V) characteristics. Various channel lengths combined with technology computer-aided design (TCAD) simulation are employed to verify and quantify the proposed physical mechanism for the hump after the PGDBS in a-IGZO TFTs.

II. Device Structure and Fabrication

N-channel inverted staggered a-IGZO TFTs with an etch stopper were fabricated on a glass substrate. After deposition of the gate electrode (Mo) by RF sputtering, a bilayer ($SiN_x/SiO_x = 400$ nm/50 nm) gate insulator was deposited by the plasma enhanced chemical vapor deposition (PECVD). Then, a 50 nm thick a-IGZO (In:Ga:Zn = 1:1:1) thin-film was deposited by DC sputtering in a gas mixture of Ar/O_2 =35/48 at room temperature (RT). The source/drain (Mo) layer and the etch stopper ($SiO_2 = 50$ nm) was formed by DC sputtering and PECVD on the a-IGZO thin film, respectively. Finally, a passivating bilayer ($SiN_x/SiO_x = 100$ nm/100 nm) was formed by PECVD and a-IGZO thin-film was annealed at T=523 K for 1 hour. We characterized a-IGZO TFTs with the channel width $W = 200$ μm, the channel length $L = 100$ μm, and the gate-source/drain (G-S/G-D) overlap length $L_{ov} = 15$ μm. High PGDBS at $V_{GS} = 30$ V and $V_{DS} = 30$ V ($V_{GD} = V_{GS}$-$V_{DS} = 0$ V) was applied for the stress time $t_{st} = 1{,}000 \sim 10{,}000$ s at RT. Agilent 4156C semiconductor parameter analyzer and HP-4284A LCR meter were employed for I-V and C-V characterization under dark. V_T is extracted by the linear extrapolation method focusing on the hump effect observed in the above threshold bias ($V_{GS} > V_T$).

III. Results and Discussion

Fig. 1 shows the transfer characteristics of the forward and reverse modes (working the source terminal as the drain and the drain terminal as the source of the channel carriers in the operation) as a function of the stress time at $V_{GS} = 30$ V and $V_{DS} = 30$ V. With increasing t_{st}, we observe a positive shift of V_T and a slight increase of the subthreshold

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The authors are with the School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea (e-mail: dmkim@kookmin.ac.kr).

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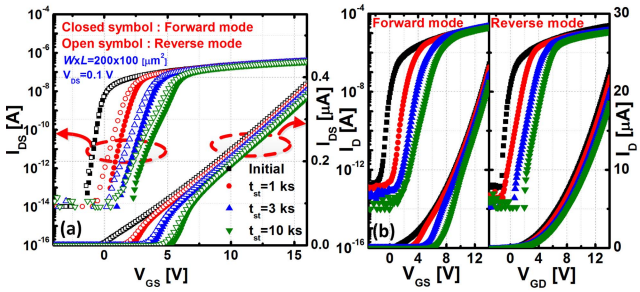

Fig. 1. Transfer characteristics of a-IGZO TFT(W/L = 200 μm/100 μm) after PGDBS at V_{GS} = V_{DS} = 30 V (V_{GD} = 0 V) (a) V_{DS} = 0.1 V, (b) V_{DS} = 20.1 V.

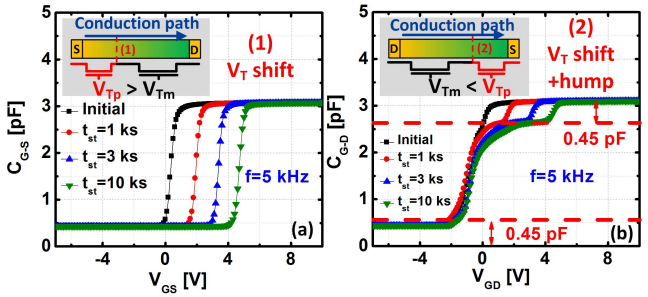

Fig. 2. C-V characteristics of the a-IGZO TFT with W/L = 200 μm/100 μm after PGDBS at V_{GS} = V_{DS} = 30 V (V_{GD} = 0 V). (a) C_{GS}-V_{GS}, (b) C_{GD}-V_{GD}. Inset shows the equivalent circuit for the difference in the hump characteristics under forward and reverse mode operations.

slope (SS) in the transfer curves [10] with a considerable hump in the above threshold bias. For the hump after the PGDBS, the a-IGZO TFT can be modeled as a series connection of the main TFT directly controlled by the gate electrode and the parasitic TFT at the gate-source (G-S) overlap region as shown in the inset of Fig. 2. The parasitic TFT is employed to model the localized trapping of electrons due to the higher vertical field during the PGDBS in the gate-insulator compared to that of the main channel region.

Compared with the threshold voltage (V_{Tm}) and the effective channel length ($L_{\mathrm{ch,m}}$) of the main TFT, the parasitic TFT for the G-S overlap region has a higher threshold voltage ($V_{\mathrm{Tp}} > V_{\mathrm{Tm}}$) with a short effective channel length as

$$V_{\mathrm{Tp}} = V_{Tm} - Q_{\mathrm{trap}}/C_{\mathrm{ox}} > V_{\mathrm{Tm}};$$

$$Q_{\mathrm{trap}} \equiv -q \int n_{trap}(x)dx \quad (1)$$

$$L_{\mathrm{ch,p}} \,(\cong L_{\mathrm{ov}}) < L_{\mathrm{ch,m}} \,(\cong L + L_{\mathrm{ov}}) \quad (2)$$

with $C_{\mathrm{ox}}(= \varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}})$ the oxide capacitance per unit area and Q_{trap} as the trapped charges in the gate insulator and at the SiO_2/a-IGZO interface. Because the current through the series-connected TFTs is limited by the transistor allowing a lower current, the current at low V_{GS} ($V_{\mathrm{TP}} < V_{\mathrm{GS}} < V_{\mathrm{Tmp}}$) is dominated by the parasitic TFT while it is dominated by the main TFT at high V_{GS}($V_{\mathrm{GS}} > V_{\mathrm{Tmp}}$) with V_{Tmp} defined as the humping gate voltage at $I_{\mathrm{Dp}} = I_{\mathrm{Dm}}$.

In the transfer curves at V_{DS} = 0.1 V as shown in Fig. 1(a), a considerable positive shift of the I_{D}-V_{GS} curves is observed in the forward mode compared to the reverse mode with increasing t_{st}. This comes from the reduced effective gate bias ($V_{\mathrm{GS,eff}} = V_{\mathrm{GS}}$-$V_{\mathrm{Tp}}$) induced by the locally trapped electrons ($\Delta V_{\mathrm{Tp}} = -Q_{\mathrm{trap}}/C_{\mathrm{ox}}$, $Q_{\mathrm{trap}} < 0$) at the SiO_2/a-IGZO interface. In the transfer curves under high drain bias at V_{DS} = 20.1 V, the hump in the reverse mode disappears as shown in Fig. 1(b). At V_{DS} = 20.1 V, the extended pinch-off of the overlap region in the reverse mode, contrary to the forward mode, screens off the localized barrier formed by Q_{trap} at the G-S overlap region. This decouples the effect of the parasitic TFT and only the main TFT works.

Fig. 2 shows capacitance-voltage (C_{GS}-V_{GS} and C_{GD}-V_{GD}) characteristics after PGDBS. While the C_{GS}-V_{GS} curve in Fig 2(a) shows only a positive shift without a hump, the C_{GD}-V_{GD} curve shows hump characteristics near the turn-on voltage in the transition region of the gate bias. The difference between the gate-to-source (C_{GS}) and the gate-to-drain (C_{GD}) configurations provides an evidence for the localized trapping of electrons at the gate-source overlap region. In the case of C_{GD}-V_{GD}, the C-V characteristic at low V_{GD} follows a typical property of the main TFT with a relatively low V_{T}. With the increase of V_{GD}, the channel conduction path is extended to the boundary between the main and parasitic TFTs. This causes an abrupt change of the capacitance and shows a hump in the C_{GD}-V_{GD} curve. Consequently, an additional gate bias is needed to form a conductive channel and this causes a hump characteristic as shown in Fig. 2(b).

For the C_{GD}-V_{GD} curves in Fig. 2(b), we note that the difference ($\Delta C \equiv C_{\mathrm{max}}$-$C_{\mathrm{hump}}$) between the maximum capacitance (C_{max}) and the capacitance (C_{hump}) at the humping gate bias (as the capacitance for the parasitic TFT) is very close to the minimum capacitance (C_{min}) as the overlap capacitance (C_{ov}) described by

$$\Delta C \left(\equiv C_{\mathrm{max}} - C_{\mathrm{hump}}\right) \cong C_{\mathrm{min}} \,(\cong C_{\mathrm{ov}})\,;\, (C_{\mathrm{ov}} = W L_{\mathrm{ov}} C_{\mathrm{ox}})\,. \quad (3)$$

This suggests that the parasitic TFT is closely related to the G-S overlap region. In our previous work [11], moreover, we confirmed that the electric field at the G-S overlap is much stronger than that in the channel region with a floated back surface in a-IGZO TFTs. It also shows a strong correlation between the localized trapping of charge at the G-S overlap region and the hump characteristic.

Using the multi-frequency C-V method [12], we extracted the subgap density-of-states (DOS: $g_{\mathrm{A}}(E)$) in the a-IGZO active layer after PGDBS. The extracted subgap DOS near the conduction band minimum (E_{C}) is shown in Fig. 3(a). With increasing with t_{st}, the acceptor-like deep trap concentration (E_{C}–E > 0.1 eV) far from E_{C} clearly increases while the acceptor- like trap concentration (E_{C}-E < 0.1 eV) close to E_{C} rarely varies. These subgap traps determine the DC electrical characteristics (V_{T}, the degradation of SS), the noise performance, the controllability of the channel (transconductance) by the gate bias, the leakage current, and long-term stability of TFTs. Fig. 3(b) shows the threshold voltage shift of the main (ΔV_{Tm}) and parasitic (ΔV_{Tp}) TFTs with t_{st}. The threshold voltage shift is as large as $\Delta V_{\mathrm{Tm,max}}$ = 3.3 and $\Delta V_{\mathrm{Tp,max}}$ = 5.6 V, respectively. This means that the shift of V_{T} and the hump effect cannot be explained only by the increased deep traps because deep traps shift as small as ~1 V and requires an additional shift mechanism [13].

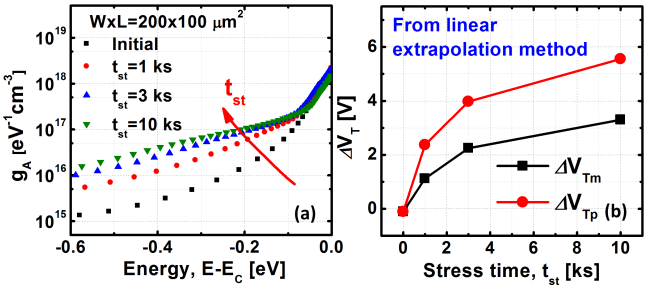

Fig. 3. (a) Subgap DOS extracted by the multi-frequency C-V method. (b) Threshold voltage change ($\Delta V_{\mathrm{T}}(t)$) of the main and parasitic TFTs with the PGDBS stress time (t_{st}) at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 30$ V.

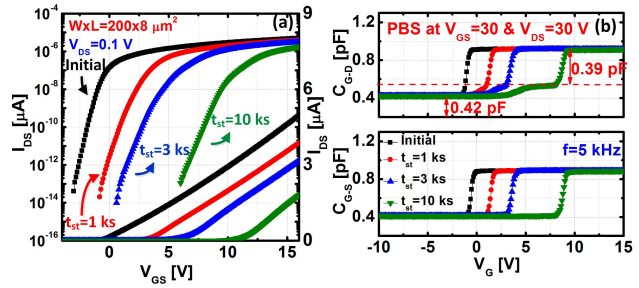

Fig. 4. (a) Transfer characteristics, (b) C-V characteristics (C_{GD}-V_{GD} and C_{GS}-V_{GS}) after PGDBS at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 30$ V.

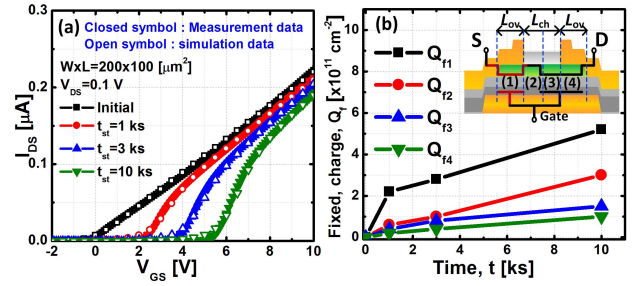

Fig. 5. (a) Experimental transfer characteristics in a-IGZO TFT ($W/L = 200\ \mu$m/100 μm) after PGDBS compared with TCAD simulation for fixed charge injection (Q_{f}) inside the gate-insulator at 4 specific regions (G-S overlap, channel 1, channel 2, G-D overlap region). (b) t_{st}-dependent fixed charge in the simulation. Inset for the location of injected charges of $Q_{\mathrm{f1}} \sim Q_{\mathrm{f4}}$.

Therefore, we investigated the channel length dependence of the PGDBS effect in a-IGZO TFTs with $W = 200\ \mu$m and fixed overlap length ($L_{\mathrm{ov}} = 15\ \mu$m) for $L = 8\ \mu$m and 100 μm. Fig. 4 shows the transfer and C-V characteristics of the short channel TFT with $L = 8\ \mu$m. While the C-V curve is similar to that of the long channel TFT with $L = 100\ \mu$m, the transfer characteristics show a positive shift but a negligible hump dissimilar to the long channel TFT. The current through the parasitic and main TFTs is dominated by the parasitic TFT over the entire gate bias range with only a positive shift because the parasitic TFT has a higher threshold voltage ($V_{\mathrm{Tp}} > V_{\mathrm{Tm}}$) but a similar effective channel length ($L_{\mathrm{ch,p}} \cong L_{\mathrm{ov}} = 15\ \mu$m, $L_{\mathrm{ch,m}} \cong L + L_{\mathrm{ov}} = 23\ \mu$m).

Finally, TCAD simulation was employed to quantitatively verify the proposed mechanism for the abnormal hump after the PGDBS. With the same geometric and material parameters in the measurement and the simulation, fixed charges were placed in four specific regions as shown in the inset of Fig. 5(b). Fig. 5(a) shows good agreement between experimental and simulation results, verifying the proposed mechanism. The quantity of the injected fixed charges in each region is defined in Fig. 5(b). The trapped charge increases with the stress time and it is most significant at the G-S overlap region.

IV. Conclusion

We investigated the hump characteristics observed in the turn-on state after high PGDBS in n-channel bottom gate a-IGZO TFTs. This hump is shown to be due to the localized trapping of electrons at the active-layer/gate-insulator interface and inside the gate-insulator near the G-S electrode overlap region. We modeled the TFT after PGDBS as a series connection of two transistors consisting of the main and parasitic TFTs. The parasitic TFT, for the G-S electrode overlapped region with localized electron trapping due to high vertical electric field, has higher threshold voltage ($V_{\mathrm{Tp}} > V_{\mathrm{Tm}}$) and shorter effective channel length ($L_{\mathrm{ch,p}} \cong L_{\mathrm{ov}} < L_{\mathrm{ch,m}}$) than those of the main TFT (V_{Tm}, $L_{\mathrm{ch,m}}$) right above the bottom gate with a floated back channel. Through a TCAD simulation for TFTs with various channel lengths, we verified the charge trapping for the hump, degradation mechanism, and series-connected TFT model. We expect that this study will help to prevent the hump phenomenon from inducing degradation in the pixel signal of current-driven displays.

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