The Effect of Gate and Drain Fields on the Competition Between Donor-Like State Creation and Local Electron Trapping in In–Ga–Zn–O Thin Film Transistors Under Current Stress

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***Abstract*— Thin-film transistors using In–Ga–Zn–O (IGZO) semiconductors were evaluated under positive bias stress with different gate and drain voltages (V_{GS} and V_{DS}, respectively). The transfer characteristics with respect to stress time were examined, focusing on the threshold voltage (V_T) values obtained when the source and drain electrodes are interchanged during readout (forward and reverse V_{DS} sweep). The V_T values shift toward either negative or positive values during stress, while transitions from negative to positive shifts are also observed. The negative V_T shift under positive bias stress is interpreted to occur by the generation of donor-like states related to ionized oxygen vacancies. On the other hand, positive V_T shifts result from the trapping of electrons near the IGZO/gate insulator interface. The transitions from negative to positive V_T shift are believed to result from the local electron trapping mechanism that gradually takes over donor-like state creation. From the experimental results and TCAD device simulation, it is suggested that a competition occurs between donor-like state creation and electron trapping. The relative magnitudes of the V_{GS} and V_{DS} fields determine which mechanism dominates, providing an analytical insight for the design of stable devices for driving transistors in AMOLED backplanes.**

***Index Terms*— Thin film transistor (TFT), In-Ga-Zn-O (IGZO), charge trapping, current stress, sub-gap states.**

I. Introduction

RECENT progresses in thin film transistors (TFT) technology based on oxide semiconductors such as In-Ga-Zn-O (IGZO) have expedited the manufacturing of high resolution flat panel displays [1], [2]. Since the first demonstration of amorphous IGZO TFTs reported by Nomura *et al.* [3] and their degradation mechanism by Kimura and Imai [4], intensive research on oxide semiconductors has been conducted worldwide [5], [6]. While only switching transistors are required in AMLCD backplanes, additional driving transistors are needed in AMOLED displays in order to convey electrical current to the emissive layer. The driving TFTs are thus constantly subjected to current stress. In a former publication, the degradation mechanism of IGZO TFTs under current stress was examined by monochromatic photonic capacitance-voltage spectroscopy (MPCVS) and TCAD simulations [7]. The present work consists of a more comprehensive study on the device degradation under current stress with different gate-to-source (V_{GS}) and drain-to-source (V_{DS}) voltages.

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II. Experimental Procedure

The fabrication procedure of bottom gate IGZO TFTs is described in the previous study [7]. Devices with channel width/length=W_{ch}/L_{ch} = 50/100 μm and gate-to-source/drain overlap length L_{OV} = 13 μm were characterized using an Agilent 4156C precision parameter analyzer. For each current-voltage (I-V) measurement of the transfer characteristics, the drain voltage (V_{DS}) was set at 10 V. The V_{GS}/V_{DS} combinations for the positive bias stress experiments were 10V/10V, 20V/10V, 30V/10V, 20V/10V, 20V/20V, 20V/30V, 30V/10V, 30V/20V, and 30V/30V. Here, $I_{DS,F}$ is the drain current measured under forward V_{DS} sweep (the drain and source configuration is identical to that during current stress), and $I_{DS,R}$ is the current measured under reverse V_{DS} sweep (the drain and source settings are interchanged with respect to the stress conditions).

The TCAD simulation of the sub-gap trap distributions was done using the following equations:

$$g_D(E) = N_{TD} \times \exp\left(\frac{E_V - E}{kT_{TD}}\right) + N_{GD} \times \exp\left(-\left(\frac{(E_V - E) + E_{GD}}{kT_{GD}}\right)^2\right) \quad (1)$$

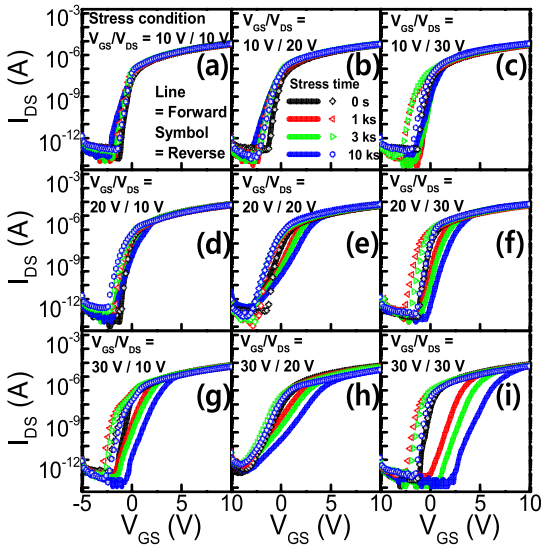

Fig. 1. Transfer characteristics of the IGZO TFT device under forward and reverse V_{DS} sweep conditions (V_{DS} = 10V). The V_{GS}/V_{DS} values for positive bias stress are (a) 10V/10V, (b) 10V/20V, (c) 10V/30V, (d) 20V/10V, (e) 20V/20V, (f) 20V/30V, (g) 30V/10V, (h) 30V/20V and (i) 30V/30V.

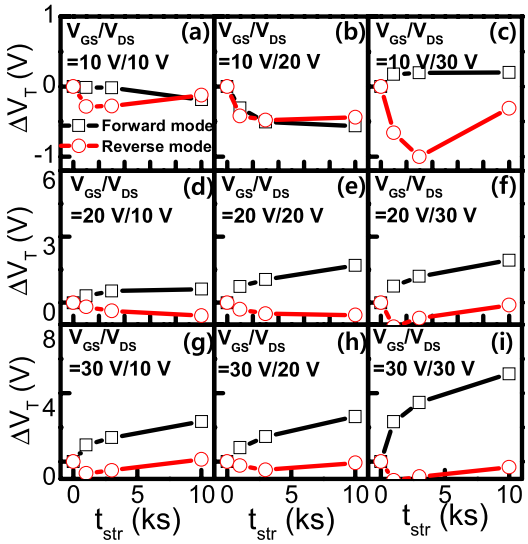

Fig. 2. Evolution of V_T values during stress. The squares represent the V_T values under forward V_{DS} sweep and the circles represent the V_T values under reverse V_{DS} sweep. The V_{GS}/V_{DS} values for positive bias stress are (a) 10V/10V, (b) 10V/20V, (c) 10V/30V, (d) 20V/10V, (e) 20V/20V, (f) 20V/30V, (g) 30V/10V, (h) 30V/20V and (i) 30V/30V.

$$g_A(E) = N_{TA} \times \exp\left(\frac{E - E_C}{kT_{TA}}\right) + N_{DA} \times \exp\left(\frac{E - E_C}{kT_{DA}}\right) + N_{GA} \times \exp\left(-\left(\frac{(E - E_C) + E_{GA}}{kT_{GA}}\right)^2\right) \quad (2)$$

where $g_D(E)$ denotes the distribution of donor-like traps and $g_A(E)$ the distribution of acceptor-like traps.

III. Results and Discussions

The solid lines and open symbols in Fig. 1(a) through (i) consist of the measured values of $I_{DS,F}$ and $I_{DS,R}$ respectively, during stress. Here, V_T is defined as the gate voltage that induces a drain current of 10 nA. With increasing stress time, the V_T values evolve differently under forward and reverse V_{DS} sweep. This is indicative of different physical phenomena taking place near the source and the drain regions, such as charge trapping or donor-like defect creation, respectively. The energy barriers become different at the source/IGZO junction and the IGZO/drain junction, which results in different gate voltages required to turn the device on and off when the source and drain electrodes are interchanged during readout. The V_T values with respect to stress time are shown in Fig. 2(a) through (i). Note that unusual behavior is observed under certain conditions, where the V_T values tend to shift in the negative direction first, and then switch directions towards positive values. For example, the V_T under reverse V_{DS} sweep ($V_{T,R}$) when V_{GS}/V_{DS} = 10V/30V (Fig. 2(c)) shifts in the negative direction for the first 3,000 seconds and shifts in the positive direction next.

The positive V_T shifts were demonstrated to occur by the trapping of electrons near the source electrode in our previous study [7]. TCAD simulations indicate that critical electric fields exist, above which donor-like state generation and electron trapping at the IGZO/gate insulator interface may occur. As shown schematically in Fig. 3(a), donor-like states can be created when fields greater than 5×10^4 V/cm are present. The critical field above which electron trapping becomes dominant is determined by considering the V_T shift under forward drain bias ($V_{T,F}$). When V_{GS}/V_{DS} = 10V/20V, the $V_{T,F}$ shifts in the negative direction (donor-like defect creation), while the opposite is observed when V_{GS}/V_{DS} = 10V/30V (electron trapping). A transition in the dominant degradation mechanism is thus expected to occur between V_{GS}/V_{DS} = 10V/20V and 10V/30V. For the latter two conditions, the average field near the source electrode is 2.86×10^5 V/cm, which may be estimated as the minimum value above which electron trapping becomes dominant, as shown in Fig. 3(b). The negative $V_{T,F}$ shifts below this value are suggested to result from the impact ionization of oxygen vacancies ($V_O + e^- \rightarrow V_O^{2+} + 3e^-$), creating donor-like sub-gap states as illustrated schematically in Fig. 3(c) [8]–[10].

The tendency to have electrons trapped in the gate insulator depends on the vertical direction and magnitude of the local field, while the probability of having donor-like states generated in the semiconductor is determined by the absolute magnitude of the local electric field regardless of its direction [8], [9].

As the gate voltage increases for a given drain bias, the presence of a Schottky barrier at the source/IGZO junction creates steep potential gradient in the semiconductor, inducing relatively high fields therein. The strong vertical gate fields convey high kinetic energy to the injected electrons, resulting in electrons being trapped mainly beneath the source electrode [7]. If the drain voltage increases for a given gate bias, an even steeper potential gradient is created in the semiconductor near the source junction. Such a phenomenon is manifested by more pronounced local electron trapping in the gate insulator in the vicinity of the source junction, which eventually screens the effects created by donor-like defects.

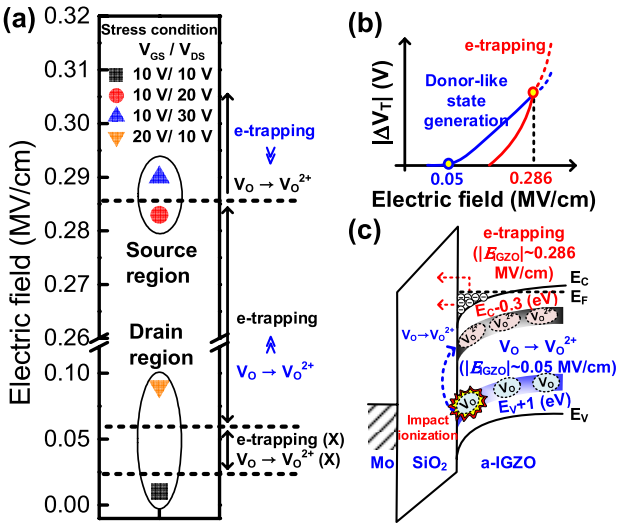

Fig. 3. (a) The relationship between total electric field magnitude and the dominant device degradation mechanism near the source and drain regions. (b) Schematic describing the competition between donor-like state generation and electron trapping, with respect to the absolute value of ΔV_T. (c) Schematic illustrating the electron trapping phenomenon and impact ionization of oxygen vacancies during positive bias stress. The neutral V_O levels at approximately $E_V + 1$ eV become excited to approximately $E_C - 0.3$ eV.

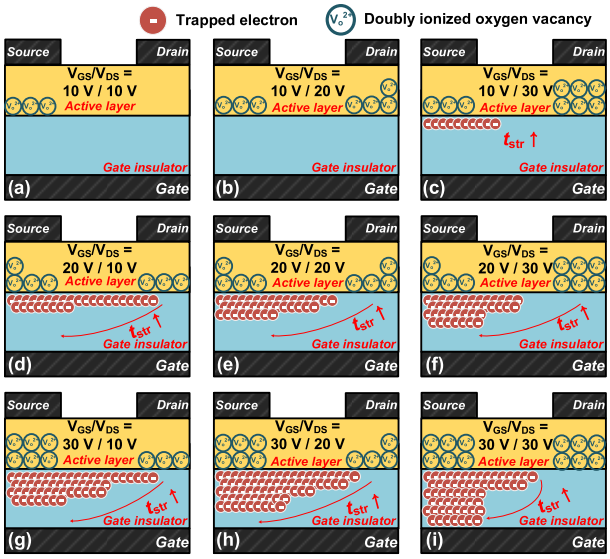

Fig. 4. Schematic describing the relative amounts of locally trapped electrons and donor-like states. Note that electrons become trapped mainly near the source electrode. The V_{GS}/V_{DS} values for positive bias stress are (a) 10V/10V, (b) 10V/20V, (c) 10V/30V, (d) 20V/10V, (e) 20V/20V, (f) 20V/30V, (g) 30V/10V, (h) 30V/20V and (i) 30V/30V.

Under reverse V_{DS} sweep, two stages of device degradation may be observed, as seen for $V_{T,R}$ in Fig. 2(c). The magnitude of the electric field near the drain junction is initially smaller than 2.86×10^5 V/cm from t = 0 up to 3000 s, so that donor-like state creation is dominant. However at t = 3000 s, TCAD simulations of the I-V curves indicate that the field magnitude exceeds 2.86×10^5 V/cm, so that electron trapping becomes dominant at beneath the drain electrode and $V_{T,R}$ begins to shift in the positive direction. Such results show that under certain V_{GS}/V_{DS} conditions, gradual transitions in the device degradation mechanism may take place.

Fig. 4 (a) through (i) depict well the relative amounts of donor-like states and trapped electrons at different locations of the devices under different V_{GS}/V_{DS} conditions. For Fig. 4(a) to (c), the drain voltage increases while V_{GS} is kept at 10 V. The kinetic energy of the electrons when $V_{DS} = 10$ V is not sufficiently high to induce electron trapping, however the local field near the source is large enough to induce donor-like state creation. Therefore the $V_{T,F}$ shift towards negative values. For $V_{DS} = 10$ V and 20 V, the electric field near the drain is large enough to create donor-like states so the $V_{T,R}$ shift mainly towards negative values. However when $V_{DS} = 30$ V, the kinetic energy of the electrons injected at the source/IGZO junction is high enough to have the carriers trapped in the gate insulator, so the $V_{T,F}$ shifts in the positive direction, while $V_{T,R}$ switches direction after t = 3000s.

For Fig. 4(d) to (f), the gate field ($V_{GS} = 20$ V) is large enough to induce sufficient electron trapping by the source electrode, resulting in positive shifts in $V_{T,F}$ in all cases. However at $V_{DS} = 10$ V and 20 V, the creation of donor-like states is dominant at the drain junction, so that the $V_{T,R}$ shift in the negative direction. At $V_{DS} = 30$ V, the local field beneath the drain electrode is larger than 2.86×10^5 V/cm after 1000 s, and so $V_{T,R}$ begins to switch directions towards positive values.

Finally, for Fig. 4(g) to (i), the gate bias ($V_{GS} = 30$ V) is large enough to convey high kinetic energy to the electrons injected at the source junction, so relatively large positive shifts in $V_{T,F}$ are observed compared to the respective $V_{GS} = 20$ V conditions. All $V_{T,R}$ initially shift towards negative values and then switch directions during stress, which is a result of electron trapping gradually becoming dominant, owing to the relatively large V_{GS} value of 30 V.

The balance between donor-like state creation and electron trapping is thus critical in the design of driving transistors in AMOLED backplanes, so as to achieve equilibrium between negative and positive V_T shifts during operation.

IV. Conclusion

In this work, the degradation of IGZO TFTs under positive bias stress with different V_{GS}/V_{DS} combinations was studied based on I-V measurements and TCAD simulations. The analyses indicate that electron trapping at the IGZO/gate insulator interface occurs in most cases near the source electrode, and donor-like state creation takes place near both the source and drain regions during stress. It is found that a competition exists between the two mechanisms, which tend to induce negative (donor-like defects) and positive (electron trapping) V_T shifts. The trapping of electrons is determined by the vertical electric field originating from the gate bias, and the generation of donor-like states depends on the absolute value of the local electric field, which is suggested to induce impact ionization of oxygen vacancies by free electrons.

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