Fabrication of InGaAs-on-Insulator Substrates Using Direct Wafer-Bonding and Epitaxial Lift-Off Techniques

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***Abstract*— Defect less semiconductor-on-insulator (-OI) by a cost-effective and low-temperature process is strongly needed for monolithic 3-D integration. Toward this, in this paper, we present a cost-effective fabrication of the indium gallium arsenide-OI structure featuring the direct wafer bonding (DWB) and epitaxial lift-off (ELO) techniques as well as the reuse of the indium phosphide donor wafer. We systematically investigated the effects of the prepatterning of the III–V layer before DWB and surface reforming (hydrophilic) to speed up the ELO process for a fast and high-throughput process, which is essential for cost reduction. This method provides an excellent crystal quality of $In_{0.53}Ga_{0.47}As$ on Si. Crystal quality of the film was evaluated using Raman spectra, and transmission electron microscope. Finally, we achieved good electrical properties of $In_{0.53}Ga_{0.47}As$-OI metal-oxide-semiconductor field-effect-transistors fabricated through the proposed DWB and ELO.**

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***Index Terms*— III–V, III–V compound semiconductor, epitaxial lift-off (ELO), indium gallium arsenide (InGaAs), InGaAs-on-insulator (OI), metal-oxide-semiconductor field-effect-transistors (MOSFETs), wafer bonding.**

I. Introduction

FOR many decades, development of the Si-based complementary- metal-oxide-semiconductor (CMOS) technology has been achieved by scaling down of devices. Now, physical limitations such as short-channel effects are confronting Si-based CMOS industry, indicating that simple scaling strategy is no more effective to enhance the device performance [1], [2]. Monolithic 3-D (M3-D) integration is a promising pathway to reduce the interconnect delay and increase the transistor density [3]–[6]. Consequently, it can reduce the power density of the chip which allows the ultimate power scaling [3]–[7]. However, the current technology has technological challenges as shown in Fig. 1, which requires low-temperature process for the fabrication of the top field-effect-transistor (FET) as well as low-cost process [3], [9]–[14]. This is an inevitable tradeoff between the performance of top FETs and lowering the process temperature to use Si-based channel materials. It is because the process temperature for top FET should be low enough to avoid the thermal damage in formerly fabricated bottom FETs, whereas it requires quite high process temperature to ensure the high performance of top FETs [13], [14]. On the other hand, a process temperature of III–V [such as indium gallium arsenide (InGaAs)] FETs is typically quite low (<400 °C), which induces no effect on the bottom FET and the interconnect metallization. Furthermore, In-rich InGaAs is expected to be the most attractive channel for the next-node transistors due to its high electron mobility [7], [15]–[19]. Recent studies demonstrated high-performance InGaAs-on insulator (-OI) metal-oxide-semiconductor FETs (MOSFETs), which are highly scalable and the most straightforward device structure for M3-D implementation [19], [20]. From the viewpoint of mass production, the current key issue is a cost-effective integration of III–V materials on a Silicon (Si) platform. There were many attempts such as direct growth on Si [15], direct wafer bonding (DWB) [21], [22], and aspect ratio trapping [23]. However, growth-based methods suffer

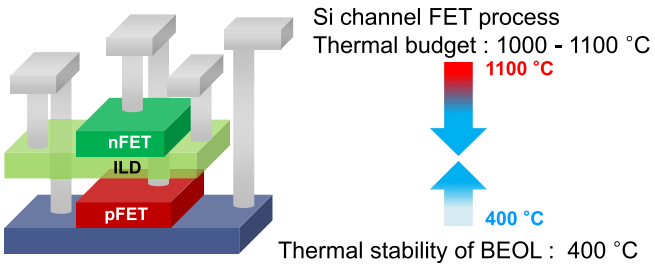

Fig. 1. Schematic of the M3-D integration and its integration challenge of process temperature, which can be overcome using III–V semiconductor.

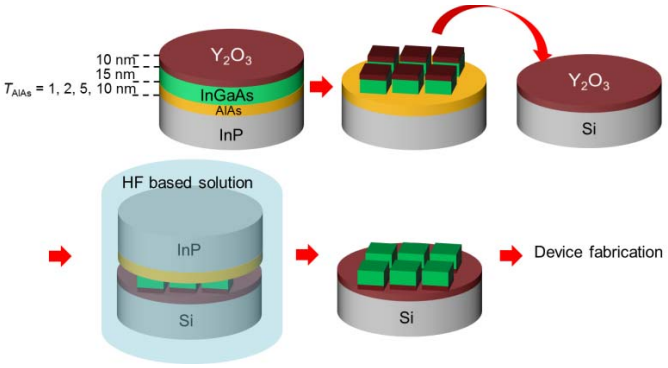

Fig. 2. Process flow for the $In_{0.53}Ga_{0.47}As$-OI wafer fabrication through the proposed wafer-bonding technique, which can significantly reduce the wafer cost by reusing of the separated donor wafer.

from the defect control due to the large lattice mismatch between III–V and Si. DWB is a promising technique for good epitaxial quality, whereas many studies use high-cost process such as etch-out of the donor substrate [21], [22]. Even though Czornomaz *et al.* [7] demonstrated the smart-cut technique for InGaAs-OI fabrication, this also requires many process sequences such as ion implantation and chemical–mechanical polishing process [8].

On the other hand, DWB which is accomplished by the epitaxial lift-off (ELO) seems to be a very promising approach for high-quality III–V-OI/Si as well as a low-cost process by reuse of the donor wafer. However, conventional ELO techniques have been studied using a GaAs donor wafer to use lattice-matched sacrificial layer of Aluminum arsenide (AlAs) [24]–[28], resulting in difficulty, in the use of In-rich InGaAs material due to the 7% lattice mismatch between GaAs and InAs. Also, many studies with GaAs donor wafer showed very long processing time (low throughput) due to long lateral etching distance and hydrophobic surfaces due to the difficulty of H_2 bubble release and etching solution flow. There is some study on ELO of epitaxial layer grown on indium phosphide (InP) with AlAs sacrificial layer [29], but ELO study on InP substrate is very limited. In their work, they also issued the long ELO time, which is typical drawback/limitation of ELO process. Therefore, they mounted a 13-g weight on the plastic substrate to increase the gap between epitaxial layer and InP and enhance the ELO speed. However, here, it should be noted that this approach cannot be directly applied to fabricate $In_{0.53}Ga_{0.47}As$ transistor on Si, because Si substrate is rigid and is almost impossible to band it to enhance ELO speed. We also reported DWB and ELO process using Y_2O_3 and AlAs sacrificial layers, respectively [30]. However, our previous study demonstrated limited analysis of the epitaxial layer quality before and after DWB and ELO. Also, etching mechanism itself was not sufficiently explained and analyzed, yet.

Therefore, in this paper, we focused more on the investigation of channel layer quality and electrical properties with respect to the thickness of AlAs sacrificial layer (T_{AlAs}). To deeply investigate the quality of channel layer, we used several analysis technique such as atomic force microscopy (AFM) and transmission electron microscope (TEM).

To fully utilize the benefit of M3-D with the InGaAs channel, we developed the DWB and ELO techniques to form the InGaAs layer on Si substrates as shown in Fig. 2. Here, we also developed the growth of the AlAs sacrificial layer on the InP donor substrate. We demonstrate InGaAs-OI MOSFETs on a Si substrate using the DWB and ELO processes with an InP donor wafer and an AlAs sacrificial layer. For high throughput, prepatterning of the III–V layer before DWB was carried out [28]. Also, we systematically investigated the ELO behavior with various T_{AlAs}, which is a critical parameter for the ELO time, the InGaAs quality, and the different etchants. From this, we provided the design principle of fabrication process to speed up the ELO process considering various physical conditions. As a result, the proposed method provides high throughput of In-rich InGaAs-OI/Si wafer and high quality of the InGaAs channel. Also, the proposed method provides an integration pathway for cost-effective M3-D using the high-quality InGaAs layer.

II. Fabrication of $In_{0.53}Ga_{0.47}As$-OI/SI Wafer and Evaluation of Film Quality

An $In_{0.53}Ga_{0.47}As$-OI/Si wafer was fabricated by DWB and ELO as shown in Fig. 2. First of all, $In_{0.53}Ga_{0.47}As$ (15 nm, undoped)/AlAs (sacrificial layers) layers were epitaxially grown on InP substrate by a metal organic chemical vapor deposition. Here, T_{AlAs} was varied to 1, 2, 5, and 10 nm to investigate the $In_{0.53}Ga_{0.47}As$ quality and the ELO time. Subsequently, a 10-nm-thick Y_2O_3 layers were deposited both on III–V($In_{0.53}Ga_{0.47}As$/AlAs/InP) and on Si wafers, respectively. Before DWB, donor wafers were prepatterned for a fast ELO via efficient gas bubble (product during etching) release and increase in the exposed area of the AlAs sacrificial layer [31]. Here, the pattern size was fixed to be $100 \times 100\ \mu m^2$. Then, Y_2O_3/$In_{0.53}Ga_{0.47}As$/AlAs/InP substrate and Y_2O_3/Si substrate were bonded to each other in the air with a prior surface activation by O_2 plasma. Finally, $In_{0.53}Ga_{0.47}As$-OI /Si substrates and InP donor wafer were separated by the selective etching of the AlAs layer in the HF-based solution.

Fig. 3(a)–(c) shows an AFM image of the surface of as-grown $In_{0.53}Ga_{0.47}As$/AlAs (2, 5, 10 nm)/InP substrate before the DWB. The samples with $T_{AlAs} = 2$ and 5 nm show very flat surface with a root mean square (R_{rms}) value = 0.11 and 0.18 nm, respectively. However, the sample with

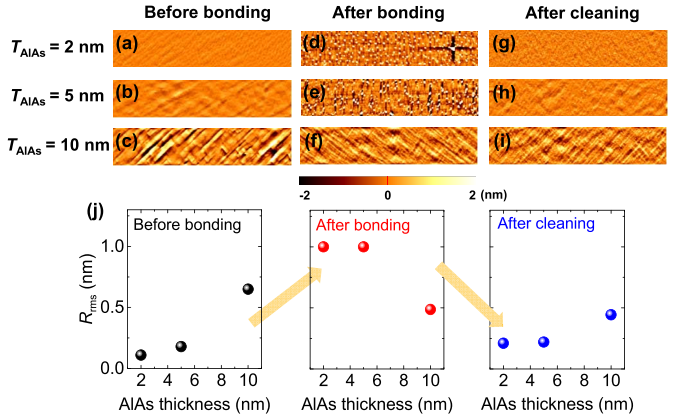

Fig. 3. AFM images of the $In_{0.53}Ga_{0.47}As$ surface on AlAs/InP before bonding with T_{AlAs} = (a) 2 nm, (b) 5 nm, and (c) 10 nm. AFM images of the $In_{0.53}Ga_{0.47}As$ surface immediately after bonding with T_{AlAs} = (d) 2 nm, (e) 5 nm, (f) 10 nm, and after cleaning with T_{AlAs} = (g) 2 nm, (h) 5 nm, (i) 10 nm and (j) R_{rms} value of the $In_{0.53}Ga_{0.47}As$ surface before bonding, after bonding, and after cleaning of samples.

T_{AlAs} = 10 nm shows a rough surface with an R_{rms} value = 0.65 nm due to the large lattice mismatch between the InP substrate and the AlAs layer. Fig. 3(d)–(f) shows AFM images of the surface of $In_{0.53}Ga_{0.47}As$-OI after DWB and ELO. $In_{0.53}Ga_{0.47}As$ surfaces were roughened shortly after ELO process due to the residue formed by etching reaction of AlAs layers for the sample with T_{AlAs} less than 5 nm. When AlAs layer etched by HF solution, an etching residue was formed, such as AlF_3 and As_2O_3. These have not good aqueous solubility, which cause to high surface roughness shortly after ELO process [24], [32]. Here, because of fast ELO in the sample with T_{AlAs} = 10 nm, a surface roughening was not observed. However, the flat and clean surface with an R_{rms} value was obtained after the HCl cleaning as shown in Fig. 3(g)–(i). $In_{0.53}Ga_{0.47}As$ layers transferred to T_{AlAs} = 2 and 5 nm show a very smooth surface with a small R_{rms} = 0.21 and 0.22 nm, respectively. Fig. 3(j) shows R_{rms} value of the $In_{0.53}Ga_{0.47}As$ surface before and after bonding as well as after cleaning of the samples.

To investigate the $In_{0.53}Ga_{0.47}As$ quality, we measured the Raman spectra of $In_{0.53}Ga_{0.47}As$/AlAs/InP substrate with different T_{AlAs} before the DWB, as shown in Fig. 4(a). The $In_{0.53}Ga_{0.47}As$ peak was quite sharp with T_{AlAs} < 5 nm, whereas a slightly broader peak was observed in the sample with T_{AlAs} = 10 nm. Also, $In_{0.53}Ga_{0.47}As$ peaks show a positive shift with an increase of T_{AlAs} (0, 2, 5, 10 nm) due to the compressive strain caused by the lattice mismatch between AlAs and $In_{0.53}Ga_{0.47}As$. After DWB and ELO process, as shown in Fig. 4(b), the Raman spectra of $In_{0.53}Ga_{0.47}As/Y_2O_3$/Si substrate shows both sharp peaks of $In_{0.53}Ga_{0.47}As$ and Si, indicating successful fabrication of high-quality $In_{0.53}Ga_{0.47}As$-OI on Si substrates. Fig. 5 shows the cross-sectional TEM images of samples right after the epitaxial growth. Fig. 5(a) shows a clean interface between AlAs and $In_{0.53}Ga_{0.47}As$ layers without visible defects or dislocations. Fig. 5(b) also shows clean interface between AlAs and $In_{0.53}Ga_{0.47}As$ layers.

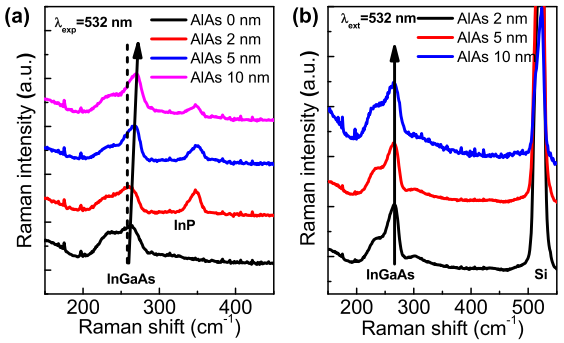

Fig. 4. (a) Raman spectra of $In_{0.53}Ga_{0.47}As$/AlAs/InP substrate with different T_{AlAs} before the DWB and (b) Raman spectra of $In_{0.53}Ga_{0.47}As/Y_2O_3$/Si substrate after bonding.

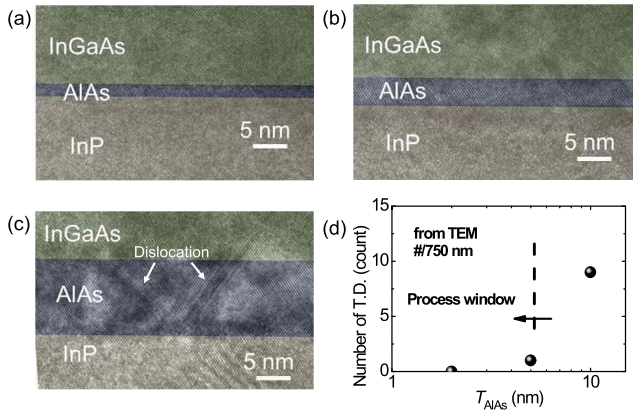

Fig. 5. Cross-sectional TEM image of $In_{0.53}Ga_{0.47}As$/AlAs/InP with T_{AlAs} = (a) 2 nm, (b) 5 nm, and (c) 10 nm. While samples with T_{AlAs} = 2 and 5 nm show excellent crystal quality, the sample with T_{AlAs} = 10 nm shows many threading dislocations. (d) Extracted number of threading dislocations with T_{AlAs} = 2, 5, and 10 nm, which indicates process window of T_{AlAs} less than 5 nm.

Fig. 5(c) shows misfit dislocation lines from AlAs to $In_{0.53}Ga_{0.47}As$, which would be caused by the large lattice mismatch. From the image, the poor electrical characteristics of $In_{0.53}Ga_{0.47}As$ grown on T_{AlAs} of 10 nm were expected. The number of dislocations seen in TEM is summarized in Fig. 5(d), indicating process window of T_{AlAs} and ensuring that high crystal quality was less than 5 nm. Cross-sectional TEM image of the fabricated $In_{0.53}Ga_{0.47}As$-OI on Si substrate from the sample with T_{AlAs} = 5 nm is shown in Fig. 6. The TEM shows very uniform $In_{0.53}Ga_{0.47}As$ layer on Y_2O_3 on Si substrates. High-resolution image shows excellent crystal quality and successful DWB behavior with a nearly indistinguishable bonding interface. EDX profiles also confirmed sharp interface and material structure. As from the Raman spectra (Fig. 4), these results suggest that bonded $In_{0.53}Ga_{0.47}As$ films on Si have no residual strain in the film.

III. Discussion on the Impacting Factor on ELO Time

To understand and make the ELO fast, the etching mechanisms for improved reaction speed are investigated. The etching mechanism of the AlAs layer by the HF-based solution

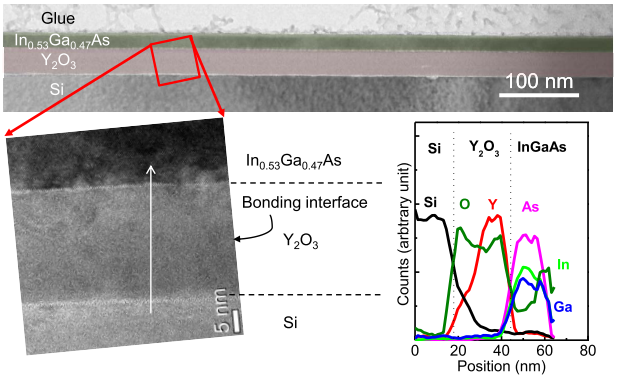

Fig. 6. Cross-sectional TEM image of $In_{0.53}Ga_{0.47}As$-OI on Si substrate. It shows excellent crystal quality and bonding interface. EDX profiles also clearly confirmed the sharp interface.

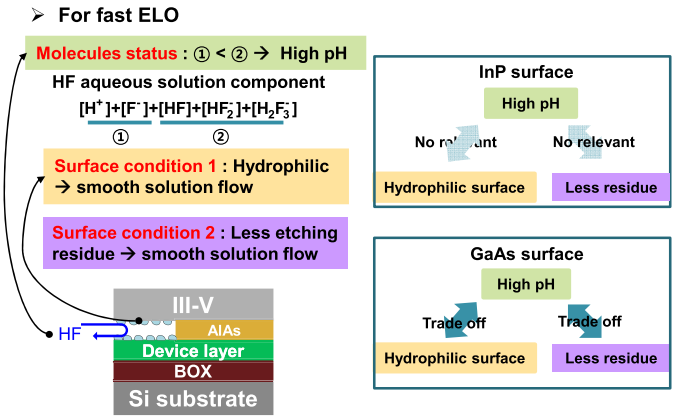

Fig. 7. Schematic illustration of the AlAs etching process for fast ELO. It shows the necessity of high concentration of undissociated HF and hydrophilic surface with less etching residue. Also, it shows the relation of fast ELO at high pH, hydrophilic surface and $t_{Residue}$ about InP and GaAs surface.

is shown in Fig. 7. To speed up the etching, it is important to achieve a high concentration of the undissociated HF, hydrophilic surface, and less amount of etching residues [33]. First, the etching reaction between AlAs and undissociated HF is preferred to enhance the ELO speed. Because, the reaction between AlAs and undissociated HF is a one-step process, whereas the reaction between AlAs and dissociated HF is a two-step process [32]. Therefore, to meet this requirement, etching solutions should show high pH values. Also, to make an efficient flow of the etchant and reaction product, a hydrophilic surface and less amount of etching residue is mandatory [24]. However, these were found to have a strong tradeoff relationship on the GaAs surface, which makes the ELO fundamentally slow. However, InP surface shows hydrophilic surface with less amount of etching residue in HF solutions with a high pH, resulting in a fast ELO process.

To investigate the effect of pH and surface condition, we measured the solution dependence of pH, thickness of the etching residue ($t_{Residue}$), contact angle, and ELO time using an HF-based solution diluted with different substances as shown in Fig. 8. Here, $t_{Residue}$ was measured by ellipsometry after dipping the sample in each HF-based solution for 6 h.

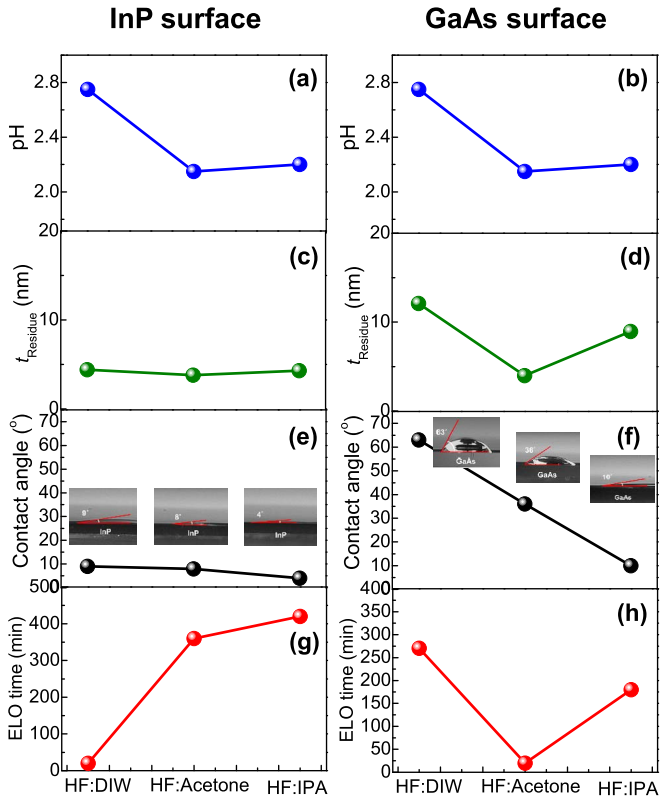

Fig. 8. Characteristics of solution dependence of (a) and (b) pH, (c) and (d) $t_{Residue}$, (e) and (f) contact angle, and (g) and (h) ELO time using HF-based solution diluted with different substances for InP and GaAs, respectively.

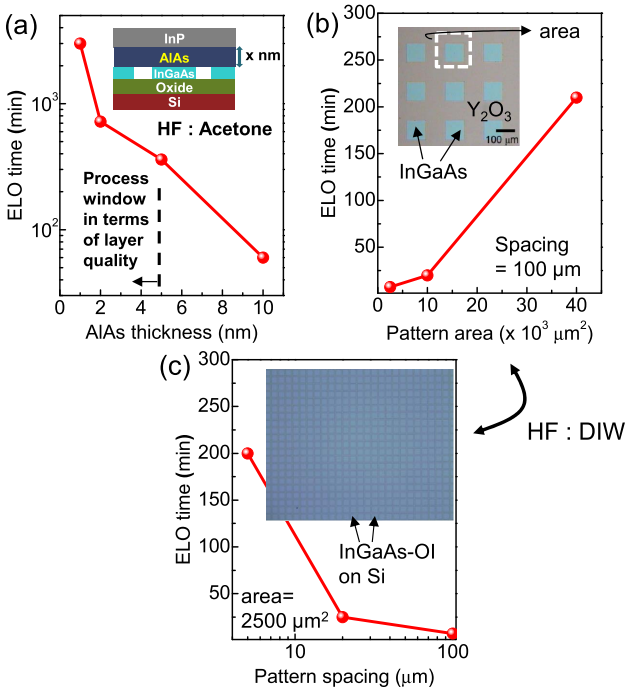

Fig. 9. (a) T_{AlAs} dependence of the ELO time for separation of the InP from $In_{0.53}Ga_{0.47}As$-OI/Si in HF solution. (b) Pattern area dependence of the ELO time with a spacing of 100 μm. (c) Pattern spacing dependence of the ELO time with a fixed pattern area of 2500 μm^2.

HF solution with high pH (HF:DIW than HF:acetone and HF:IPA) is clearly observed with a short ELO time on the InP surface contrary to the GaAs surface [24]. It is due to the

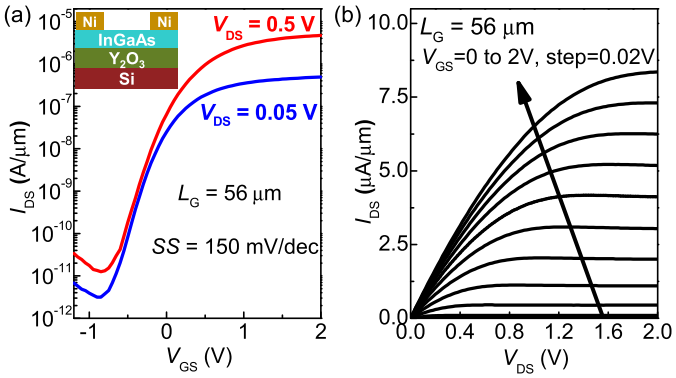

Fig. 10. (a) Transfer. (b) Output characteristics of bottom-gate $In_{0.53}Ga_{0.47}As$-OI MOSFETs with $Lg = 56$ μm. Transfer curves show high on/off ratio of 10^5. Output curves also show good current saturation.

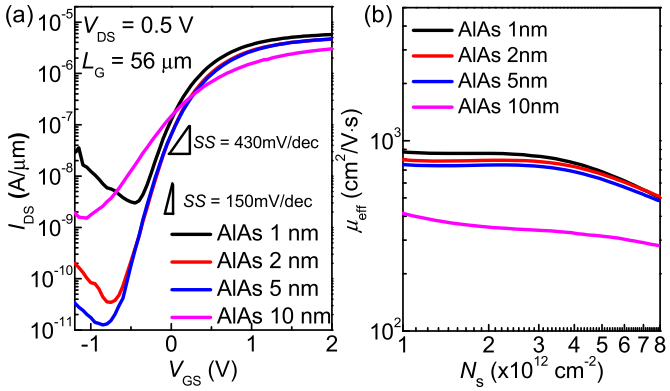

Fig. 11. (a) Transfer curves. (b) Mobility characteristics of $In_{0.53}Ga_{0.47}As$-OI MOSFETs using transferred $In_{0.53}Ga_{0.47}As$ using InP donor wafer with T_{AlAs} of 1, 2, 5, and 10 nm.

thick residue of HF:DIW and HF:IPA on GaAs, which makes the ELO slow as shown in Fig. 8(d). Here, the etching residue limiting further ELO reaction is known to be Arsenic (As) film [33], which is generated by the reaction ($GaAs_{(s)} + 3HF_{(aq)} \rightarrow GaF_{3(aq)} + AsH_{3(g)} \Delta G = -21$ kcal/mol, $2AsH_{3(g)} \rightarrow 2As_{(s)} + 3H_{2(g)} \Delta G = -153$ kcal/mol). Gibbs free energy (ΔG) for these two reaction is negative and the value of the secondary reaction is quite high, indicating reaction is spontaneously occurred [33]–[37]. Therefore, As film is formed between epitaxial layer and substrate hinders further chemical reaction. On the other hand, InP surface shows a less $t_{Residue}$ for all HF solutions allowing a fast ELO as shown in Fig. 8(c), because the chemical reaction is quite different on InP surface. Similar reaction can be considered in InP ($InP_{(s)} + 3HF_{(aq)} \rightarrow InF_{3(s)} + PH_{3(g)} \Delta G = -39$ kcal/mol, $2PH_{3(g)} \rightarrow 2P_{(s)} + 3H_{2(g)} \Delta G = 32.2$ kcal/mol) [35], [37]. For InP, ΔG is positive in the secondary reaction, indicating this reaction is hard to be occurred. However, in the first reaction, InF_3 solid can be formed, which can make the ELO reaction difficult. We believe that this film can only be formed on the surface, because further reaction will be possibly stopped when the surface was coated by InF_3 layer. We also investigated the contact angle of HF-based solutions at InP and GaAs surface to see the hydrophilicity of the solution for each substrates as shown in Fig. 8(e) and (f). The contact angle on InP surface was small independently of HF-based solutions, which also allows a fast ELO. However, the contact angle on GaAs surface has the smallest value at HF:IPA solution, which is the strong tradeoff considering the requirement for fast ELO (large pH and less $t_{Residue}$). As a result, the ELO time strongly depends on pH of HF-based solutions on InP surface. On the other hand, the ELO on GaAs surface was the fastest in HF: acetone solution due to the relatively small contact angle and small $t_{Residue}$ as shown in Fig. 8(g) and (h).

We also observed a physical-dimension dependence of T_{AlAs} and prepattern before DWB, which are also critical for fast ELO process. T_{AlAs} dependence of ELO time is shown in Fig. 9(a). Faster ELO was observed with thicker T_{AlAs}, whereas the process window of T_{AlAs} in terms of layer quality is quite thin considering the large lattice mismatch-induced surface roughening. These results indicate that an appropriate design of T_{AlAs} is important to achieve both fast ELO process and good layer quality. To confirm the possibility of transferring a dense pattern, we also investigated the ELO time dependence of the prepatterned area and spacing in Fig. 9(b) and (c). Here, we changed the prepatterned area and spacing area. The prepatterned area was varied to be 50×50, 100×100, and 200×200 μm^2 with a fixed spacing of 100 μm. Also, spacing between patterns was varied to be 5, 20, and 100 μm with a fixed prepatterned area of 50×50 μm^2. We found that the ELO time strongly depends on the prepattern size. ELO time was significantly decreased with a decrease in the prepatterned area. Prepatterned area of 50×50 μm^2 sample showed the fastest ELO time as fast as 8 min as shown in Fig. 9(b). On the other hand, the sample with narrow spacing between patterns showed slower ELO time as shown in Fig. 9(c), showing that there is a tradeoff between reduction in the pattern spacing and the ELO time. These results clearly indicate that the pattern design for prepatterning before the DWB is important for both a dense pattern transfer and a fast ELO process.

IV. Electrical Characterization of $In_{0.53}Ga_{0.47}As$-OI MOSFETs

To investigate the electrical characteristics of the transferred $In_{0.53}Ga_{0.47}As$ layer, we fabricated bottom-gate $In_{0.53}Ga_{0.47}As$-OI MOSFETs with Ni source/drain (S/D). Here, from the analysis of electrical properties of long-channel MOSFETs, the layer quality of transferred layer can be validated, whereas Raman, TEM can only show the information of small area of the sample. The device consisted of a 15-nm-thick $In_{0.53}Ga_{0.47}As$ channel (unintentionally doped)/20-nm-thick Y_2O_3 gate oxide/Si with doping concentration $N_D \sim 1 \times 10^{19}$ cm^{-3}. The final device structure is shown in the inset of Fig. 10(a). First, device isolation was carried out by the mesa etching process with Al_2O_3 field oxide. Then, Ni was deposited for S/D contacts by the electron beam evaporator, followed by thermal annealing at 250 °C for 1 min in an N_2 ambient. Fig. 10(a) and (b) shows transfer and output curves of the bottom-gate $In_{0.53}Ga_{0.47}As$-OI MOSFETs with a gate length $L_G = 56$ μm, fabricated from

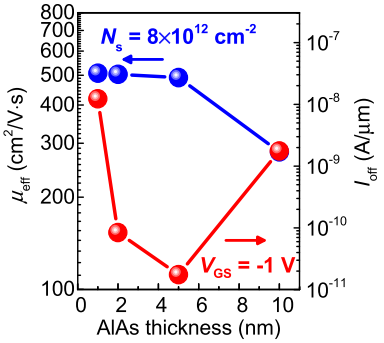

Fig. 12. Comparison with mobility at high-field region and I_{OFF} as a function with T_{AlAs} of 1, 2, 5, and 10 nm.

the sample with a $T_{AlAs} = 5$ nm. We obtained good transfer curves with a steep subthreshold slope (*SS*) of 150 mV/dec and high on/off ratio of 10^5. Also, a clear current saturation was observed in the output curves in Fig. 10(b). Fig. 11(a) shows drain current (I_{DS})–gate voltage (V_{GS}) transfer curves of $In_{0.53}Ga_{0.47}As$-OI MOSFETs from $T_{AlAs} = 1$, 2, 5, and 10 nm. Steep transfer behaviors were observed in the sample from thin T_{AlAs} less than 5 nm, whereas the transfer curves from the sample with a $T_{AlAs} = 10$ nm shows large *SS* due to poor layer quality and uniformity. On the other hand, I_{DS}–V_{GS} curve transferred from $T_{AlAs} = 1$ and 2 nm shows larger OFF-current than that from $T_{AlAs} = 5$ nm. This is because $In_{0.53}Ga_{0.47}As$ layers were damaged by HF solutions during a long time process of ELO. As mentioned in Section III, an etching residue of As film after dipping the sample in HF solution for a long time was produced by the reaction between GaAs and HF. Finally, after air exposure, As film is changed to As_2O_3 or As_2O_5 by the reaction with H_2O in the air [32]. Although As_2O_3 or As_2O_5 are partially removed by HCl solution and it shows good surface morphology as shown in Fig. 3, but complete removal of As_2O_3 or As_2O_5 by HCl solution is quite difficult [38]. We think that remaining arsenic oxide and related trap caused the surface leakage current and we believe that this can be eliminated using another surface cleaning solution such as NH_4OH or adding surface protection layer of InP between $In_{0.53}Ga_{0.47}As$ channel and AlAs.

The effective mobility (μ_{eff}) characteristics of each sample are shown in Fig. 11(b) as a function of sheet charge carrier density (N_s). As expected from the transfer curves, μ_{eff} of the samples from $T_{AlAs} = 1$, 2, and 5 nm show higher values than that from $T_{AlAs} = 10$ nm. Fig. 12 summarized μ_{eff} of the $In_{0.53}Ga_{0.47}As$-OI MOSFETs at $N_s = 8 \times 10^{12}$ cm^{-2} and OFF-current density at $V_{GS} = -1$ V as a function of T_{AlAs}. We obtained similar μ_{eff} in T_{AlAs} with 1, 2, 5 nm, whereas the sample transferred from T_{AlAs} of 10 nm shows lower μ_{eff} than other samples due to the poor channel quality caused by the lattice mismatch between $In_{0.53}Ga_{0.47}As$ and AlAs layers. Also, the sample transferred from $T_{AlAs} = 5$ nm shows the lowest OFF-current density, thanks to the fast ELO process without any damage during the ELO process shown in the sample with T_{AlAs} of 1 and 2 nm. Considering the thick EOT (20-nm-thick Y_2O_3) and unpassivated/-optimized process, further improvement is still possible. It should be noted that these results highlight the first successful operation of $In_{0.53}Ga_{0.47}As$-OI MOSFETs fabricated by DWB and ELO.T_{AlAs}-dependence of the donor wafer on the electrical properties of $In_{0.53}Ga_{0.47}As$-OI MOSFETs indicates that high film quality was achieved using the proposed method with $T_{AlAs} < 5$ nm as shown in Fig. 12. Finally, Table I summarizes various integration schemes of III–V on Si, showing that the proposed scheme provides high-quality III–V integration on Si with a cost-effective process [21]–[23], [39]. Moreover, the ELO techniques are comparatively benchmarked in Table II [24]–[28]. The proposed integration scheme provides a high-quality $In_{0.53}Ga_{0.47}As$-OI with the highest throughput (fast ELO) and the most cost-effective process (thin AlAs). If we estimate the etching rate of AlAs by HF, it would be around 5 μm/min (100 μm for 20 min). It seems to be long compared with the fastest etching rate of 14.3 μm/min in [33]. However, it should be noted that in our ELO process, all of the patterns with a pattern size of 100×100 μm^2 are simultaneously etched in the HF solution; thereby the throughput of ELO process is quite high if we compare the ELO time with a large wafer size. Also, other studies reporting that all relatively fast ELO process uses flexible carrier to increase the ELO speed, but our work report the fastest process of film transfer from rigid substrate (InP) to rigid substrate (Si).

TABLE I
BENCHMARK OF THE INTEGRATION METHOD OF III–V MATERIAL ON Si SUBSTRATES

	DWB (grown on III-V Sub.) [21]	DWB (grown on Si Sub.) [22]	ART [23]	CELO [39]	This work
Wafer size > 300 mm	×	●	●	●	●
Cost	High	Medium	Low	Low	Low
Growing method	III-V/III-V Sub.	III-V/thick buffer/ Si Sub.	III-V/buffer/Si Sub.	Lateral growth	III-V/III-V Sub.
Channel layer quality	●	▲	▲	●	●
Back interface control	●	●	×	×	●
SCEs control	UTB or Fin	UTB or Fin	Fin	UTB or Fin	UTB or Fin

TABLE II
COMPARISON OF ELO TECHNIQUES WITH OTHER GROUPS

	IBM T.J. Watson [24]	U. Michigan [26]	U. National Chung Hsing [27]	AIST [28]	This work
Donor substrate	GaAs	GaAs	GaAs	GaAs, Ge	InP
ELO time	8 hours	5 hours	3 hours	5 hours	20 min
Sacrificial layer	InAlP (100 nm)	AlAs (20 nm)	AlAs (20 nm)	AlAs (5-150 nm)	AlAs (5 nm)
Application	LED, MOScap, Solar cell	LED, MESFETs, Solar cell	Solar cell	CMOS	CMOS

V. Conclusion

We developed the ELO techniques to from high-quality $In_{0.53}Ga_{0.47}As$-OI structure on Si for M3-D integration. We also first demonstrated $In_{0.53}Ga_{0.47}As$-OI MOSFETs on Si using the developed ELO technique, which employed prepatterning before DWB and InP donor wafer. We systematically investigated the effect of T_{AlAs} on epitaxial $In_{0.53}Ga_{0.47}As$ film and ELO behaviors with various HF solutions (pH) and surface states (GaAs vs. InP). We found that InP surface is more favorable for fast ELO than GaAs, which is the material system ELO typically used. Using DWB and ELO, $In_{0.53}Ga_{0.47}As$-OI shows excellent film quality and good electrical properties. This ELO concept is promising to provide a cost-effective III–V M3-D integration scheme on the Si platform for the next-generation logic applications.

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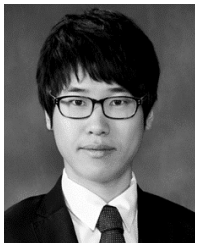

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