Degradation on the Current Saturation of Output Characteristics in Amorphous InGaZnO Thin-Film Transistors

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***Abstract*— Degradation on the current saturation of the output characteristics in amorphous indium–gallium–zinc–oxide (a-IGZO) thin-film transistors with the bottom-gate structure is investigated. As the drain-to-source voltage (V_{DS}) increases at a fixed gate-to-source voltage (V_{GS}), the current from drain to source (I_{DS}) becomes nonsaturated and increases due to the mobility enhancement and I_{DS} also decreases again due to the electron trapping into the gate insulator and/or an interface, which occurs mainly at the channel edge near a drain. Analysis is validated by using the pulsed I_{DS}–V_{DS} measurement. Nonsaturated current is attributed to the Joule heating-assisted mobility enhancement and the thermally activated electron trapping, which is the reason why the nonsaturation becomes more prominent as the IGZO active thin film becomes thinner. Furthermore, it is found that the rate of the increased I_{DS} per increasing V_{DS} gets higher as either the channel width (W) increases or the channel length (L) decreases; whereas, the rate of the decreased I_{DS} per increasing V_{DS} becomes higher as the device size, i.e., $W \times L$, increases. The former is well correlated with Joule heating while the latter with the self-heating-assisted electron trapping due to a total heat accumulated in an active layer.**

***Index Terms*— Amorphous indium–gallium–zinc–oxide (a-IGZO), charge trapping, nonsaturated current, output characteristic, self-heating, thin-film transistor.**

I. Introduction

THIN-FILM transistors (TFTs) with channel layer made from amorphous indium–gallium–zinc–oxide (a-IGZO) have been actively researched and begun to be commercialized as the switching/current-driving devices for large-area, high frame-rate display backplanes of active-matrix liquid crystal displays and active-matrix organic light-emitting diodes because they have good electrical and optical characteristics, such as high mobility, large-area uniformity, transparency in the visible light range, low-temperature/cost fabrication processing, and compatibility with flexible substrates [1]. Moreover, a-IGZO TFTs have also been employed very recently in the sensor-embedded flexible circuits for wearable healthcare and Internet-of-Things applications [2], [3], in which the IGZO TFTs were used not only in the digital logic gates but also used as the analog amplifiers. Therefore, a robust current saturation in output characteristics of IGZO TFTs becomes more important in terms of performance and reliability of the a-IGZO analog circuitry. However, up to now, the reliability of IGZO TFTs has been evaluated mainly through their transfer characteristics, such as threshold voltage (V_T) and subthreshold slope (SS), rather than output characteristics [4], [5]. Reliability of output characteristics has been rarely investigated compared with its importance.

In this paper, the degradation on the current saturation of the output characteristic of the a-IGZO TFT with the bottom-gate structure is investigated with varying either the thickness of a-IGZO active film or the device size. A large device size is used to exclude short-channel or narrow-width effects. The nonsaturated current is found to result from the Joule heating-assisted mobility enhancement followed by the self-heating-assisted electron trapping into the gate insulator (GI) and/or interface.

II. Experiment

A schematic of the fabricated a-IGZO TFT with a bottom-gate structure is illustrated in Fig. 1(a). The TFTs were fabricated on highly doped p-type silicon substrates with thermally grown SiO_2 layers. The highly doped p-type silicon and SiO_2 acted as the gate electrode and GI, respectively, with the GI thickness (T_{ox}) = 50 nm. The a-IGZO layer was then RF sputter-deposited in an Ar/O_2 mixture (3/0.1 sccm) at room temperature. In this process, the active-layer thickness (T_{act}) was designed from 15 to 100 nm in order to investigate the effect of IGZO film thickness [see insets of Fig. 1(c) and (d)]. Before depositing the source/drain (S/D) electrode, the device was treated with Ar plasma (150 W, 0.1 torr) to improve

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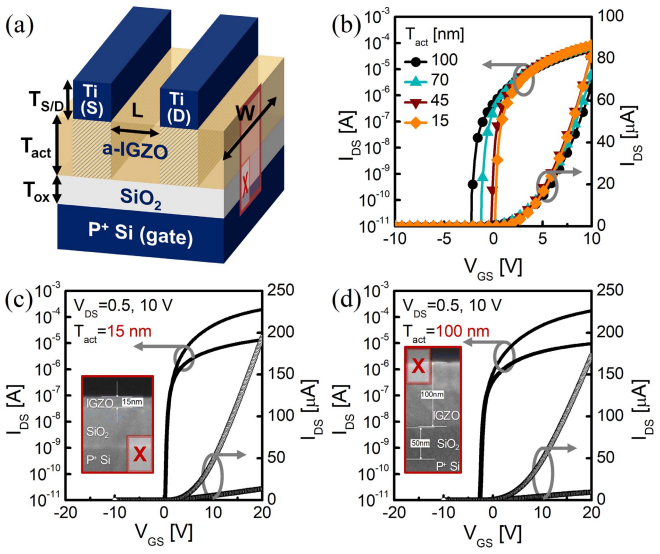

Fig. 1. (a) Schematic 3-D view of the fabricated a-IGZO TFTs with an inverted staggered bottom-gate structure. (b) I_{DS}–V_{GS} transfer characteristics at V_{DS} = 10 V with various T_{act}s. The I_{DS}–V_{GS} transfer characteristics of (c) thin-active device with T_{act} = 15 nm and (d) thick-active device with T_{act} = 100 nm. Insets: cross-sectional scanning electron microscope images of deposited a-IGZO film on the thermally grown SiO_2. T_{ox} = 50 nm and $T_{S/D}$ = 80 nm.

its performance [6]. Then, a Ti layer was deposited with an electron-beam evaporator and was patterned to form the S/D electrode with the thickness of S/D electrodes $T_{S/D}$ = 80 nm. Finally, the samples were annealed at 523 K for 1 h to improve their electrical properties.

The channel width (W) and length (L) were 200 and 100 μm, respectively. The dc current–voltage (I–V) and pulsed I–V characteristics were measured at room temperature under dark ambient using an Agilent 4156C precision semiconductor parameter analyzer and a Keithley 4200 system, respectively. A technology computer-aided design (TCAD) simulation was carried out by using Atlas 2-D of Silvaco.

III. Results and Discussion

The measured transfer characteristics, i.e., the current from drain to source (I_{DS}) versus the applied gate-to-source voltage (V_{GS}) at fixed drain-to-source voltage (V_{DS}) = 10 V, with varying T_{act} are shown in Fig. 1(b). The detailed transfer characteristics at V_{DS} = 0.5 and 10 V are shown in Fig. 1(c) [T_{act} = 15 nm] and Fig. 1(d) [T_{act} = 100 nm], respectively. The parameters of thin devices (T_{act} = 15 nm) are as follows: V_T = 1.22 V, SS = 0.18 V/dec, ON-current (I_{ON}) = 5.08 μA, ON/OFF current ratio (I_{ON}/I_{OFF}) = 1.50 × 10^6, and the field-effect mobility (μ_{FE}) = 9.74 cm^2/Vs, while those of thick devices (T_{act} = 100 nm) are V_T = −1.69 V, SS = 0.27 V/dec, I_{ON} = 4.70 μA, I_{ON}/I_{OFF} = 0.83 × 10^6, and μ_{FE} = 7.80 cm^2/Versus. It is clearly observed that both V_T and I_{ON} increase as the active layer gets thinner, as shown in Fig. 1(b)–(d).

Although these tendencies are consistent with those in [7]–[10], it should be noted that the electrostatic and quantitative explanation of the active thickness dependence of the transfer characteristic was insufficient in most of the previous studies.

In order to explain the case where the process and the material are the same and only T_{act} is different, it is reasonable to assume that the trap density per unit volume of IGZO film is the same regardless of T_{act}. However, a total amount of charged traps in the active layer will be larger if the active layer is thicker. Under the subthreshold regime, a channel layer that is difficult to control by V_{GS} is formed easier especially from the bottom of the active layer as T_{act} becomes thicker. Therefore, the subthreshold current increases under the same V_{GS} as T_{act} gets larger. If T_{act} is large, the total amount of charged traps in the active film is also large, so that the charge for compensating the electric field generated by V_{GS} can be coped enough with localized charge, i.e., a voltage drop occurs across the entire depth direction of the active film, and the accumulation layer (conduction channel) would be formed only thinly on the surface between the IGZO active and GI. Accordingly, the accumulation layer can be formed on the surface of the active layer with a lower V_{GS}. That is, V_T is lowered with the increase of T_{act} as shown in Fig. 1(b)–(d).

On the other hand, in the above-mentioned threshold regime (the ON condition of TFT), the total amount of charged traps in the active layer decreases as the active thickness becomes thinner, so the charge for compensating the electric field generated by V_{GS} must be covered by the accumulated charge by electrons. That is, the thinner the active layer is, the more the accumulation occurs in the active layer. This means that the thickness of the conduction channel in the ON-state becomes rather thick, which means that the channel resistance is lowered [8]. Therefore, as the active layer becomes thinner, I_{ON} increases as shown in Fig. 1(b)–(d). In other word, the surface accumulation condition changes into the volume accumulation condition as the active film gets thinner.

In order to verify the observed T_{act} dependences of V_T, SS, and I_{ON}, the TCAD simulation was carried out as shown in Fig. 2.

The device structure and thermal conductivities of materials used in our simulation are shown in Fig. 2(a) [11]–[14]. The measured T_{act} dependence of transfer characteristic [Fig. 1(b)–(d)] is reproduced well by the device simulation [Fig. 2(b)], which suggests that the electron concentration in channel increases (decreases) at V_{GS} sufficiently above V_T (below V_T) with thinner IGZO film.

The measured I_{DS}–V_{DS} output characteristics at V_{GS} = V_T + 15 V are shown in Fig. 3(a) and (b). While a current saturation is clearly observed at V_{DS} < 20 V [$V_{DS,max}$ = 20 V in Fig. 3(a)], I_{DS} becomes nonsaturated and continues increasing at V_{DS} > 20 V [$V_{DS,max}$ = 40 V in Fig. 3(b)], where $V_{DS,max}$ means the maximum value of swept V_{DS}. In the case of T_{act} = 15 nm, I_{DS} again decreases at V_{DS} > 30 V [Fig. 3(b)]. The T_{act}-dependent nonsaturated current observed is schematically illustrated in Fig. 3(c), where the region of I_{DS} increase and I_{DS} decrease is symbolized by I and II, respectively.

In order to figure out the origin of the nonsaturated I_{DS} and its T_{act} dependence, the output curve of thin device

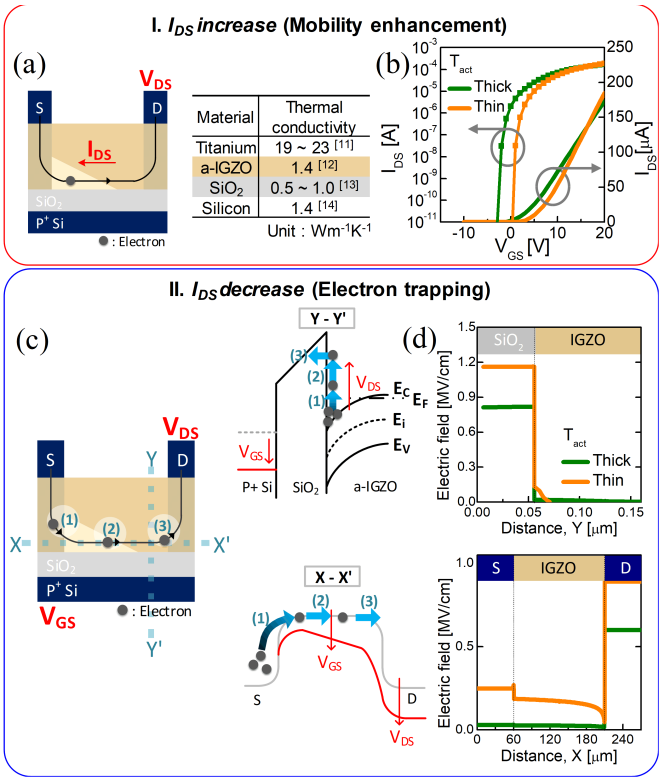

Fig. 2. (a) Schematics illustrating the device structure and thermal conductivities [11]–[14] used in TCAD simulation. (b) Simulated transfer characteristics. (c) Schematic views of vertical and lateral energy band diagrams with indicating the position along the current path. (d) Simulated vertical and lateral distribution of electric field. The electric field increases with thinner T_{act}.

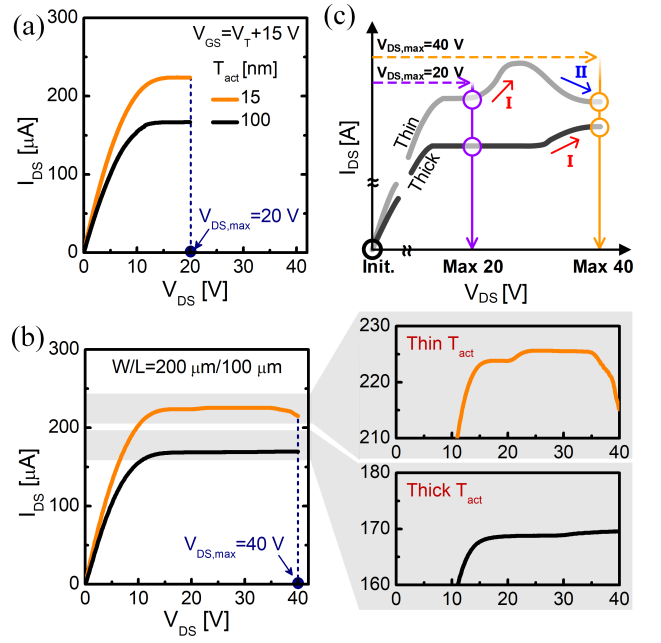

Fig. 3. Measured output characteristics of a-IGZO TFTs with different T_{act}s in the V_{DS} sweep range. (a) From 0 to 20 V ($V_{DS,max} = 20$ V) and (b) from 0 to 40 V ($V_{DS,max} = 40$ V) with $V_{GS} = V_T + 15$ V. (c) Schematic illustrating the T_{act}-dependent output characteristic of a-IGZO TFT.

($T_{act} = 15$ nm) is measured in the pulsed I–V mode, as shown in Fig. 4, with varying the conditions of V_{DS} pulse applied at a fixed $V_{GS} = V_T + 15$ V. The conditions of V_{DS} pulse, such as

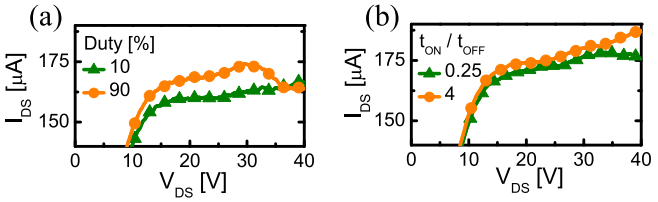

Fig. 4. Measured pulsed I_{DS}–V_{DS} characteristic of thin devices with variations of (a) duty and (b) t_{ON}/t_{OFF} of V_{DS} pulse.

TABLE I
MEASUREMENT CONDITION OF PULSED I–V WITH VARIATION OF DUTY

Parameter	Value		Unit
Duty	10	90	%
Period	1.0		
On time (t_{ON})	0.1	0.9	ms
Off time (t_{OFF})	0.9	0.1	

TABLE II
MEASUREMENT CONDITION OF PULSED I–V WITH VARIATION OF t_{ON}/t_{OFF}

Parameter	Value		Unit
t_{ON} / t_{OFF}	4	0.25	
Period	2.5	2.5	
On time (t_{ON})	2.0	0.5	ms
Off time (t_{OFF})	0.5	2.0	

the duty, ON-time (t_{ON}), and OFF-time (t_{OFF}), are controlled as summarized in Tables I and II. They are intended for modulating the extent to which a self-heating or Joule heating occurs because the device would be heated (cooled down) during t_{ON} (t_{OFF}). Note that the time scale of each V_{DS} step on the order of magnitude of milliseconds is the enough heating time [15], whereas the heat in IGZO film accumulated during the current-flowing period cannot be efficiently dissipated out of active film due to relatively low thermal conductivities of IGZO and SiO_2 as shown in Fig. 2(a) [12], [13].

It is clearly observed in Fig. 4(a) that the degradation on I_{DS} saturation in output characteristic gains prominence as the duty increases. This suggests that the nonsaturated I_{DS}, i.e., the I_{DS} increase followed by the I_{DS} decrease, is attributed to the self-heating because it becomes more significant with the reduction of time for heat release (higher duty). On the other hand, the I_{DS} increase dominates at longer t_{ON} and the I_{DS} decrease becomes more activated at longer t_{OFF} [see Fig. 4(b)]. The temperature in the channel is greatly increased because of the longer heat generation time; while in the latter case, the temperature change is relatively small since there is sufficient time to release the heat.

Therefore, the I_{DS} increase at high V_{DS} [indicated by I in Fig. 3(c)] originates from self-heating in the IGZO active layer. Self-heating not only enhances the carrier mobility in the trap-limited conduction regime but lowers V_T as well [16]–[18], which results in the I_{DS} increase. Our explanation is validated in a TCAD-based device simulation as shown in Fig. 2(b). In the simulation results, the higher I_{DS} of the thin device is consistent with more significant self-heating and reproduces more activated I_{DS} increase compared with that of the thick device [Fig. 3(c)].

On the other hand, when the electrons gain sufficient kinetic energy, they inject into the GI as illustrated in Fig. 2(c). This injection by thermionic field emission and Fowler–Nordheim tunneling occurs especially around the drain, along the path (1) → (2) → (3) in Fig. 2(c), and the trapped electrons increase V_T and consequently decrease I_{DS} as V_{DS} increases. Thus, as V_{DS} increases further, the consecutive I_{DS} decrease [indicated by II in Fig. 3(c)] is observed because electrons become trapped in the GI and/or interface. The simulation results in Fig. 2(d) suggest that the vertical and/or lateral electric field becomes higher and the electrons gain more kinetic energy in the thin device than in the thick device. Therefore, the electron trapping, i.e., the I_{DS} decrease, would begin to dominantly occur at lower V_{DS} as the IGZO active layer becomes thinner [see Fig. 3(b) and (c)].

More in detail, among four t_{ON}/t_{OFF} conditions such as 0.1/0.9, 0.9/0.1, 2/0.5, and 0.5/2 ms, the critical V_{DS}, i.e., $V_{DS,crt}$ (the V_{DS} value at which the current ceases to saturate and begins to rise) is ~20 V ($t_{ON}/t_{OFF} = 0.9/0.1$ ms), ~23 V ($t_{ON}/t_{OFF} = 2/0.5$ ms), and ~27 V ($t_{ON}/t_{OFF} = 0.1/0.9$ and/or 0.5/2 ms) as shown in Fig. 4. Here, the I_{DS} decrease is prominently observed at $V_{DS} < 40$ V only when $t_{ON}/t_{OFF} = 0.9/0.1$ ms while the I_{DS} decrease is not observed at $V_{DS} < 40$ V only when $t_{ON}/t_{OFF} = 2/0.5$ ms. Compared with cases of $t_{ON}/t_{OFF} = 0.9/0.1$ and 2/0.5 ms, the extent to which I_{DS} becomes nonsaturated is relatively weak in cases of $t_{ON}/t_{OFF} = 0.1/0.9$ and 0.5/2 ms. In addition, the I_{DS} decrease occurs very weakly when $t_{ON}/t_{OFF} = 0.5/2$ ms.

Therefore, at $t_{ON} > t_{OFF}$, the longer t_{ON} is compared to t_{OFF}, the current ceases to saturate and starts to rise at the lower V_{DS} ($V_{DS,crt}$ becomes lower). Also, as the I_{DS} increase begins at the lower V_{DS}, the I_{DS} decrease begins again at the lower V_{DS} value. This means that the larger the degrees of mobility enhancement and V_T lowering are, the more active the charge trapping phenomenon is. This is evidence that charge trapping is also related to self-heating. In addition, $V_{DS,crt}$ decreases sensitively as the t_{ON}/t_{OFF} ratio increases.

On the other hand, when $t_{ON} < t_{OFF}$, the degradation of current saturation is relatively less. That is, $V_{DS,crt}$ further increases. In the case of $t_{ON} < t_{OFF}$, compared with $t_{ON} > t_{OFF}$, the I_{DS} increase is weak, the I_{DS} decrease is also weak, and $V_{DS,crt}$ is relatively insensitive to the t_{ON}/t_{OFF} ratio. Furthermore, the longer the duration of t_{ON} is, the I_{DS} decrease due to charge trapping is observed at the lower V_{DS}.

In Figs. 3 and 4, we emphasize that charge trapping can be accelerated by the self-heating associated with thermionic-field emission [19], [20]. As a result, in a structure with a high current flow, heat generation due to power consumption is enhanced, and thereby, electron trapping is promoted.

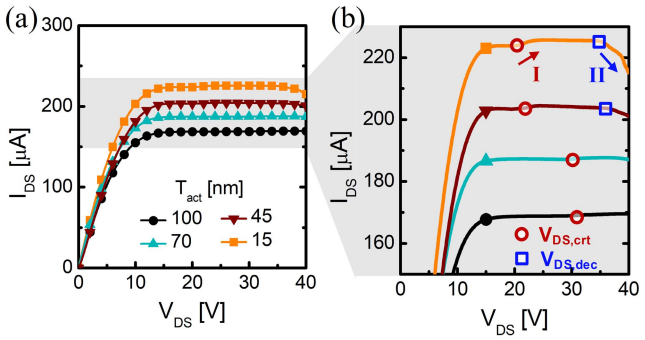

Fig. 5. (a) Measured output characteristics of a-IGZO TFTs with different T_{act}s at $V_{GS} = V_T + 15$ V. (b) Changes of $V_{DS,crt}$ and $V_{DS,dec}$ with the variation of T_{act}.

In order to investigate the active thickness dependence of the current saturation degradation more in detail, both $V_{DS,crt}$ and $V_{DS,dec}$, i.e., the V_{DS} value at which the current begins to decrease in region II, are taken for the cases of $T_{act} = 15$, 45, 70, and 100 nm as shown in Fig. 5. The parameters are as follows: $V_{DS,crt} = 20.4$ V ($T_{act} = 15$ nm), 21.4 V ($T_{act} = 45$ nm), 29.8 V ($T_{act} = 70$ nm), and 30.4 V ($T_{act} = 100$ nm), $V_{DS,dec} = 35$ V ($T_{act} = 15$ nm), and 35.7 V ($T_{act} = 45$ nm), respectively. These results suggest that our explanation of the T_{act} dependence of current saturation degradation is reasonable and reproducible.

In addition, in order to determine whether the electron trapping happens locally near the drain region, we switch the location of S/D to each other after sweeping V_{DS} up to $V_{DS,max}$. In the transfer characteristics shown in Fig. 6(a) and (b), the forward mode means the same S/D location as that when sweeping V_{DS} up to $V_{DS,max}$, whereas the reverse mode corresponds to switching the location of S/D to each other compared with the forward mode. We also confirm the transfer characteristics in the linear and saturation regions by reading out I_{DS} by setting the constant V_{DS} to 0.5 and 10 V. In the thin device, V_T shifts in the positive direction when $V_{DS,max} = 40$ V (max 40), but remains unchanged compared with the initial (Init.) V_T when $V_{DS,max} = 20$ V (max 20) [Fig. 6(c)]. Therefore, it is certain that the I_{DS} decrease in output characteristic results from the electron trapping followed by the V_T increase. Furthermore, it is noteworthy that V_T slightly increases only when the forward mode is carried out at $V_{DS} = 10$ V [Fig. 6(c)]. This suggests that the electrons are locally trapped in GI near the drain rather than the source, as illustrated by energy band diagram with different energy barriers in Fig. 6(e). Among the read-out conditions, the energy barrier is lowered only under the condition of $V_{DS} = 10$ V in the forward mode, resulting in a relatively small V_T compared to others. In contrast, V_T lowers with increasing $V_{DS,max}$ in the thick device, as shown in Fig. 6(d). It validates that self-heating followed by V_T lowering causes the abnormal I_{DS} increase in the output characteristic [16].

In order to investigate the influence of device size on the degradation of current saturation, the output curves are also measured with varying W and L, as shown in Fig. 7(a).

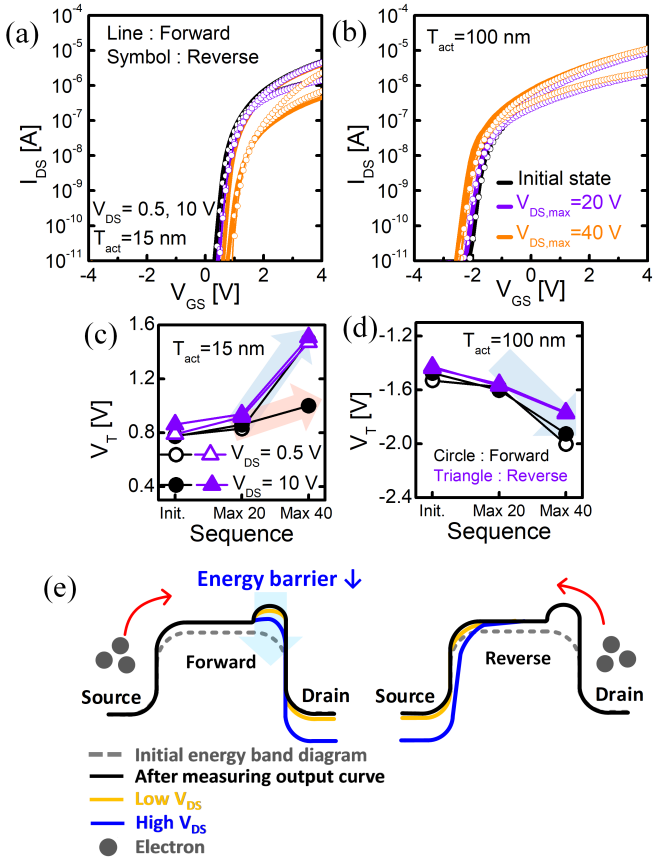

Fig. 6. Measured transfer characteristics of the forward and reverse modes at initial state and after observing output characteristics with conditions of Fig. 3 of (a) thin and (b) thick devices. (c) V_T taken from (a) in the thin device. (d) V_T taken from (b) in the thick device. (e) Schematics illustrating the lateral electric potential profiles according to read-out mode, i.e., forward and reverse.

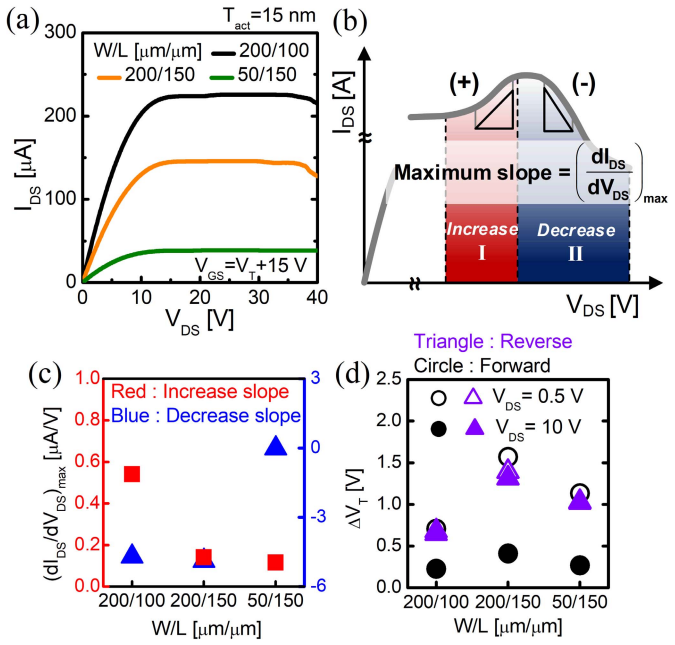

Fig. 7. (a) Device size dependence of the output characteristics. (b) Enlarged schematic describing the defined parameter $(dI_{DS}/dV_{DS})_{max}$. (c) Extracted $(dI_{DS}/dV_{DS})_{max}$ from the output characteristics shown in (a). (d) ΔV_T taken from the read-out transfer curves at initial state and after sweeping output curve in devices with different sizes (W/L).

The slopes (dI_{DS}/dV_{DS}) are extracted from the output characteristics to indicate the extent to which the nonsaturated current phenomena happen and the maximum value among their magnitudes, i.e., $(dI_{DS}/dV_{DS})_{max}$, is taken in the I_{DS} decrease (II) as well as the I_{DS} increase (I) regions, respectively, as seen in Fig. 7(b). Extracted $(dI_{DS}/dV_{DS})_{max}$ is summarized as the functions of W and L, as shown in Fig. 7(c). $(dI_{DS}/dV_{DS})_{max}$ in region I becomes larger as either W increases or L decreases. This suggests that the I_{DS} increase in output characteristics is observed more prominently as I_{DS} itself increases, which is strongly reminiscent of Joule heating.

On the other hand, $(dI_{DS}/dV_{DS})_{max}$ in region II becomes larger as the device size, i.e., $W \times L$, increases, which is strongly correlated with self-heating-assisted electron trapping because a total heat accumulated in an active layer with low thermal conductivity increases with increasing the device size [12], [19]. The W and L dependences of the V_T shift (ΔV_T) after read-out of the output characteristics at $V_{DS,max} = 40$ V are also shown in Fig. 7(d). ΔV_T is the largest at the case of maximum $W \times L$ value, which suggests ΔV_T is also correlated with self-heating.

In Fig. 7(c), it is noteworthy that the case of $W \times L = 50 \times 150$ μm^2 is not applicable to the discussion on the device size dependence of $(dI_{DS}/dV_{DS})_{max}$ in region II because in the case of device with $W/L = 50/150$ μm, any I_{DS} decrease is not observed after read-out of the output characteristics at $V_{DS,max} = 40$ V, i.e., $(dI_{DS}/dV_{DS})_{max}$ in region II ~ 0.

Furthermore, in Fig. 7(d), it is clearly observed that ΔV_T after read-out of the output characteristics at $V_{DS,max} = 40$ V is the largest in $W/L = 200/150$ μm among $W/L = 200/100$, 200/150, and 50/150 μm. ΔV_T in $W/L = 200/150$ μm is larger than that in $W/L = 200/100$ μm although I_{ON} is lower in $W/L = 200/150$ μm than that in $W/L = 200/100$ μm, which suggests that the $W \times L$ value as well as W/L value affects ΔV_T.

In order for the I_{DS} increase (negative ΔV_T) to occur, and then the I_{DS} decrease (positive ΔV_T) to be observed, it is necessary to compensate the mobility enhancement and V_T lowering by the charge trapping. However, since the device with $W/L = 50/150$ μm has little I_{DS} increase itself, there is no negative ΔV_T to compensate. Therefore, the larger ΔV_T in $W/L = 50/150$ μm than that in $W/L = 200/100$ μm can be observed, as shown in Fig. 7(d).

Finally, it needs to be discussed whether a different active layer thickness would have a possibility to cause the heat dissipation difference. If I_{ON} is independent of the active thickness T_{act}, a total heat generated in an active film can be roughly proportional to a total volume of active film, i.e., $W \times L \times T_{act}$. This total volume would strongly affect the heat dissipation. However, as mentioned earlier, I_{ON} increases as T_{act} becomes thinner. Thus, the self-heating definitely becomes more prominent as T_{act} becomes thinner, which makes the T_{act} aspect simpler. It should be noted that from the viewpoint of T_{act}, the self-heating is dominated by a

high I_{ON} rather than by the surface area or the volume of heat dissipation.

If I_{ON} decreases as T_{act} becomes thinner, the thickness aspect may become very complicated because the Joule heating and the heat dissipation will move in an opposite direction. However, it is not our case. Quantitative analysis is necessary as further study.

Consequently, the factors that determine nonsaturation in output characteristics are largely related to the dimensions of the device structure, which affect the current, the area in which heat is generated, and the electric field. These comprehensive measured and simulation results support two mechanisms on the nonsaturated current in output characteristics of IGZO TFTs under high current flowing conditions and their dependence on the dimensions. The first mechanism is Joule heating followed by V_T lowering and mobility enhancement, and the second is self-heating-assisted (thermionic field emission and Fowler–Nordheim tunneling) electron trapping in the GI near the drain region followed by V_T increase.

IV. Conclusion

Degradation on the current saturation in output characteristics in IGZO TFTs is observed and its origins are experimentally analyzed and verified by TCAD simulation. The influence of IGZO active thickness on this nonsaturation is also investigated. I_{DS} becomes nonsaturated and gradually increases at a high V_{DS} and then decreases at a higher V_{DS} when the output curve is measured. I_{DS} increases due to Joule-heating followed by V_T lowering and mobility enhancement, which gains prominence as the active layer becomes thinner. These phenomena were also more activated as either W increases or L decreases. In addition, the I_{DS} decrease results from the self-heating-assisted electron trapping into GI near the drain region followed by V_T increase and gains significance as the active layer becomes thinner and as the device size, i.e., $W \times L$, increases.

Our results suggest that the nonsaturated output characteristics and their related mechanisms need to be carefully considered as main reliability issues when designing analog circuitry or high-current driving applications based on IGZO TFTs where a robust current saturation and large output resistance are critical.

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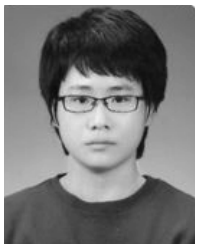

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