Influence of the Gate/Drain Voltage Configuration on the Current Stress Instability in Amorphous Indium-Zinc-Oxide Thin-Film Transistors With Self-Aligned Top-Gate Structure

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***Abstract*— The influence of V_{GS}/V_{DS} condition on the current stress (CS) instability in amorphous InZnO thin-film transistors (TFTs) with the self-aligned top-gate structure is comprehensively analyzed and quantitatively validated by consolidating: 1) the *I–V* and *C–V* characteristics; 2) the extraction of density of states; 3) the decomposition of threshold voltage shift (ΔV_T); and 4) the computer-aided design simulation. It has been found that in a high V_{GS} and low V_{DS} CS condition, electron trapping into the gate insulator globally occurs. However, these effects are combined with a local electron trapping into gate insulator in the source region and the generated peroxide defects in the drain region under a high V_{DS} and low V_{GS} CS condition. The peroxide formation that is followed by the donor generation is clearly distinguished by the activation energy of 0.49 eV from the oxygen vacancies ionization which has been widely modeled for explaining the donor creation in amorphous oxide semiconductor TFTs.**

***Index Terms*— InZnO thin-film transistor, current stress (CS), density-of-state, amorphous oxide semiconductor.**

I. Introduction

AMORPHOUS oxide semiconductor (AOS) materials have attracted much attention due to their potential application in high-resolution large-area displays which make use of thin-film transistors (TFTs) [1]. The commercialization of the AOS TFT-driven active-matrix organic light-emitting diode (AMOLED) display has been recently accelerated, especially for devices with the self-aligned top-gate structure. This is due to the high mobility, low source/drain (S/D) resistance, and low parasitic capacitance this technology offers [2]–[5]. However, current stress instability under practical operating conditions remains a central challenge in the mass production of AOS TFT-driven AMOLED displays. To address this problem, it is necessary to optimize the gate-to-source voltage (V_{GS}) and the drain-to-source voltage (V_{DS}), during the design process of high performance and high reliability of AMOLED pixels [6]. However, the quantitative analysis of the mechanism and the modeling of the influence of the V_{GS}/V_{DS} configuration on the instabilities of AOS TFTs with self-aligned top-gate structure have not been reported in the semiconductor materials literature.

In this work, the effect of the V_{GS}/V_{DS} configuration on the current stress (CS)-induced instability in the amorphous indium-zinc-oxide (a-IZO) TFTs with the self-aligned top-gate structure is investigated and modeled. The relevant mechanisms are figured out by considering two different V_{GS}/V_{DS} conditions; the saturation operating condition of V_{GS}/V_{DS} = 10 V/30 V, i.e., higher V_{DS} than V_{GS} (*HVDS*), and the linear operating condition of V_{GS}/V_{DS} = 30 V/10 V, i.e., higher V_{GS} than V_{DS} (*HVGS*). Quantitative modeling was carried out using technology computer-aided design simulations(TCAD).

II. Experimental Procedure

The fabrication of TFT devices with self-aligned top-gate structure was conducted by depositing a 50-nm-thick a-IZO active layer on a glass substrate, using the radio frequency magnetron sputtering process. Subsequently, a 100-nm-thick SiO_2 acting as the gate insulator (GI) was deposited using plasma-enhanced chemical vapor deposition (PECVD). A 100-nm-thick layer of molybdenum (Mo) acting as the gate electrode was sequentially sputtered at room temperature. These two layers were continuously dry-etched using a gate pattern. This process was followed by the Ar plasma treatment to form the S/D n^+ regions of the active layer. Next, a 200-nm-thick a-SiO2 interlayer dielectric was deposited by PECVD. Subsequently, a 200-nm-thick layer of Mo acting as the S/D metal was sputtered at room temperature and then patterned by dry etching. Finally, the TFT devices were subjected to thermal annealing at 250 °C for 1 h. The fabricated device is schematically illustrated in the inset of Fig. 1(b). The channel width (W) and length (L) are 40 μm and 40 μm.

Manuscript received June 7, 2019; revised June 30, 2019; accepted July 4, 2019. Date of publication July 8, 2019; date of current version August 23, 2019. This work was supported in part by the National Research Foundation of Korea (NRF) through the Korean Government, Ministry of Education, Science and Technology (MEST), under Grant 2016R1A5A1012966, Grant 2017R1A2B4006982, Grant 18ZB1800, and Grant 2016M3A7B4909668, in part Silvaco, and in part by the IC Design Education Center (IDEC). The review of this letter was arranged by Editor A. V. Y. Thean. *(Corresponding author: Dae Hwan Kim.)*

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Digital Object Identifier 10.1109/LED.2019.2927378

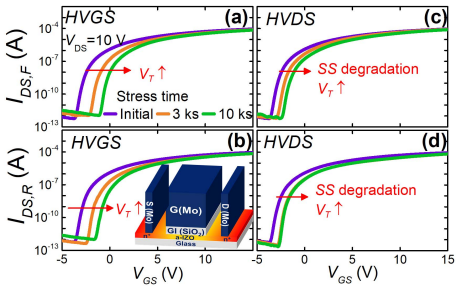

Fig. 1. Measured transfer characteristics of the a-IZO TFTs under (a) forward and (b) reverse V_{DS} modes in *HVGS* and under (c) forward and (d) reverse V_{DS} modes in *HVDS* condition. The inset in (b) is a schematic illustration of the fabricated a-IZO TFTs structure.

III. Results and Discussion

Figs. 1(a)-(d) show the measured transfer curves of a-IZO TFTs at $V_{DS} = 10$ V during the CS time (t_{str}) up to 10^4 s under the *HVGS* and *HVDS* conditions. In the curves, $I_{DS,F}$ is the drain-to-source current, measured under forward V_{DS} mode (the drain and source positions are identical to the CS positions) in read-out condition, while $I_{DS,R}$ is the drain-to-source current, measured under reverse V_{DS} mode (the drain and source positions are interchanged with respect to the CS positions). The threshold voltage (V_T) was defined as the value of V_{GS} that induces $I_{DS} = 10$ nA at $V_{DS} = 10$ V and the sub-threshold swing (*SS*) was measured from $I_{DS} = 1$ nA to 10 nA in the sub-threshold region.

Under CS, the positive V_T shift (ΔV_T) is observed in all cases shown in Fig. 1. It is evident from Figs. 1(a) and (b), that in the case of *HVGS*, the ΔV_T in forward V_{DS} mode ($\Delta V_{T,F}$) is analogous to that in the reverse V_{DS} mode ($\Delta V_{T,R}$) as t_{str} increases, while the *SS* is nearly unchanged. However, in the case of *HVDS*, $\Delta V_{T,F}$ and $\Delta V_{T,R}$ behave differently and a significant degradation of the *SS* is observed [Figs. 1(c)-(d)]. This result implies that the local ΔV_T values near source and drain are evolved differently during CS and the traps are generated near the conduction band minimum level (E_C), especially in the *HVDS* condition.

For more detailed analysis, the small signal *C-V* (capacitance-voltage) characteristics between the gate and S/D tied to ground, i.e., C_{G-DS}-V_G, are measured as shown in Figs. 2(a) and (b). Under the *HVDS* [Fig. 2(b)], the *C-V* slope decreases with a positive ΔV_T, while the turn-on voltage of C_{G-DS} decreases during CS compared to the initial state [reference point A in Figs. 2(c) and (d)]. This suggests that a negative ΔV_T mechanism occurs locally in the drain region which is denoted by the blue box in Fig 2(d) [7], [8]. In general, the origin of negative ΔV_T may be due to either hole trapping into GI or donor generation. In our case, a local negative ΔV_T during CS is attributed to donor generation since the holes have short life-time and low mobility in a-IZO TFTs [9]. Thus, as indicated in Fig. 2(d), the CS-induced positive/negative ΔV_T near S/D, individually results from the electron trapping into GI (symbolized by the trapping length L_{trap}) / the donor generation (denoted by the length of donor generation region L_{DG}), respectively. In Figs. 2(c) and (d), point B shows that the source region with L_{trap} is turned on at $V_G = V_B$ while the channel region becomes totally conducting at $V_G = V_C$.

The direct evidence of the CS instability was experimentally verified, by extracting the subgap density-of-state (*DOS*) (shown in Fig. 3) using the multi-frequency method [10].

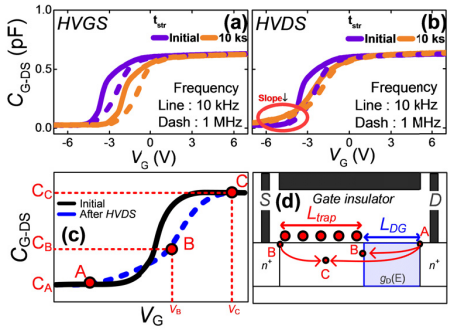

Fig. 2. (a) t_{str}-dependent C_{GDS}-V_G during (a) the *HVGS* and (b) the *HVDS*. Scheme of (c) the *C-V* curve under *HVDS* and (d) the spatial evolution of the TFT conducting channel during the *HVDS* depending on the V_G-dependent C_{G-DS} characteristic.

The energy distribution of the AOS *DOS* is described by the following equation models [6], [10]:

$$g_A(E) = g_{TA}(E) + g_{DA}(E) = N_{TA} \times \exp\left(\frac{E - E_C}{kT_{TA}}\right) + N_{DA} \times \exp\left(\frac{E - E_C}{kT_{DA}}\right) \quad (1)$$

$$g_D(E) = g_{TD}(E) + g_{SD}(E) = N_{TD} \times \exp\left(\frac{E_V - E}{kT_{TD}}\right) + N_{SD} \times \exp\left(-\left(\frac{(E_V - E) + E_{SD}}{kT_{SD}}\right)^2\right) \quad (2)$$

where the donor-like tail states (g_{TD}) [not shown in Fig. 3], shallow donor states (g_{SD}), acceptor-like tail (g_{TA}) and deep states (g_{DA}) are individually modeled with the parameters of densities/characteristic energies and the Gaussian peak center energy of N_{TD}/kT_{TD}, N_{SD}/kT_{SD}, N_{TA}/kT_{TA}, N_{DA}/kT_{DA}, and E_{SD}. In the *HVGS* condition [Fig. 3(a)], the *DOS* remains unchanged during CS compared to that in the initial state, i.e., $N_{TD} = 1 \times 10^{20}$ cm^{-3}eV^{-1}, $kT_{TD} = 0.15$ eV, $N_{TA} = 1 \times 10^{18}$ cm^{-3}eV^{-1}, $kT_{TA} = 0.04$ eV, $N_{DA} = 2.5 \times 10^{17}$ cm^{-3}eV^{-1}, $kT_{DA} = 0.25$ eV. The change in g_{SD} is negligible (the extracted values of parameters are within the range of those reported in the literature [9], [11], [12]), while $g_{SD}(E)$ noticeably increases to be $N_{SD} = 1.3 \times 10^{17}$ cm^{-3}eV^{-1}, $E_{SD} = E_C - 0.3$ eV, and $kT_{SD} = 0.5$ eV after $t_{str} = 10^4$ s only in the *HVDS* condition [Fig. 3(b)]. This result is consistent with the *HVDS* CS-induced donor generation mentioned above and presented in Figs. 2(c) and (d). The increase of $g_{SD}(E)$ may be associated with excessive oxygen [13], [14], oxygen interstitials [15], ionized oxygen vacancy defects [16], [17], and intrinsic (In*-M) electron-trapped centers [18]. Among them, the increased Gaussian distribution of *DOS* near E_C is usually related to the ionization of oxygen vacancies ($V_o + 2h^+ \rightarrow V_o^{2+}$) or the formation of peroxide defects ($O^{2-} + O^{2-} \rightarrow O_2^{2-} + 2e^-$) [13], [19], [20]. These two phenomena can occur locally near the drain region by self-heating [17], [21], the high electric field [22], and the negative bias stress caused by V_{GD} near the drain side [23].

An experimental decomposition technique [24], can be used for a more quantitative analysis on the influence of the V_{GS}/V_{DS} configuration, the decomposition of a total ΔV_T ($\Delta V_{T,tot}$) into the ΔV_T due to the electron trapping into GI ($\Delta V_{T,GI}$) [illustrated as L_{trap} in Fig. 2(d)] and the ΔV_T resulting from the g_{SD} generation ($\Delta V_{T,SD}$) [denoted by L_{DG} in Fig. 2(d)]. The symbols in Fig. 4, indicate that the only

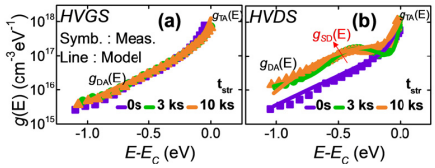

Fig. 3. t_{str}-evolution of DOS under (a) the *HVGS* and (b) the *HVDS*.

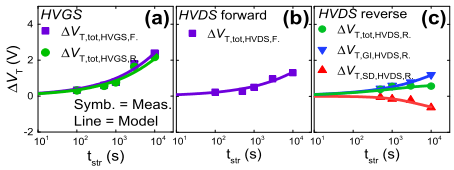

Fig. 4. Decomposed $\Delta V_T(t_{str})$ under (a) the *HVGS*, (b) forward and (c) reverse mode of the *HVDS* (Symbol: measurement and line: MSEF model).

TABLE I
THE MSEF PARAMETERS FOR EACH CS CONDITION

Parameters	*HVGS,F/R*	*HVDS,F*	*HVDS,R*	*HVDS,R*
ΔV_T [V]	Positive			Negative
ΔV_{T0} [V]	30	10	10	−0.7
β	0.4 – 0.5			0.95
τ [s]	$3 \times 10^6 - 6 \times 10^6$			5×10^3
E_a [eV]	0.83 – 0.85			0.49
Mechanism	Charge-trapping into GI			Peroxide defect

$\Delta V_{T,tot,HVDS,R}$ should be decomposed into $\Delta V_{T,GI,HVDS,R}$ and $\Delta V_{T,SD,HVDS,R}$, whereas the only $\Delta V_{T,GI}$ contributes to $\Delta V_{T,tot}$ in all cases of $\Delta V_{T,tot,HVGS,F}$, $\Delta V_{T,tot,HVGS,R}$, and $\Delta V_{T,tot,HVDS,F}$. Here, the complicated subscripts identify the $\Delta V_{T,tot}/\Delta V_{T,tot}/\Delta V_{T,tot}$, the CS type of *HVGS/HVDS*, and $\Delta V_{T,F}/\Delta V_{T,R}$, respectively. Consistently with the donor generation locally near the drain, it is noteworthy that the $\Delta V_{T,SD}$ is observed only in $\Delta V_{T,tot,HVDS,R}$.

The mechanism on the donor generation under the *HVDS* CS can be elucidated, by fitting the experimentally decomposed $\Delta V_{T,tot}(t_{str})$ with the multiple stretched-exponential functions (MSEFs) [lines in Fig. 4(c)], as follows [26]:

$$\Delta V_{T,tot}(t) = \Delta V_{T0,SD}\left[1-\exp\left(-\left(\frac{t}{\tau_{SD}}\right)^{\beta_{SD}}\right)\right] + \Delta V_{T0,GI}\left[1-\exp\left(-\left(\frac{t}{\tau_{GI}}\right)^{\beta_{GI}}\right)\right] \quad (3)$$

where ΔV_{T0} is ΔV_T at infinite time, τ is the characteristic time constant, and β is the stretching exponent. Then, $\Delta V_{T,SD}$ is the negative component of ΔV_T caused by the creation of shallow donor states, while $\Delta V_{T,GI}$ is the positive component of ΔV_T caused by the charge-trapping in the GI (because the $\Delta V_{T0,GI}$ has a positive value). The lines in Fig. 4 and Table I show that all of $\Delta V_{T,tot}$, $\Delta V_{T,GI}$, and $\Delta V_{T,SD}$ are well fitted with the MSEFs using individually selected parameters.

Furthermore, the effective energy barrier, i.e., the activation energy (E_a) corresponding to the respective physical mechanism, can be extracted by using the Laplace transform method [27] (data not shown). In Table I, the values of E_a are found to be 0.83, 0.83, 0.85, 0.85, and 0.49 eV corresponding to $\Delta V_{T,tot,HVGS,F}$, $\Delta V_{T,tot,HVGS,R}$, $\Delta V_{T,tot,HVDS,F}$, $\Delta V_{T,GI,HVGS,R}$, and $\Delta V_{T,SD,HVGS,R}$, respectively. The values of $E_{a,GI}$'s = 0.83 – 0.85 eV are in good agreement with

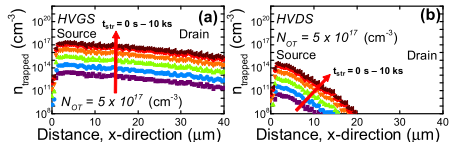

Fig. 5. Simulated $n_{trapped}$ during (a) the *HVGS* and (b) the *HVDS*.

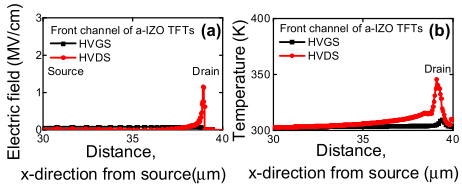

Fig. 6. Simulated distribution of (a) electric field and (b) temperature under CS.

the E_a values reported in studies which have considered the charge-trapping in the GI as the dominant mechanism on ΔV_T. These observed E_a values ranged from 0.60 to 1.33 eV [25], [27], [28]. On the other hand, it is noteworthy that the value of $E_{a,SD}$ = 0.49 eV extracted at negative ΔV_T under the *HVDS* condition coincides with the E_a value associated with the peroxide defect formation through electron de-trapping ($O^{2-}+O^{2-} \rightarrow O_2^{2-}+2e^-$). This E_a value has been calculated to be 0.46 eV [29]. The extracted $E_{a,SD}$ = 0.49 eV does not match the E_a value for the reaction of ionized oxygen vacancies ($V_o + 2h^+ \rightarrow V_o^{2+}$, E_a = 0.88 – 0.97 eV) [30]. Therefore, the donor generation under the *HVDS* CS condition is attributed to the formation of peroxide defects rather than the ionization of oxygen vacancies.

The Atlas-2D TCAD software [31] was used to simulate the local charge-trapping model and the change in the *DOS*, in order to thoroughly verify this physical behavior. The simulations were incorporated into by physical models, a transient charge-trapping model, the GI trap model, F-N tunneling, band-to-band tunneling, trap-assisted tunneling, and hot-carrier injection. The spatial distribution of the density of trapped electrons ($n_{trapped}$) in the GI over CS time at a fixed density of oxide bulk trap ($N_{OT} = 5 \times 10^{17}$ cm^{-3}) is shown in Figs. 5(a) and (b). In the *HVGS* case, global charge-trapping occurs throughout the GI as t_{str} increases. However, in the *HVDS* case, $n_{trapped}$ increases locally only in the drain region as t_{str} increases.

Finally, the higher electric field and the temperature of a-IZO TFTs were observed in the drain side, under the *HVDS* condition as shown in Figs. 6(a) and (b). These simulation results verify that the formation of peroxide defects becomes more activated due to a locally higher electric field and temperature in the drain side as V_{DS} becomes higher than V_{GS}, i.e., in the *HVDS* condition.

IV. CONCLUSION

The effect of V_{GS}/V_{DS} configuration on the CS instability in a-IZO TFTs with self-aligned top-gate structure is controlled by the combination of the GI charge trapping and the local formation of peroxide defects. The latter becomes more boosted as the V_{DS} becomes higher than V_{GS}, i.e., *HVDS* rather than *HVGS* due to locally higher electric field and self-heating near the drain edge. Our results provide a guide-line to optimize the bias point of current-driving TFTs with the self-aligned top-gate structure in the AOS-driven AMOLED backplanes.

REFERENCES

[1] M. Nag, F. De Roose, K. Myny, S. Steudel, J. Genoe, G. Groeseneken, and P. Heremans, "Characteristics improvement of top-gate self-aligned amorphous indium gallium zinc oxide thin-film transistors using a dual-gate control," *J. Soc. Inf. Display*, vol. 25, no. 6, pp. 349–355, 2017. doi: 10.1002/jsid.558.

[2] D. H. Kang, I. Kang, S. H. Ryu, and J. Jang, "Self-aligned coplanar a-IGZO TFTs and application to high-speed circuits," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1385–1387, Oct. 2011. doi: 10.1109/LED.2011.2161568.

[3] J. C. Park, H.-N. Lee, and S. Im, "Self-aligned top-gate amorphous indium zinc oxide thin-film transistors exceeding low-temperature poly-Si transistor performance," *ACS Appl. Mater. Interfaces*, vol. 5, no. 15, pp. 6990–6995, 2013. doi: 10.1021/am401128p.

[4] D. Geng, D. H. Kang, M. J. Seok, M. Mativenga, and J. Jang, "High-speed and low-voltage-driven shift register with self-aligned coplanar a-IGZO TFTs," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 1012–1014, Jul. 2012. doi: 10.1109/LED.2012.2194133.

[5] N. Morosawa, M. Nishiyama, Y. Ohshima, A. Sato, Y. Terai, K. Tokunaga, J. Iwasaki, K. Akamatsu, Y. Kanitani, S. Tanaka, T. Arai, and K. Nomoto, "High-mobility self-aligned top-gate oxide TFT for high-resolution AM-OLED," *J. Soc. Inf. Display*, vol. 21, no. 11, pp. 467–473, 2013. doi: 10.1002/jsid.206.

[6] S. Choi, H. Kim, C. Jo, H.-S. Kim, S.-J. Choi, D. M. Kim, J. Park, and D. H. Kim, "The effect of gate and drain fields on the competition between donor-like state creation and local electron trapping in In–Ga–Zn–O thin film transistors under current stress," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1336–1339, Dec. 2015. doi: 10.1109/LED.2015.2487370.

[7] H. Choi, J. Lee, H. Bae, S.-J. Choi, D. H. Kim, and D. M. Kim, "Bias-dependent effective channel length for extraction of subgap DOS by capacitance-voltage characteristics in amorphous semiconductor TFTs," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2689–2694, Jun. 2015. doi: 10.1109/TED.2015.2443492.

[8] D. W. Kwon, J. H. Kim, W. Kim, S. W. Kim, J.-H. Lee, and B.-G. Park, "Analysis on trapping kinetics of stress-induced trapped holes in gate dielectric of amorphous HfInZnO TFT," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2398–2404, Jun. 2016. doi: 10.1109/TED.2016.2555332.

[9] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous In–Ga–Zn–O thin-film transistors," *Sci. Technol. Adv. Mater.*, vol. 11, no. 4, Feb. 2010, Art. no. 044305. doi: 10.1088/1468-6996/11/4/044305.

[10] S. Lee, S. Park, S. Kim, Y. Jeon, K. Jeon, J.-H. Park, J. Park, I. Song, C. J. Kim, Y. Park, D. M. Kim, and D. H. Kim, "Extraction of subgap density of states in amorphous InGaZnO thin-film transistors by using multifrequency capacitance–voltage characteristics," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 231–233, Mar. 2010. doi: 10.1109/LED.2009.2039634.

[11] M. Bae, D. Yun, Y. Kim, D. Kong, H. K. Jeong, W. Kim, J. Kim, I. Hur, D. H. Kim, and D. M. Kim, "Differential ideality factor technique for extraction of subgap density of states in amorphous InGaZnO thin-film transistors," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 399–401, Mar. 2012. doi: 10.1109/LED.2011.2182602.

[12] E. K.-H. Yu, S. Jun, D. H. Kim, and J. Kanicki, "Density of states of amorphous In-Ga-Zn-O from electrical and optical characterization," *J. Appl. Phys.*, vol. 116, no. 15, 2014, Art. no. 154505. doi: 10.1063/1.4898567.

[13] H.-H. Nahm, Y.-S. Kim, and D. H. Kim, "Instability of amorphous oxide semiconductors via carrier-mediated structural transition between disorder and peroxide state," *Phys. Status Solidi B*, vol. 249, no. 6, pp. 1277–1281, 2012. doi: 10.1002/pssb.201147557.

[14] K. Ide, Y. Kikuchi, K. Nomura, M. Kimura, T. Kamiya, and H. Hosono, "Effects of excess oxygen on operation characteristics of amorphous In-Ga-Zn-O thin-film transistors," *Appl. Phys. Lett.*, vol. 99, no. 9, Sep. 2011, Art. no. 093507. doi: 10.1063/1.3633100.

[15] X. Zhou, Y. Shao, L. Zhang, H. Lu, H. He, D. Han, Y. Wang, and S. Zhang, "Oxygen interstitial creation in a-IGZO thin-film transistors under positive gate-bias stress," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1252–1255, Sep. 2017. doi: 10.1109/LED.2017.2723162.

[16] S. M. Lee, W.-J. Cho, and J. T. Park, "Device instability under high gate and drain biases in InGaZnO thin film transistors," *IEEE Trans. Device Mater. Rel.*, vol. 14, no. 1, pp. 471–476, Mar. 2014. doi: 10.1109/TDMR.2013.2278990.

[17] J. I. Kim, I.-T. Cho, S.-M. Joe, C.-Y. Jeong, D. Lee, H.-I. Kwon, S. H. Jin, and J.-H. Lee, "Effect of temperature and electric field on degradation in amorphous InGaZnO TFTs under positive gate and drain bias stress," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 458–460, Apr. 2014. doi: 10.1109/LED.2014.2306818.

[18] H.-H. Nahm and Y.-S. Kim, "Undercoordinated indium as an intrinsic electron-trap center in amorphous $InGaZnO_4$," *NPG Asia Mater.*, vol. 6, no. 11, p. e143, Nov. 2014. doi: 10.1038/am.2014.103.

[19] J. Yao, N. Xu, S. Deng, J. Chen, J. She, H.-P. D. Shieh, P.-T. Liu, and Y.-P. Huang, "Electrical and photosensitive characteristics of a-IGZO TFTs related to oxygen vacancy," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 1121–1126, Apr. 2011. doi: 10.1109/TED.2011.2105879.

[20] S. Jeon, S.-E. Ahn, I. Song, C. J. Kim, U.-I. Chung, E. Lee, I. Yoo, A. Nathan, S. Lee, K. Ghaffarzadeh, J. Robertson, and K. Kim, "Gated three-terminal device architecture to eliminate persistent photoconductivity in oxide semiconductor photosensor arrays," *Nature Mater.*, vol. 11, no. 4, pp. 301–305, Apr. 2012. doi: 10.1038/nmat3256.

[21] J. I. Kim, K. S. Chang, D. U. Kim, I.-T. Cho, C.-Y. Jeong, D. Lee, H.-I. Kwon, S. H. Jin, and J.-H. Lee, "Thermoreflectance microscopy analysis on self-heating effect of short-channel amorphous In-Ga-Zn-O thin film transistors," *Appl. Phys. Lett.*, vol. 105, no. 4, 2014, Art. no. 043501. doi: 10.1063/1.4891644.

[22] H. Im, H. Song, J. Jeong, Y. Hong, and Y. Hong, "Effects of defect creation on bidirectional behavior with hump characteristics of InGaZnO TFTs under bias and thermal stress," *Jpn. J. Appl. Phys.*, vol. 54, no. 3S, 2015, Art. no. 03CB03. doi: 10.7567/JJAP.54.03CB03.

[23] S. Oh, B. S. Yang, Y. J. Kim, Y. J. Choi, U. K. Kim, S. J. Han, H. W. Lee, H. J. Kim, S. Kim, J. K. Jeong, and H. J. Kim, "Dynamics of negative bias thermal stress-induced threshold voltage shifts in indium zinc oxide transistors: Impact of the crystalline structure on the activation energy barrier," *J. Phys. D, Appl. Phys.*, vol. 47, no. 16, Apr. 2014, Art. no. 165103. doi: 10.1088/0022-3727/47/16/165103.

[24] S. Choi, J. Jang, H. Kang, J. H. Baeck, J. U. Bae, K.-S. Park, S. Y. Yoon, I. B. Kang, D. M. Kim, S.-J. Choi, Y.-S. Kim, S. Oh, and D. H. Kim, "Systematic decomposition of the positive bias stress instability in self-aligned coplanar InGaZnO thin-film transistors," *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 580–583, May 2017. doi: 10.1109/LED.2017.2681204.

[25] D. H. Kim, S. Choi, J. Jang, H. Kang, D. M. Kim, S.-J. Choi, Y.-S. Kim, S. Oh, J. H. Baeck, J. U. Bae, K.-S. Park, S. Y. Yoon, and I. B. Kang, "Experimental decomposition of the positive bias temperature stress-induced instability in self-aligned coplanar InGaZnO thin-film transistors and its modeling based on the multiple stretched-exponential functions," *J. Soc. Inf. Display*, vol. 25, no. 2, pp. 98–107, Feb. 2017. doi: 10.1002/jsid.531.

[26] S. Lee, A. Nathan, S. Jeon, and J. Robertson, "Oxygen defect-induced metastability in oxide semiconductors probed by gate pulse spectroscopy," *Sci. Rep.*, vol. 5, no. 1, Dec. 2015, Art. no. 014902. doi: 10.1038/srep14902.

[27] T.-C. Chen, T.-C. Chang, C.-T. Tsai, T.-Y. Hsieh, S.-C. Chen, C.-S. Lin, M.-C. Hung, C.-H. Tu, J.-J. Chang, and P.-L. Chen, "Behaviors of InGaZnO thin film transistor under illuminated positive gate-bias stress," *Appl. Phys. Lett.*, vol. 97, no. 11, 2010, Art. no. 112104. doi: 10.1063/1.3481676.

[28] C.-H. Han, S.-S. Kim, K.-R. Kim, D.-H. Baek, S.-S. Kim, and B.-D. Choi, "Effects of electron trapping and interface state generation on bias stress induced in indium–gallium–zinc oxide thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 53, no. 8S3, Aug. 2014, Art. no. 08NG04. doi: 10.7567/JJAP.53.08NG04.

[29] Y. Kang, H.-H. Nahm, and S. Han, "Light-induced peroxide formation in ZnO: Origin of persistent photoconductivity," *Sci. Rep.*, vol. 6, no. 1, Dec. 2016, Art. no. 35148. doi: 10.1038/srep35148.

[30] M. D. H. Chowdhury, S. H. Ryu, P. Migliorato, and J. Jang, "Effect of annealing time on bias stress and light-induced instabilities in amorphous indium–gallium–zinc-oxide thin-film transistors," *J. Appl. Phys.*, vol. 110, no. 11, Dec. 2011, Art. no. 114503. doi: 10.1063/1.3662869.

[31] *ATLAS User's Manual*, Silvaco, Santa Clara, CA, USA, 2018.