A narrow bandgap SiGe channel superlattice bandgap engineered 1T DRAM cell for low voltage operation and extended hole retention time

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A narrow bandgap SiGe channel superlattice bandgap engineered 1T DRAM cell for low voltage operation and extended hole retention time

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Received 11 May 2011, in final form 24 June 2011
Published 10 August 2011
Online at stacks.iop.org/SST/26/095025

Abstract

We propose a SiGe channel superlattice bandgap engineered (SiGe SBE) 1-transistor dynamic random access memory (1T DRAM) cell structure for improved generation and extended retention of hot holes adopting a narrow bandgap Si$_{0.8}$Ge$_{0.2}$ channel even with an extremely short gate length of 30 nm. The proposed SiGe channel SBE 1T DRAM shows longer retention time than the Si channel SBE 1T DRAM. It also provides improved design flexibility by optimizing the structural and process parameters, so the retention characteristics get better. Especially, it should be noted that the retention time can be further improved if the doping concentration of the Si buffer layer decreases. The narrow bandgap SiGe channel SBE structure also allows the 1T DRAM cell to generate more electron–hole pairs during the write ‘1’ operation through the impact ionization in the channel under a high electric field. In addition to the long retention time with the SBE structure, the narrow bandgap SiGe channel SBE 1T DRAM cell enables the 1T DRAM cell to have a fast write speed and to operate at lower voltage, thanks to the narrow bandgap Si$_{0.8}$Ge$_{0.2}$ channel.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

An energy band engineered structure having a Si$_{1-x}$Ge$_x$ storage pocket within the Si body has recently been proposed for the scalability of planar 1-transistor dynamic random access memory (1T DRAM) cells [1, 2]. These structures have an improvement of the drain current difference between read ‘1’ and read ‘0’, thanks to the quantum well (QW). However, there are still problems such as dislocations caused by the lattice mismatch and defect creation by the thick SiGe epitaxial layer, which has a bad influence on the electric performance related to the retention characteristics [3]. As a solution to these issues, we have reported a superlattice bandgap engineered (SBE) 1T DRAM cell with an extremely short gate length of 30 nm [4]. As well as reducing defects from a lattice mismatch through the superlattice heterostructure of Si and SiGe, it is profitable for a hole confinement by using the band offset in the valence band as a potential barrier.

Meanwhile, the SBE 1T DRAM cell with a Si channel as well as the planar SOI 1T DRAM cell needs to have a suppressed leakage current under a cut-off state to guarantee a long retention time with a large sensing margin to distinguish two states. To reduce the leakage current, previous 1T DRAM cells pursue a higher threshold voltage. As a result, it is difficult for 1T DRAM cells to have a high performance for logic device applications due to a limited generation of electron–hole pairs (ehps) and a long time to write data ‘1’. To improve the performance, new concepts of 1T-DRAMs such as the metastable dip RAM (MSDRAM) cell [5, 6], strained SOI 1T DRAM [7] and A-RAM [8] have recently been investigated.
In this work, we report a narrow bandgap SiGe SBE 1T DRAM cell for improved generation and storage and, hence, a large sensing margin. It uses a Si$_{0.8}$Ge$_{0.2}$ channel having a narrower bandgap compared to Si, having all structural merits of the SBE 1T DRAM cell [4]. It has a discrete structural and operational difference compared to a partial SiGe region in the body (substrate) as a QW 1T DRAM [1], URAM with a QW in the buried Si$_{1-x}$Ge$_x$ [2] and the conventional SBE 1T DRAM with the Si channel [4] in that it has a SiGe region in the whole channel. We previously proved the validity of employing the SiGe layer as a channel as well as a body in double HBT-based 1T DRAM cell [9]. However, there is still difficulty in scaling down of the gate length due to the short channel effect with the SiGe layer as a whole body. We note that the strained SiGe channel is usually used to improve the CMOS performance beyond the device scaling limit because of the high drive current enhancement with improved channel carrier mobility [10, 11]. Because the narrow bandgap SiGe channel is more adaptive to the generation of excess carriers during the write ‘1’ operation through the impact ionization, thanks to the narrow bandgap, a high supply voltage or a long write time is not required to increase the driving current. Because the proposed SiGe SBE 1T DRAM cell has a structural merit to have improved performance, it is possible to achieve significantly improved performance while keeping the good retention characteristic. Electrical performance of the proposed SiGe SBE 1T DRAM cell is verified by the Sentaurus 2-D TCAD simulation [12].

2. Device structure of the SiGe channel SBE 1T DRAM

A cross-sectional structure of the proposed SiGe SBE 1T DRAM cell is comparatively shown in figure 1 with the Si channel SBE 1T DRAM cell structure. These devices have an extremely short channel length of 30 nm and the oxide thickness of 1.5 nm, and other design parameters are summarized in table 1. The expected process sequence is described in figure 2 considering a practical implementation for mass production.

Table 1. Simulation parameters for the SiGe SBE capacitorless DRAM cell.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Reference value</th>
<th>Parameter</th>
<th>Reference value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{ch}$</td>
<td>3.0</td>
<td>$N_{ch}$</td>
<td>$1 \times 10^{17}$</td>
</tr>
<tr>
<td>$T_{buffer}$</td>
<td>10</td>
<td>$N_{buffer}$</td>
<td>$1 \times 10^{17}$</td>
</tr>
<tr>
<td>$T_{Si}$</td>
<td>3.0</td>
<td>$N_{Si}$</td>
<td>$1 \times 10^{16}$</td>
</tr>
<tr>
<td>$T_{SiGe}$</td>
<td>0.5</td>
<td>$N_{SiGe}$</td>
<td>$1 \times 10^{16}$</td>
</tr>
<tr>
<td>$T_{Si, bottom}$</td>
<td>1.0</td>
<td>$N_{Si, bottom}$</td>
<td>$6 \times 10^{18}$</td>
</tr>
<tr>
<td>$T_{cap}$</td>
<td>1.0</td>
<td>$N_{cap}$</td>
<td>$1 \times 10^{17}$</td>
</tr>
</tbody>
</table>

Figure 1. Cross-sectional structures of (a) the Si channel SBE 1T DRAM cell and (b) the proposed SiGe SBE 1T DRAM cell with a channel length $L = 30$ nm.
storage layer for extended retention of generated holes as shown in figure 1(b) while the SBE 1T DRAM cell has a crystallized Si channel as shown in figure 1(a). In the SiGe SBE 1T DRAM cell, the top Si capping layer is required to form a gate oxide (SiO₂) and to reduce the defect density at the interface between the gate oxide and Si by blocking an out-diffusion of Ge into the oxide [14, 15]. However, the extremely thick capping layer is not suitable for scaling down to short channel devices because it minimizes the gate-to-channel capacitance [16] and reduces the driving current during the write ‘1’ process. Therefore, a proper and optimized thickness of the Si capping layer is required. The bottom Si buffer layer isolates the Si₀.₈Ge₀.₂ storage layer from the Si₀.₈Ge₀.₂ channel layer for a better retention of generated holes. Namely, the bottom Si₀.₈Ge₀.₂ storage layer works only as a storage layer and not for ehp generation while the top Si₀.₈Ge₀.₂ channel layer is designed for a better ehp generation even at low voltages.

Also the strained Si₀.₈Ge₀.₂ storage layer under the bottom Si buffer layer is not connected to the n⁺ S/D region because it is isolated by the bottom Si buffer layer and by the SiO₂ physical barrier. As a result, most of the SRH recombination occurs in the narrow bandgap channel region, not in the Si₀.₈Ge₀.₂ storage layer, and then the retention time would be significantly improved. Due to the narrow bandgap Si₀.₈Ge₀.₂ channel layer, the SiGe SBE 1T DRAM cell has a distinguishable improvement from the Si channel SBE 1T DRAM cell and other conventional Si channel 1T DRAM cells. The narrow bandgap Si₀.₈Ge₀.₂ channel layer allows a better ehp generation at low voltage with a faster speed due to increased number of ehps and high carrier mobility in the narrow bandgap SiGe channel layer compared to that in the Si channel layer as in conventional 1T DRAM structures. In addition, the voltage at which the current suddenly increases by hot carriers is considerably lowered, so the lower voltage can be used for the write ‘1’ operation and unnecessary power dissipation can be prohibited.

3. TCAD simulation results and discussion

3.1. Memory characteristics and low voltage operation

In order to confirm a robust operation of the SiGe SBE 1T DRAM cell, a 2D TCAD device simulation is performed for a device with a channel length $L = 30$ nm, combining advanced physical models with quantum effects, tunneling mechanisms and mobility models [12]. A hydrodynamic model is used in the simulation to properly describe the deep-submicron devices. And mobility models including the Philips unified mobility model, high-field saturation (velocity saturation) and electric field normal to the interface are specified for the simulation. In the case of the generation
and recombination model, avalanche model, band-to-band tunneling, Auger recombination and SRH recombination considering doping dependence, temperature dependence and electric field are considered in the simulation. The density gradient quantization model is also activated for a quantum correction.

The parameters used for the strained SiGe are values calculated according to the model of Van de Walle [17]. The transport parameters at 300 K for SiGe under biaxial compressive strain are also used when a thin SiGe film is grown on the top of a relaxed Si.

The operating condition is summarized in Table 2 with reference values of $V_{op} = 1.1$ V, $V_{RB} = -0.4$ V and $t_{write} = 50$ ns. For a comparative investigation, the SiGe SBE 1T DRAM cell is under the same condition (doping concentrations, thicknesses and other structural parameters except the channel layer) as the Si channel SBE 1T DRAM cell. There are two differences between them, which are materials organizing the channel and the presence of the Si capping layer above the channel. They are summarized in Table 2 to denote the quantitative parameters used in the comparative simulation of the SiGe SBE 1T DRAM cell with the Si channel SBE structure.

Due to a very thin substrate between the top and bottom gates with a short-channel length of 30 nm, the SiGe SBE 1T DRAM cell is fully depleted and then the role of the bottom gate becomes important. The energy band shows a profitable structure for the long retention time of data ‘1’ and ‘0’. Figures 3(a) and (b) show transient characteristics and valence band structures in the depth direction, respectively, as a function of the bottom gate voltage ($V_{RB}$) during the read operation for the SiGe SBE 1T DRAM cell. (a)Transient characteristics as a function of the bottom gate voltage ($V_{RB}$) during the read operation for the SiGe SBE 1T DRAM cell. (b) Valence band ($E_v$) energy band diagram along the depth direction for low ($V_{RB} = 0.0$ V) and high ($V_{RB} = -0.6$ V) bottom gate voltages during the read operation.

Simulated retention characteristics are shown in figure 4(a) for a SiGe SBE 1T DRAM cell as a function of $V_{RB}$. It is assumed that the minimum difference of 20 $\mu$A per unit width ($W = 1 \mu$m) is required to distinguish two states during the read operation, so the time satisfying this drain current difference more than 20 $\mu$A $\mu$m$^{-1}$ is defined as the retention time. The valence band in the bottom gate region raised by the applied negative $V_{RB}$ helps the energy band of the storage layer as well as the superlattice region to head upward as shown in figure 4(b). It means that there is a low density of holes in the Si$_{0.8}$Ge$_{0.2}$ storage layer, and then the read ‘1’ current becomes smaller when the bottom gate has a negatively higher potential.

Figure 5 shows the bottom gate effect on the retention time during the hold states. If $|V_{shold}|$ is higher than 0.9 V, most generated holes exist in the storage layer due to an electric field formed by it. On the other hand, a smaller $|V_{shold}|$ helps generated holes to be removed from the storage layer, so the retention characteristic of data ‘0’ gets better. Therefore, a

Table 2. Operation conditions for capacitorless 1T DRAM cells.

<table>
<thead>
<tr>
<th>Top gate (V)</th>
<th>Drain (V)</th>
<th>Bottom gate (V)</th>
<th>Source (V)</th>
<th>Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write ‘1’</td>
<td>$V_{op}$</td>
<td>0.0</td>
<td>0.0</td>
<td>$t_{write}$</td>
</tr>
<tr>
<td>Write ‘0’</td>
<td>$-V_{op}$</td>
<td>$V_{op}$</td>
<td>0.0</td>
<td>$t_{write}$</td>
</tr>
<tr>
<td>Read</td>
<td>0.3</td>
<td>0.3</td>
<td>$V_{RB}$</td>
<td>10</td>
</tr>
<tr>
<td>Hold</td>
<td>0.0</td>
<td>0.0</td>
<td>$-V_{op}$</td>
<td>10</td>
</tr>
</tbody>
</table>
Figure 4. (a) Retention characteristics and (b) the valence band energy diagram for various bottom gate voltages \((V_{\text{RB}} = -0.6 \sim 0.0 \text{ V})\) during the read operation for the SiGe SBE 1T DRAM cell.

Figure 5. Retention characteristics of the various bottom gate voltages \((V_{\text{hold}})\) during hold operation for the SiGe SBE 1T DRAM cell.

Figure 6. Output characteristics of the Si channel SBE and SiGe SBE 1T DRAM cells as a function of the gate voltage \((V_{\text{GS}} = 0.1 \sim 1.1 \text{ V})\).

Figure 7 shows output characteristics of the SiGe SBE 1T DRAM compared to the Si channel SBE 1T DRAM as a function of the front gate voltage \((V_{\text{GS}})\). The kink effect is originated from the abrupt increase of ehps by the impact ionization under a high electric field. In order to generate ehps during write ‘1’, channel electrons should acquire an extra kinetic energy \((E_k)\) larger than the bandgap \((E_g)\) of the region where the impact ionization occurs. The kinetic energy is given by

\[
E_k = q \int_0^{L_g} E_l \, dx = q E_l L_g \geq E_g, \tag{1}
\]

where \(E_l\) is the lateral electric field in the channel region.

Because the energy bandgap of the Si\(_{0.8}\)Ge\(_{0.2}\) channel \((E_g, \text{SiGe})\) is narrower than that of the Si channel \((E_g, \text{Si})\), a lower \(E_k\) for the SiGe SBE 1T DRAM cell is required for the impact ionization to occur. That is, the SiGe SBE 1T DRAM cell generates more ehps during the write ‘1’ operation compared to the Si channel SBE 1T DRAM cell even for the same drain and front gate biases at \(V_{\text{DS}} = V_{\text{GS}} = 1.1 \text{ V}\). As expected, more holes generated by the impact ionization can make drain currents higher as shown in figure 6.

Figure 7 shows the drain current difference as a function of the hold time under the same bias condition for the two 1T DRAM cells. When the operating bias \((V_{\text{op}})\) is 1.1 V, the current difference \((\Delta I_{\text{DS}})\) of the Si channel SBE 1T DRAM cell is rapidly decreased with the hold time \((t_{\text{hold}})\) while two 1T DRAM cells having the Si and SiGe channels have a similar \(\Delta I_{\text{DS}}\) for shorter \(t_{\text{hold}}\). Also, when the operating bias becomes \(V_{\text{op}} = 1.0 \text{ V}\), \(\Delta I_{\text{DS}}\) sharply decreases more than at \(V_{\text{op}} = 1.1 \text{ V}\) in the Si channel SBE 1T DRAM cell. This is because the number of the generated excess carriers is proportional to the applied electric field. When \(V_{\text{op}}\) is less than 0.9 V, \(\Delta I_{\text{DS}}\) in the Si channel SBE 1T DRAM cell becomes smaller than 20 \(\mu A \, \mu m^{-1}\). On the other hand, \(\Delta I_{\text{DS}}\) is less sensitive to \(V_{\text{op}}\) in the SiGe SBE 1T DRAM cell since carriers reduced by decreased \(V_{\text{op}}\) are partially compensated with additional

proper value of the bottom gate voltage should be selected during the read and/or hold operation, considering these trade-off relationships.
generation of holes, thanks to the narrow bandgap. As a result, there is a small difference in the drain current after \( t_{\text{hold}} = 1 \text{ s} \) as \( V_{\text{op}} \) is lower than 1.1 V. It means that the SiGe SBE 1T DRAM cell guarantees a robust operation at low voltage compared to the Si channel SBE 1T DRAM and other planar Si channel 1T DRAM cells.

3.2. Design flexibility and retention characteristics

The proposed SiGe SBE 1T DRAM cell provides an improved flexibility on the design and control parameters than those of the conventional 1T DRAM cell because the Si channel of the conventional one is divided into four discrete parts. We preferentially compared the SiGe SBE 1T DRAM cell with the Si channel SBE 1T DRAM under the same conditions for the thickness and doping concentration as shown in figure 8. We also investigated effects of the doping concentration and the thickness on the programming margin and the retention time as shown in figures 9–11.

First of all, under the same conditions for the doping concentration in the Si buffer layer and the channel as well as the structural parameters, the retention characteristic of the SiGe SBE 1T DRAM cell is compared with the Si channel SBE 1T DRAM as shown in figure 8. In the SiGe SBE 1T DRAM cell, the valence energy band of the storage layer is located below that of the Si channel SBE 1T DRAM because more holes are stored in the narrow bandgap Si\(_{0.8}\)Ge\(_{0.2}\) storage layer. It makes holes in the storage layer easy to be swept into the S/D during the hold time. However, because the SiGe SBE 1T DRAM cell generates much more holes than lost holes through an emission into S/D due to the energy band, the drain current for read ‘1’ is higher. Hole concentrations in the p-Si (\( P_{\text{Si}}(E) \)) and p-SiGe channel (\( P_{\text{SiGe}}(E) \)) are described as

\[
P_{\text{Si}}(E) = p_1 \propto n_{i,\text{Si}} \propto e^{-E_g,\text{Si}/kT},
\]

where \( p_1 \propto n_{i,\text{Si}} \propto e^{-E_g,\text{Si}/kT} \).

\[
P_{\text{SiGe}}(E) = p_2 e^{\Delta E_{v}/kT}
\]

where \( p_2 \propto n_{i,\text{SiGe}} \propto e^{-E_v,\text{SiGe}/kT} \).

where \( p_1 \) and \( p_2 \) are determined by the intrinsic carrier concentrations (\( n_i \)) and the doping concentration of the channel layer. Otherwise, \( P_{\text{SiGe}}(E) \) in the p-SiGe channel of the SiGe SBE 1T DRAM cell is additionally affected by the valence band offset (\( \Delta E_v \)) between the Si S/D and the SiGe channel. As a result, holes in the SiGe channel increase exponentially in proportion to \( \Delta E_v \) than those in the Si channel SBE 1T DRAM by

\[
\frac{P_{\text{SiGe}}(E)}{P_{\text{Si}}(E)} = e^{\Delta E_v/2kT + \Delta E_{v,\text{channel}}/kT} > 1
\]

with \( \Delta E_v \equiv E_g,\text{Si} - E_g,\text{SiGe} \) and \( \Delta E_{v,\text{channel}} \equiv E_{V,\text{source}} - E_{V,\text{channel}} \). That is, generated holes can be more stored in the SiGe channel as well as in the storage layer, thanks to the valence band offset between the S/D and the channel. Furthermore, in the case of the SiGe SBE 1T DRAM cell, the write '0' efficiency is improved due to a higher dielectric constant of the SiGe channel layer (\( \varepsilon_r = 12.6 \)) [4]. It is helpful to improve the retention time of state '0'. As a result, it is confirmed that the SiGe channel SBE 1T DRAM cell is better than the Si channel SBE 1T DRAM cell in terms of retention characteristics.

On the other hand, figure 9(d) shows the doping concentration dependence of the Si buffer layer under fixed channel doping of \( 1 \times 10^{17} \text{ cm}^{-3} \) in the SiGe channel SBE 1T DRAM cell. As the doping concentration in the buffer layer is more decreased, the potential drop is increased through the Si buffer layer and then the valence band of the Si\(_{0.8}\)Ge\(_{0.2}\) storage layer is bent up and holes are more stable to be stored. As a result, it is easy to hold generated holes during the hold time and finally the drain current of state '1' increases (figure 9(b)). In the case of state '0', the band-to-band tunneling between the p-type buffer layer and the n\(^+\) drain is quite probable as \( N_{\text{buffer}} \) is extremely increased to \( 1 \times 10^{18} \text{ cm}^{-3} \). It causes degraded retention characteristics of data '0' for higher \( N_{\text{buffer}} \).

Figure 9(c) shows the effect of the Si buffer layer thickness on the retention characteristic. The Si buffer layer plays a major role in separating the Si\(_{0.8}\)Ge\(_{0.2}\) channel from the SiGe channel SBE 1T DRAM cell.
Figure 9. (a) Retention characteristics for the Si channel SBE and the SiGe SBE 1T DRAM cells as a function of the buffer layer doping concentration and (b) valence energy band diagram during hold operation for various buffer doping concentrations. (c) Retention characteristics as a function of the buffer layer thickness.

Si$_{0.8}$Ge$_{0.2}$ storage layer just as the SiO$_2$ physical barrier does. As the distance between the carrier generation region and the carrier storage region becomes extremely longer, it is difficult for the holes in the Si$_{0.8}$Ge$_{0.2}$ storage layer to be emitted into the S/D during write ‘0’. It induces the read ‘0’ current to increase.

Figure 10. Retention characteristics of the proposed SiGe SBE 1T DRAM cell. (a) Retention characteristics of the Si channel SBE and the SiGe SBE 1T DRAM cells as a function of the channel doping concentration ($N_{\text{ch}}$). (b) Retention characteristics as a function of the channel thickness ($T_{\text{ch}}$).

However, a thin $T_{\text{buffer}}$ causes the band-to-band tunneling to increase due to the reduced distance between holes stored in the storage layer and highly doped S/D. Thus, a longer buffer layer is preferred to have a better retention characteristic as shown in figure 9(c).

A higher channel doping concentration is usually required to reduce the off-state leakage current in 1T DRAM cells. However, a high channel doping induces an accelerated band-to-band tunneling through the n$^+$/p$^+$ junction near the S/D. It makes the data ‘0’ retention time degraded as the hold time gets increased as shown in figure 10(a). Figure 10(b) shows the retention time as a function of the channel thickness. Likewise, the total number of ehps generated by the impact ionization is directly proportional to the thickness of the Si$_{0.8}$Ge$_{0.2}$ channel; the thick channel layer augments the write ‘1’ current. However, the thickness of the SiGe channel should be within the critical thickness to keep a strained state without inducing crystal defects [16], although a defect generation above the critical thickness cannot be reflected in the simulation model. Therefore, the channel thickness of 3 nm is chosen to be appropriate. In figure 11(a), the write ‘0’ operation is limited...
Figure 11. Retention characteristics of the SBE 1T DRAM cells as a function of storage layer doping and thickness. (a) Retention characteristics of the SiGe SBE 1T DRAM cells as a function of the Si$_{0.8}$Ge$_{0.2}$ storage layer doping concentration ($N_{str}$). (b) Retention characteristics as a function of the Si$_{0.8}$Ge$_{0.2}$ storage layer thickness ($T_{str}$).

by the extremely high doping concentration. This is because the quantized holes head toward the stable state in terms of the energy level. As the Si$_{0.8}$Ge$_{0.2}$ storage layer thickness gets thicker, the volume to store holes generated by the impact ionization also increases and the read current of data ‘0’ is slowly increased with the hold time due to the decreased band-to-band tunneling. Consequently, the retention characteristic is improved and the hole current by write ‘1’ is increased for the thicker Si$_{0.8}$Ge$_{0.2}$ storage layer as shown in figure 11(b). However, the thickness of the Si$_{0.8}$Ge$_{0.2}$ storage layer ($T_{str}$) should also be within the critical thickness just as the Si$_{0.8}$Ge$_{0.2}$ channel does, so $T_{str} \approx 3$ nm is obtained to be suitable for proper operation.

3.3. Writing speed

A fast write speed is one of the key performance parameters in the 1T DRAM cells. The write time is inversely proportional to the number of holes generated by the impact ionization for data ‘1’. Namely, the write speed gets fast if more holes are generated in a given time. The generated holes increase with increasing gate and drain biases due to high vertical and lateral fields in the DRAM cell or long programming time. However, a high drain bias is not desirable for a high density memory because power dissipation and reliability concerns through the gate oxide may occur, so a new alternative is needed for high performance capacitorless 1T DRAM cells.

Figure 12 shows the drain current differences (read ‘1’ current – read ‘0’ current) in the proposed SiGe SBE 1T DRAM cell compared to the Si channel SBE 1T DRAM for the write time as a function of the operating voltage when the hold time is 10 ns and 10 ms. In the Si channel SBE 1T DRAM cell, a shorter write time below 50 ns gives a very small difference between read ‘1’ and ‘0’ in the drain current regardless of the operating voltage because it cannot generate enough number of ehps during that short write time. However, in the SiGe SBE 1T DRAM cell, the decreasing rate of the sensing margin is very small as the write time becomes short (figure 12(a)). This is because the SiGe SBE 1T DRAM cell has a Si$_{0.8}$Ge$_{0.2}$ channel with a narrow energy bandgap and, therefore, more ehps can be generated during the short write time compared to the Si channel SBE 1T DRAM cell. After 1 s of the hold
time, the drain current difference of the SiGe SBE 1T DRAM cell is smaller than that of the Si channel SBE 1T DRAM cell because it has a large drain current for read ‘0’ (figure 12(b)). However, when the write time becomes shorter, the SiGe SBE 1T DRAM cell can generate much more holes, so it has a larger drain current difference. As mentioned earlier, the SiGe SBE 1T DRAM cell provides enough drain current difference than that in the Si channel SBE DRAM cell at a low operation voltage. For these results, we confirmed a high performance with outstanding retention characteristics from the SiGe SBE 1T DRAM cell.

4. Conclusion

A SiGe SBE 1T DRAM cell with a narrow bandgap Si$_{0.8}$Ge$_{0.2}$ channel is proposed for the sub-30 nm channel length and we confirmed memory characteristics using a 2D TCAD simulation. We verified the proposed SiGe channel SBE 1T DRAM cell to have a fast writing speed and operate at low supply voltage due to the Si$_{0.8}$Ge$_{0.2}$ channel layer with a smaller bandgap compared to the Si channel layer in conventional 1T DRAM cells. In addition, it has a good retention time as in the Si channel SBE 1T DRAM cell with identical structural characteristics except the narrow bandgap SiGe channel layer. The retention time is also improved compared to that of the Si channel SBE 1T DRAM and other conventional 1T DRAM cells with a Si layer for the channel by controlling the structural and process parameters. It was also confirmed that the proposed SiGe SBE 1T DRAM cell has better performance with improved retention time allowing a low voltage operation and a fast write speed.

Acknowledgments

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean Government (MEST) (grant nos 2010-0013883 and 2009-0080344). The CAD software was supported by the IC Design Education Center (IDEC).

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