Modeling and extraction technique for parasitic resistances in MOSFETs Combining DC I–V and low frequency C–V measurement

Ja Sun Shin, Hagyoul Bae, Euiyoun Hong, Jaeman Jang, Daeyoun Yun, Jieun Lee, Dae Hwan Kim,* Dong Myong Kim

School of Electrical Engineering, Kookmin University, 861-1 Jeongneung-dong, Seongbuk-gu, Seoul 136-702, Republic of Korea

ARTICLE INFO

1. Introduction

With a scaling down of devices in the CMOS technology, the device performance strongly depends on the parasitic source (R_S), drain (R_D), substrate (R_sub), and gate (R_G) resistances. The parasitic gate resistance, which is a crucial determinant in high speed and high frequency performance, significantly increases with a scaling down of the gate length (L) in extremely short channel MOSFETs with a poly-silicon. In conventional techniques, RF/MW vector network analyzer was employed for extraction of R_G from scattering parameters [1–5]. Currently, RF transistor models provided by foundry usually consisted of an intrinsic core model with added extrinsic parasitic resistances at the gate, source, drain, and substrate [6]. On the separate extraction of the asymmetric R_G from R_B [7–9], there are few reports to distinguish the spreading current path-dependent resistance component (R_{sh} or R_{dn}) below the spacer from the extrinsic resistance (R_{so} or R_{se} in the source or drain) as shown in Fig. 1. Even though Ng and Lynch [10] separated the intrinsic sheet resistance (R_{sh} \equiv R_{so} + R_{dn}) from the extrinsic contact resistance (R_{c} \equiv R_{se} + R_{de}) using analytical equations, it is effective only when process variables are provided. In addition, R_{so} in the source has not been separated from R_{se} in the drain through Ng and Lynch [10], while R_{se} has been separated from R_{so} in [11].

In this work, we report a simple technique with equivalent circuit model for a completely separate extraction of R_{se} from R_{so}, as well as R_{so}, R_{se}, R_{de}, and R_{se}, as parasitic resistances in MOSFETs without employing multiple devices by using lab-basic DC I–V (current–voltage) and low-frequency (LF) C–V (capacitance–voltage) characterization equipment [9,12]. The proposed technique does not require particular de-embedding test structures or special pad patterns as in the microwave probing through a vector network analyzer to obtain intrinsic s-parameters.

2. Experimental procedure for complete extraction

A lumped element equivalent model is schematically shown in Fig. 1 with parasitic resistances and capacitances in MOSFETs under above-threshold bias (V_C > V_T). Here we applied the proposed method to the MOSFETs without leaky/conductive path through the gate oxide, while the resistance considering the leaky path through the gate oxide should be included in parallel with C_{OX} in MOSFETs with a ultra-thin gate oxide in extremely scaled devices [13].

The gate length- and gate bias (V_{GS})-independent extrinsic resistances (R_{ext} \equiv R_{so} + R_{dn} + R_{se} + R_{de}) can be divided into R_{so} and R_{de} in the source and R_{se} and R_{de} in the drain. Spreading

* Corresponding author. Tel.: +82 2 910 4719; fax: +82 2 910 4449.
E-mail address: dmkim@kookmin.ac.kr (D.M. Kim).

Please cite this article in press as: Shin JS et al. Modeling and extraction technique for parasitic resistances in MOSFETs Combining DC I–V and low frequency C–V measurement. Solid State Electron (2012). doi:10.1016/j.sse.2012.01.007
component $R_S$ and $R_D$ depend on the spacer between the S/D and contact and the gate while the extrinsic elements $R_{se}$ and $R_{De}$ depend mainly on the contact property. As the lab-basic equipment, we employed HP 4284A for C-V and Agilent 4156C for $I$-$V$ measurement in the proposed technique for the complete separate extraction of parasitic resistances in MOSFETs.

As the first step for the proposed extraction technique, in order to extract $R_{ext}$, the total resistance ($R_{Tlinear}$) is obtained from the current in the linear region under small drain voltage ($V_{DS}$) through the Path I (Fig. 2a). It is described by

$$R_{Tlinear} = V_{DS}/I_D = (R_{S} + R_{so} + R_{De} + R_{Do}) + R_{SD}(V_{GS}) + R_{ch}(V_{GS}, L_{eff}) \quad (1a)$$

$$R_{ext} = R_{S} + R_{so} + R_{De} + R_{Do} \quad (1b)$$

$$R_{SD}(V_{GS}) = \frac{\Delta L}{\mu_{int}C_{ox}W(V_{GS} - V_{T})} \quad (1c)$$

$$R_{ch}(V_{GS}) = \frac{L_{eff}}{\mu_{int}C_{ox}W(V_{GS} - V_{T})} \quad (1d)$$

with $\mu_{int}$ and $\mu_{ch}$ as the bias-dependent effective mobility in the lightly-doped source/drain (LDD) region and the channel, respectively. If $V_{GS}$ is high enough to remove $R_{SD}(V_{GS})$ and $R_{ch}(V_{GS}, L_{eff})$ in the measured $R_T$, $R_{ext}$ can be obtained from the $R_T$ versus $V_{GS}$ ($\equiv V_{GS} - V_{T}$) through an extrapolation to a large effective gate voltage. Here, $R_{SD}$ is obtained under the assumption that $R_{So}$ is negligible compared with $R_{SD}$ when the effective gate voltage ($V_{GS} - V_{T}$) is extrapolated to infinity through the fitting function of the Eq. (1).

We note that $R_{Se}$, $R_{De}$, $R_{So}$, and $R_{Do}$ can be separately extracted through the proposed technique combining $I$-$V$ and $C$-$V$ as long as the total $R_{SD}$ is extracted. Namely, other methods [14,15] can be combined to the extraction of $R_{SD}$ especially in modern devices with a short gate length.

As the next step, $R_1 = (R_{S} + R_{De} + R_{C})$ or $R_2 = (R_{Do} + R_{De} + R_{C})$ is obtained through the $C$-$V$ measurement for Path V or Path VI. For the gate bias ($V_{G}$)-dependent $C$-$V$ characterization, a parallel mode of the measured resistance ($R_{m}$) and capacitance ($C_{m}$) is employed to get $C_{Se} - V_{C}$ curve shown as an inset in Fig. 3a. $R_{m}$ and $C_{m}$ are converted as series mode capacitance ($C_{Se}$) and resistance ($R_{Se}$) through the impedance identity. $R_{Se}$ converted from the two terminal (gate-to-source: $G$-$S$ and gate-to-drain: $G$-$D$) $C$-$V$ measurement is equivalent to combination of the parasitic resistances within the MOSFET. Therefore, $R_{Se,G-S}$ for the $G$-$S$ and $R_{Se,G-D}$ for the $G$-$D$ configurations are described by

$$R_{Se,G-S}(V_C) = \frac{R_{m1}}{1 + (\alpha C_{m1} R_{m1})} = (R_{So} + R_{Se} + R_{C}) + R_{th,S}(V_C) \quad (2a)$$

$$R_{Se,G-D}(V_C) = \frac{R_{m2}}{1 + (\alpha C_{m2} R_{m2})} = (R_{Do} + R_{De} + R_{C}) + R_{th,D}(V_C) \quad (2b)$$

where $V_{C}$-independent $R_{C}$ is governed by the sheet resistivity ($\rho_S$) and device structure ($W$ and $L$), which is close to 1, is employed to compensate a deviation of the $V_{C}$-dependency of the channel resistance during the $C$-$V$ characterization. $R_1$ and $R_2$ can be obtained by considering the leaky conducting path in the thin gate oxide through two frequency method [16], if the gate length of the measured device is shorter than 0.35 μm.

As the final step, the parasitic junction current method (PJCM) [9] is combined for a separation of $R_{Se}$ (or $R_{De}$) into individual $R_{Se}$ and $R_{So}$ (or $R_{De}$ and $R_{Do}$) as well as the extraction of $R_{sub}$. By combining Eqs. (2) and (3) with the PJCM, $R_{So}$ and $R_{Do}$ can be fully separated by

$$R_{So} = R_1 - R_{Se, PJCM} = (R_1 |_{eq(2a)} - R_1 |_{eq(3)}) - R_{Se, PJCM} \quad (4a)$$

$$R_{Do} = R_2 - R_{De, PJCM} = (R_2 |_{eq(2b)} - R_2 |_{eq(3)}) - R_{De, PJCM} \quad (4b)$$

Fig. 1. An equivalent circuit considering the leakage current through the gate oxide for LDD MOSFETs with parasitic resistances, oxide capacitance ($C_{ox}$), inner finger capacitance ($C_{f}$) and source/drain overlap capacitance ($C_{So}/C_{Do}$).

Fig. 2. (a) $R_T$ versus $V_{GS}$. The inset is the output characteristics for various $V_{GS}$. (b) $R_T$ versus $L$ with several different values of $V_{GS}$.

Please cite this article in press as: Shin JS et al. Modeling and extraction technique for parasitic resistances in MOSFETs Combining DC $I$-$V$ and low frequency $C$-$V$ measurement. Solid State Electron (2012), doi:10.1016/j.sse.2012.01.007
Therefore, combining the 4 terminal $I$–$V$ data for Path I, PJCM for Paths II–IV, and the 2 terminal $C$–$V$ data for Paths V and VI in Fig. 1, a complete extraction of parasitic resistances ($R_{S0}, R_{D0}, R_{So}, R_{De}, R_{Sub}$, and $R_{G}$) in MOSFETs is possible in MOSFETs without employing multiple devices having various $W/L$ combinations or specific test patterns.

3. Experimental results and discussions

For a verification of the proposed technique, we employed n-channel MOSFETs with a poly-Si gate. Output characteristic of a MOSFET with $W/L = 175/0.35 \mu m$ is shown in the inset of Fig. 2a. Under $V_{DD} \sim 0.05 \, V$ in the linear operation, $R_T$ is obtained as a function of $V_{DS}$ shown in Fig. 2a. Through Eq. (1) with experimental data shown in Fig. 2a, $C$–$V$-independent $R_{ext}$ is obtained to be $R_{ext} = R_{So} + R_{So} + R_{D0} + R_{De} = 12.91 \, \Omega$. By comparing $R_{ext}$ of the single device obtained from Fig. 2a with one extracted by channel resistance method (CRM) in Fig. 2b [12], the validity of $R_{ext}$, which is used to separately extract the extrinsic resistances, is verified. (That is, it is not true that Fig. 2b is imperatively necessary to extract $R_{ext}$ in proposed method.) $R_{ext|CRM} (= R_{So} + R_{D0})$, determined from the intercept of the three lines, is obtained to be 13.06 $\Omega$ as shown in Fig. 2b and almost consistent with that extracted in a single device for $W/L = 175/0.35 \mu m$.

Fig. 3a shows a series mode capacitance ($C_{se}$) versus $V_{G}$ converted from the data obtained by the parallel mode $C$–$V$ measurement at $1 \, MHz$. It is directly proportional to $L$ under strong inversion ($V_{C} > V_{T}$). The inner fringing capacitance ($C_{Gi}$), which can affect the total capacitance as the channel length gets short under strong inversion, can be added to the overlap capacitance ($C_{sov}$, $C_{Dov}$) [17] as shown in Fig. 1. Namely, the sum of $C_{sov}$ ($C_{Dov}$) and $C_{Gi}$ is extracted to be 0.2 pF from $L$-independent capacitance term because these do not depend on the channel length. The inset of Fig. 3b shows the series resistances of the gate-to-drain ($R_{G,C,D}$) and gate-to-source ($R_{G,C,S}$) terminals converted by Eqs. (2a) and (2b). In the extraction of $R_{1|=|}R_{2;G,S}$ and $R_{3;G,D}$, the fitted functions of $R_{se,C,S}$ and $R_{se,G,D}$ are used due to a fluctuation of the measured $C$–$V$ data. For a MOSFET with $W/L = 175/0.35 \mu m$, we obtained $R_{T} = 1902.29 \, \Omega$, $R_{S} = 1902.84 \, \Omega$ and finally $R_{C} = 1896 \, \Omega$ from Eq. (3). Therefore, $V_{C}$-independent $R_{C}$ extracted in n-channel MOSFETs with various channel lengths is shown in Fig. 4. We verified the validity of this extraction method by showing almost constant slope ($=3.7 \, \Omega/\mu m$), which is the sheet resistance $\rho_{S}$ of the poly-Si gate. It is because the resistivity and gate thickness of devices on one wafer are the same. According to the fabrication condition of devices measured in this work, $\rho_{S}$ from typical specifications is 3.5 $\Omega/\mu m$ and maximum $\rho_{S}$ is 10 $\Omega/\mu m$.

Through the stepwise procedure proposed in this work, we obtained $R_{S} = 3.34 \, \Omega$, $R_{D0} = 3.31 \, \Omega$, and $R_{Sub} = 5.67 \, \Omega$ from the PJCM. Finally, $R_{So} = R_{S} - R_{C} - R_{Se} = 2.84 \, \Omega$ and $R_{De} = R_{D0} - R_{C} - R_{De} = 3.42 \, \Omega$ is also extracted from Eqs. (4a) and (4b). The extrinsic resistances completely extracted from the proposed technique using DC $I$–$V$ and LF $C$–$V$ are summarized in Table 1. Here, the extracted $R_{S}$ and $R_{D0}$ are verified by comparing $R_{So}$ from CRM. The difference of $R_{S0}$ and $R_{D0}$ or that of $R_{So}$ and $R_{De}$ can be occurred in the case considering the asymmetries caused by the intentional and/or accidental layout and process variation. Also, the normalized gate resistances $R_{C}$ is obtained from extracted result and that from process data are compared for the verification. In the case of the MOSFET with the same gate width, $R_{S}$, $R_{D0}$, and $R_{Sub}$ also show a small fluctuation according to gate length variation. The normalized gate resistance

![Fig. 3. (a) $C_{se}$ versus $V_{G}$ for various gate lengths. The inset shows that the parallel mode of $R_{m}$ and $C_{m}$ measured at 1 MHz is converted to a series mode of $R_{se}$ and $C_{se}$. (b) $R_{se}$ versus $V_{G}$ above $V_{T}$.](image)

![Fig. 4. The extracted $V_{C}$-independent $R_{C}$ versus $W/L$ ratio.](image)

<table>
<thead>
<tr>
<th>$L$ ($\mu m$)</th>
<th>0.35</th>
<th>1.05</th>
<th>1.75</th>
<th>2.45</th>
<th>3.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{S}$</td>
<td>3.34</td>
<td>3.32</td>
<td>3.33</td>
<td>3.22</td>
<td>3.36</td>
</tr>
<tr>
<td>$R_{D0}$</td>
<td>2.84</td>
<td>2.96</td>
<td>3.04</td>
<td>2.88</td>
<td>2.84</td>
</tr>
<tr>
<td>$R_{C}$</td>
<td>6.18</td>
<td>6.28</td>
<td>6.37</td>
<td>6.10</td>
<td>6.20</td>
</tr>
<tr>
<td>$R_{Sub}$</td>
<td>2.84</td>
<td>2.96</td>
<td>3.04</td>
<td>2.88</td>
<td>2.84</td>
</tr>
<tr>
<td>$R_{D0} - R_{C}$</td>
<td>From CRM,</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{Sub}$</td>
<td>5.67</td>
<td>6.83</td>
<td>6.69</td>
<td>6.96</td>
<td>6.86</td>
</tr>
</tbody>
</table>

Table 1

Extracted parasitic resistances in n-MOSFETs ($W = 175 \mu m$) through the proposed DC $I$–$V$ and LF $C$–$V$ technique.

Please cite this article in press as: Shin JS et al. Modeling and extraction technique for parasitic resistances in MOSFETs Combining DC $I$–$V$ and low frequency $C$–$V$ measurement. Solid State Electron (2012), doi:10.1016/j.sse.2012.01.007
shows very uniform result even with $L$-dependent small variations. These verify a usefulness of the proposed technique for separate extraction of parasitic resistances in individual MOSFETs.

4. Conclusion

In this work, a simple technique combining DC $I-V$ and LF $C-V$ for a separate extraction of parasitic extrinsic resistances ($R_C$, $R_S = R_{So} + R_{Sdp}$, $R_D = R_{Do} + R_{Dde}$, and $R_{sub}$) in MOSFETs was proposed. It combined easy-accessible lab-basic $I-V$ and parallel mode $C-V$ equipment for the characterization of parasitic resistances without employing multiple devices or MW vector network analyzer. The current path-dependent source resistance $R_{So}$ was also fully separated from the current path-dependent drain resistance $R_{Do}$. We expect that the proposed technique is useful in the extraction of completely separated parasitic resistances in individual MOSFETs for accurate and convenient characterization, modeling, and application to a systematic design and robust implementation of CMOS integrated circuits.

Acknowledgments

This work was supported by the National Research Foundation of Korea (NRF) Grant funded by the Korean Government (MEST) (Grants Nos. 2010-0013883 and 2009-0080344). The CAD software was supported by SILVACO and IC Design Education Center (IDEC).

References


Please cite this article in press as: Shin JS et al. Modeling and extraction technique for parasitic resistances in MOSFETs Combining DC $I-V$ and low frequency $C-V$ measurement. Solid State Electron (2012), doi:10.1016/j.sse.2012.01.007