Comparative analysis of temperature thermally induced instability between Si–In–Zn–O and Ga–In–Zn–O thin film transistors

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Thermally induced instability of amorphous Si–In–Zn–O (SIZO) with 1 wt.% silicon (Si) concentration and Ga–In–Zn–O (GIZO) with gallium (Ga) of 30 wt.% thin film transistors (TFTs) has been investigated, by comparing the density of states extracted from multi-frequency method. It was observed that the density of state of SIZO-TFT was lower than that of GIZO-TFT, in spite of low processing temperature of SIZO-TFT and thermally induced instability of SIZO- and GIZO-TFT was strongly related with the total trap density. We report that Si of only 1 wt.% in SIZO can improve thermal stability of threshold voltage of In–Zn–O based TFTs more effectively than Ga of 30 wt.% in GIZO.

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1. Introduction

Transparent amorphous oxide semiconductors (TAOSs) based thin-film transistors (TFTs) have been intensively investigated for various electronic applications including active matrix organic light emitting diode and active matrix liquid crystal display due to their high field effect mobility than that of conventional hydrogenated amorphous silicon thin TFTs [1–2]. In addition, TFTs using the TAOSs as an active channel layer can be fabricated even at room temperature, resulting in cost reduction in device fabrication [3]. TAOSs also have good optical transparency in visible light region, thermal/chemical stability [4] and environmental stability [5]. Amorphous Ga–In–Zn–O (GIZO), as the most representative TAOS material, TFT has high field effect mobility and good stability under various stress conditions, such as illumination stress, bias stress and temperature stress [6–7]. In general, amorphous GIZO-TFT fabricated at room temperature has been annealed at temperature ranging between 300 °C and 400 °C in thermal furnace [8–9]. Meanwhile, it was reported that amorphous Si–In–Zn–O (SIZO) TFT fabricated at the processing temperature of 150 °C has high field effect mobility and good stability under varied stress conditions [10–11]. Therefore, amorphous SIZO-TFT fabricated at low processing temperature can be applied in a flexible electronics. Until now, comparative study of SIZO- and GIZO-TFT on instability under temperature stress using density of states (DOSs) has never been reported.

In this paper, instability induced by temperature stress of SIZO- and GIZO-TFT fabricated at processing temperatures of 150 °C and 350 °C is systematically investigated and comparatively analyzed, by using their DOSs extracted from multi-frequency method (MFM) technique [12] and their activation energy (E_A) depending on gate voltage (V_GS). Also, it is reported that 1 wt.% silicon (Si) as a stabilizer in SIZO channel layer [13] can improve thermally induced instability of threshold voltage of In–Zn–O based TFTs more effectively than 30 wt.% gallium (Ga) in GIZO. In particular, it is suggested that the origin of instability under temperature thermally induced stress is closely related with total trap density of SIZO- and GIZO-TFT.

2. Experimental details

150 nm thick Mo, as gate electrode, patterned by shadow mask was deposited on glass substrate by direct current sputtering method. Also, 200 nm thick amorphous SiN, which acts as gate dielectric was prepared by using plasma enhanced chemical vapor deposition at 350 °C, and then amorphous SIZO and GIZO channel layer with 30 nm in thickness were grown by radio frequency magnetron sputtering method at room temperature, respectively. Amorphous SIZO and GIZO channel layers and source/drain electrodes were well defined by a conventional photolithography and wet etching process. 10 nm thick Ti and 60 nm thick Au, as source/drain electrodes, were deposited by electron beam evaporation and thermal evaporation method, respectively. The lift-off process was performed by dipping TFTs in acetone. The channel length (L) and width (W) of SIZO- and GIZO-TFT were kept at 200 μm and 100 μm, respectively. The SIZO-TFT was annealed at 150 °C for 1 h in thermal furnace with N₂ atmosphere. The GIZO-TFT was annealed at 350 °C for 1 h in N₂ atmosphere.

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ambient atmosphere. The SIZO- and GIZO-TFT were fabricated at their optimized sputtering conditions, respectively. The optimized sputtering conditions for SIZO and GIZO active layer including total pressures, sputtering gases, oxygen partial pressures, and sputtering power were 0.4 Pa, Ar/O2 for SIZO and only Ar for GIZO, 2 sccm for SIZO and 30 W, respectively. All of transfer characteristics were obtained by using semiconductor parameter analyzer (HP 4145B) in dark and vacuum state of ~2.67 Pa, since all of TFTs were unpassivated. Also, the thermal stress was measured in vacuum and in the dark state at temperature ranging from 293 K to 353 K. All of Vth values were determined by 10 nA×L/W at VDS = 10.1 V [14]. The gate capacitance (C–V) measurements made at frequencies of 10 to 1000 Hz as a function of gate voltage were performed by using precision LCR meter (Agilent 4284A). Finally, the subgap DOSs of SIZO- and GIZO-TFT were extracted from frequency independent C–V data [12].

Table 1

<table>
<thead>
<tr>
<th>Channel layer</th>
<th>Vth (V)</th>
<th>μFE (cm²/V-s)</th>
<th>Ion/off ratio</th>
<th>Subthreshold swing (V/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIZO</td>
<td>1.14</td>
<td>8.52</td>
<td>2.8×10⁷</td>
<td>0.74</td>
</tr>
<tr>
<td>GIZO</td>
<td>9.31</td>
<td>8.52</td>
<td>7.7×10⁷</td>
<td>0.91</td>
</tr>
</tbody>
</table>

3. Results and discussion

Fig. 1 shows transfer curves of amorphous SIZO- with Si of 1 wt.% and amorphous GIZO-TFT with Ga of 30 wt.% in concentration respectively. It was confirmed that the SIZO active layer prepared at room temperature by sputtering method followed by annealed at 150 °C has amorphous structure by high resolution transmittance electron microscopy and fast Fourier transform analysis [10]. Electrical properties of the SIZO- and GIZO-TFT, such as threshold voltage (Vth), field effect mobility (μFE) and on-off current ratio (Ion/off ratio) were summarized in Table 1. The SIZO-and GIZO-TFT showed identical μFE value. Also, the SIZO-TFT showed better subthreshold swing (SS) and lowerIon/off ratio than those of the GIZO-TFT. Especially, the Vth of SIZO-TFT was shifted toward further negative direction, compared with that of the GIZO-TFT.

As shown in Fig. 2, the SIZO-TFT had less total trap density, which includes the interface states between a channel layer and a gate insulator and bulk traps in semiconductor channel region, than that of the GIZO-TFT, in spite of low processing temperature. By integrating the area below DOSs, the calculated total trap density of the SIZO- and GIZO-TFT was 2.94×10¹⁶ cm⁻³ and 3.24×10¹⁶ cm⁻³, respectively. Also, the carrier concentration (cm⁻³) in SIZO- and GIZO-TFT was 3.1×10¹⁶ cm⁻³ and 1.2×10¹⁶ cm⁻³, which was estimated by using the equation n = IDSL/qVDS μFE W/d, where n is the carrier concentration, IDS is the drain to source current at a drain voltage (VDS) of 0.5 V and VGS = 0 V, d is the semiconductor thickness, q is the electron charge, and μFE is the electron mobility [15]. Therefore, further negative Vth shift of SIZO-TFT as shown in Fig. 1 can be originated from less DOS and/or more carrier concentration.

Fig. 3 shows the Vth shift of SIZO- and GIZO-TFT under thermally temperature induced stress. As increasing temperature, the Vth values were shifted to negative direction for the SIZO- and GIZO-TFT, since captured electrons are emitted from traps by thermal energy as in amorphous Zn–In–Sn–O TFTs [16]. As a result, the Vth shift induced by temperature stress from 293 K to 353 K was 1.32 V for the SIZO-TFT and 1.51 V for the GIZO-TFT, respectively. Based on these results, it is believed that the variation of Vth shift under temperature stress is consistent well with that of total trap density as shown in Fig. 2. Therefore, we report that total trap density in the SIZO and GIZO channel layer has a significant effect on temperature induced Vth instability of the TFTs. In addition, 1 wt.% Si atoms in SIZO can improve thermally induced instability of Vth of In–Zn–O based TFTs more effectively than Ga atoms of 30 wt.% in GIZO.

Fig. 4 illustrates the Ec (Ec = En – Er) as a function of VGS of the SIZO- and GIZO-TFT, respectively. The Ec and Er are defined as conduction band minimum and Fermi energy, respectively. The Ec was estimated by fitting the drain to source current curves in subthreshold region with inverse temperature, which was obtained from transfer curves in Fig. 3 [16–17]. As shown in Fig. 4, the falling rate defined as the rate of change of Ec was 0.25 eV/(V)⁻¹ for the SIZO-TFT and 0.16 eV/(V)⁻¹ for the GIZO-TFT. Therefore, it is confirmed that total trap density of the SIZO-TFT is lower than that of the GIZO-TFT, since the falling rate is inversely proportional to total trap density [16].

Fig. 5 shows the variation of electrical properties of the SIZO- and GIZO-TFT as a function of temperature. As shown in Fig. 5(a), μFE of SIZO-TFT was degraded to 4.26 cm²/Vs at 40 °C. However, μFE of GIZO-TFT was not changed. Also, the variation in SS of SIZO-TFT with different temperatures was larger than that of the GIZO-TFT. However, relatively low processing temperature could be considered for the performance of SIZO-TFT in terms of μFE and SS as a function of temperature.
4. Conclusions

1 wt.% Si incorporated amorphous SIZO-TFT fabricated at 150 °C showed slightly better stability of $V_{th}$ under thermal stress than that of amorphous GIZO-TFT with processing temperature of 350 °C. It was observed that DOS in SIZO-TFT was lower than that of GIZO-TFT. The result suggests that the thermally induced $V_{th}$ shift in amorphous SIZO and GIZO is closely related with the variation of total trap density. In addition, Si of 1 wt.% in SIZO can improve stability of $V_{th}$ under thermal stress more effectively than Ga of 30 wt.% in GIZO.

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