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# Artificial synaptic characteristics with strong analog memristive switching in a Pt/CeO<sub>2</sub>/Pt structure

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## Abstract

Artificial synaptic potentiation and depression characteristics were demonstrated with  $Pt/CeO_2/Pt$  devices exhibiting polarity-dependent analog memristive switching. The strong and sequential resistance change with its maximum to minimum ratio >10<sup>5</sup>, imperatively essential for stable operation, as repeating voltage application, emulated the potentiation and depression motion of a synapse with variable synaptic weight. The synaptic weight change could be controlled by the amplitude, width, and number of repeated voltage pulses. The voltage polarity-dependent and asymmetric current–voltage characteristics and consequential resistance change are thought to be due to local inhomogeneity of electrical and physical states of CeO<sub>2</sub> such as charging at interface states, valence changes of Ce cations, and so on. These results revealed that the CeO<sub>2</sub> layer could be a promising material for analog memristive switching elements with strong resistance change, as an artificial synapse in neuromorphic systems.

Keywords: artificial synapse, memristive device, analog resistance change, CeO2

(Some figures may appear in colour only in the online journal)

# 1. Introduction

Artificial synapses emulating biological synaptic behavior have been under active investigation for their application to highly energy efficient neuromorphic systems [1–14]. Artificial synapses connected with neuron circuits that have a high connectivity allow for simultaneous parallel signal processing and consequently adaptive learning/memory functions with a modulated synaptic weight. Memristive devices with a metal– resistive switching element–metal structure have a memorized resistance change as a result of signal processing, so they have been considered as one of the promising candidates for artificial synapses [1–10]. Besides the memristive devices, synaptic transistors with a memorized conductance change have been also proposed, with these having several structures and operation principles such as a ferroelectric field effect transistor [11], nonvolatile floating-gate transistor [12], synaptic transistor using the modulation of a channel state through ionic exchange with a gate insulator [13, 14], and so on.

Until now, a variety of memristive elements with metal oxides have been explored for use in an artificial synapse [1–5]. For instance, Borghetti *et al* reported a hybrid logic-inmemristor with digitally configured TiO<sub>2</sub>-memristor arrays performing logic functions as an electronic synapse computer [1]. Yu *et al* also reported multilevel resistance change in a TiN top electrode/TiO<sub>x</sub>/HfO<sub>x</sub>/TiO<sub>x</sub>/HfO<sub>x</sub>/Pt bottom electrode structure and applied it to the simulation of a neuromorphic visual system [2]. The actual biological synapse experiences an analog-type change of synaptic weight for consequent adaptive learning/memory states through the alteration of released neurotransmitters, neurotransmitter receptors, and the number of Ca ion channels inside the synapse as a result of signal processing. In this regard, the



Figure 1. RBS spectra of (a) non-annealed and (b) 600  $^{\circ}$ C-annealed CeO<sub>2</sub> layers on Si substrate.

artificial synapse with memristive devices should have an analog-type resistance change to emulate synaptic behavior more precisely.

A few studies have been reported on the analog resistive switching of metal oxide layers. For example, Jo et al demonstrated a memristive device with a gradually changing resistance in the mixed layer of Ag and Si as a result of Ag ionic redistribution in response to an applied voltage, and then applied the device for emulating synaptic behavior [3]. Li et al also demonstrated synaptic behavior in a Ag/polymer/ Ta system through Ag diffusion into the polymer layer [4]. Zhang et al reported the analog resistance change in Pt/ GeSO/TiN owing to the electrolyte function of GeS in GeSO and the synaptic behavior with analog resistance change [5]. In addition, Seo et al reported the analog synaptic behavior in an Al/TiO<sub>x</sub>/TiO<sub>y</sub>/W structure through the movement of oxygen between the  $TiO_v$  and  $TiO_x$  layers [6]. Also, we previously reported the analog resistance change in the np junction of an n-type Pt-Fe<sub>2</sub>O<sub>3</sub> core-shell nanoparticle assembly on a p-Si substrate where the electrical charging at nanoparticles altered a built-in potential barrier [7]. In addition, we demonstrated the memristor ratioed logic-based NAND operation using analog  $Ag/Fe_2O_3$  nanoparticle assembly/Pt memristors in series with a CMOS inverter [8]. Although these studies demonstrated the analog resistance change in memristive devices, it remains a challenge to realize highly reliable analog memristive devices with a strong resistance change for artificial synapses.

Among various metal oxides exhibiting the resistance change, ceria  $(CeO_2)$  is thought to be a good candidate for analog switching elements. In principle, the resistive switching in resistive random access memory (ReRAM) associates the reversible formation and rupture of conducting filaments or modulation of the electrode/oxide interface for digital-type resistance change [9, 10]. These phenomena involve the migration of oxygen ions (and vacancies) within the oxide or between the electrode and the oxide, which is hard to control precisely. In particular, it is more difficult to control the redistribution ions and vacancies for the analog switching without abrupt change of state. Considering these circumstances, CeO<sub>2</sub> could be a promising analog switching element because it is a good electrolyte of oxygen ions [15]. Also,  $CeO_2$  has variable valence states of Ce cations ( $Ce^{3+}$  and  $Ce^{4+}$ ), which is likely to be modulated by the applied voltage. Thus, it is expected that the resistance of a CeO<sub>2</sub> layer would be modulated in an analog fashion by controlling the distribution of oxygen ions and variable Ce cations.

Several research groups have demonstrated the digitaltype resistance change for ReRAM application with a CeO<sub>2</sub> layer [16–20]. Sun *et al* reported the bipolar switching in an Al/CeO<sub>x</sub>/Pt structure with multilevel resistance states by the formation and rupture of a filament consisting of oxygen vacancies through the valence change between Ce<sup>3+</sup> and Ce<sup>4+</sup> [16]. Also, Younis *et al* proposed the switching mechanism determined by the number of oxygen vacancies in a Au/CeO<sub>2</sub>/ITO structure [17]. Hsieh *et al* [18] and Ismail *et al* [19] also reported the bipolar switching in Al/CeO<sub>2</sub>/Au and Zr/CeO<sub>x</sub>/Pt structures, respectively. Also, Lin *et al* reported the unipolar switching of a polycrystalline CeO<sub>2</sub> layer in a Pt/CeO<sub>2</sub>/Pt structure [20]. However, the analog switching with a CeO<sub>2</sub> layer has not been reported yet.

In this study, we demonstrated analog-type memristive switching characteristics with a strong resistance change by orders of magnitude in a  $Pt/CeO_2/Pt$  device structure. In addition, while the  $Pt/CeO_2/Pt$  device has a symmetric structure with the same Pt top and bottom electrodes, it exhibited the polarity-dependent and asymmetric diode-type resistive switching and emulated synaptic behaviors such as potentiation and depression. Its detailed switching characteristics for artificial synapses will be discussed in detail.

#### 2. Experimental section

The 50 nm-thick CeO<sub>2</sub> layer was deposited on a Pt bottom electrode on top of a Ti/SiO<sub>2</sub>/Si substrate by rf magnetron sputtering with a CeO<sub>2</sub> target in Ar ambient. Then, a CeO<sub>2</sub>/Pt structure was annealed at 600 °C for 1 h in air. The stoichiometry of CeO<sub>2</sub> layer was confirmed using Rutherford backscattering spectroscopy (RBS, NEC pelletron 6SDH-2). The chemical bonding states in CeO<sub>2</sub> layers were also examined by x-ray photoelectron spectroscopy (XPS, AXIS-HSi (KRATOS)). On top of the CeO<sub>2</sub> layer, a Pt top electrode

was deposited by e-beam evaporation with a diameter of  $\sim 100 \ \mu m$  using a shadow mask. The microstructure, chemical composition, and valence state of Ce cations in the Pt/CeO<sub>2</sub>/Pt structure were analyzed using cross-sectional transmission electron microscopy (TEM, JEM2100F) with energy-dispersive spectroscopy (EDS) and electron energy loss spectroscopy (EELS). The current–voltage (*I–V*) measurements by voltage sweep and pulse on the Pt/CeO<sub>2</sub>/Pt devices were performed using Agilent 4156B semiconductor parameter analyzers with an Agilent 41501B pulse generator. The voltage was applied at the top Pt electrode while the bottom Pt electrode was kept grounded.

#### 3. Results and discussion

Figures 1(a) and (b) shows the RBS spectra of non-annealed and 600 °C-annealed CeO<sub>2</sub> layers on a Si substrate, respectively. Because of overlapping peak positions of the Ce and Pt electrode, the RBS analysis to measure the stoichiometry of CeO<sub>2</sub> layer was carried out using the CeO<sub>2</sub> layer deposited on the Si substrate. The spectra of both non-annealed and annealed CeO<sub>2</sub> layers show a stoichiometry simulated to be Ce<sub>0.84~0.87</sub>O<sub>2</sub>. Since there is no stable phase with higher oxygen content than CeO<sub>2</sub> in a Ce–O system [21], the deposited layer is regarded to be almost a stoichiometric CeO<sub>2</sub> phase with some excess oxygen atoms in the grain boundaries or other defect sites.

Figure 2 shows the XPS spectra of O 1s and Ce 3d levels of non-annealed and annealed CeO<sub>2</sub> layers on the Pt bottom electrode. The XPS spectra were obtained from the surface of the CeO<sub>2</sub> layers without etching the surface because the layers would be damaged through the ion beam irradiation etch changing the valence state of Ce cations [22]. The peaks were calibrated with the C1s peak at 284.5 eV. The O 1s spectra of both layers in figure 2(a) show the main peak at 528.9 eV assigned to the lattice oxygen in  $CeO_2$  [19, 23]. The lattice oxygen peaks bound to  $Ce^{3+}$  and  $Ce^{4+}$  were not separately observed due to the negligible difference of binding energies [23]. Also, the higher energy peaks were observed at 529.5 and 531.1 eV due to the presence of defects such as nonlattice oxygen and oxygen vacancies [19]. It indicates that the CeO<sub>2</sub> layers have oxygen-related defects even after annealing. The peaks for surface chemisorbed oxygen and a hydroxyl group observed around at 531.3-531.9 eV and 532.7-533.5 eV, respectively [24], were not clearly found. The Ce 3d spectra in figure 2(b) indicate that  $Ce^{4+}$  and  $Ce^{3+}$  cations coexisted in both non-annealed and annealed CeO2 layers. Nevertheless, the peaks corresponding to Ce<sup>4+</sup> ions lined with blue color at 881.8  $(\nu)$ , 888.9  $(\nu'')$ , 897.8  $(\nu''')$ , 900.3 (u), 907.1 (u''), and 916.1 eV (u''') had a higher intensity than the other peaks to  $Ce^{3+}$  ions in red color (879.9 ( $\nu_0$ ), 884.7 ( $\nu'$ ), 898.6 ( $u_0$ ), and 903.2 eV (u'). The notation of u and v refers to the  $3d_{5/2}$  and  $3d_{3/2}$  spin-orbit components, respectively [23]. The six peaks for  $Ce^{4+}$  consist of three spin-orbit doubles, where the peaks of u''' and v''' result from a Ce  $3d^9$  O  $2p^6$  Ce  $4f^0$  final state and the peaks of u, v, u'', and  $\nu''$  come from a mixture of Ce 3d<sup>9</sup> O 2p<sup>5</sup> Ce 4f<sup>1</sup> and Ce 3d<sup>9</sup>  $O 2p^4 Ce 4f^2$  final states. Also the peaks for  $Ce^{3+}$  consist of two



**Figure 2.** XPS spectra of (a) O 1s and (b) Ce 3d levels of nonannealed and 600  $^{\circ}$ C-annealed CeO<sub>2</sub> layers.

pairs of doublets where  $u_0/v_0$  and  $u'/\nu'$  correspond to a mixture of Ce 3d<sup>9</sup> O 2p<sup>6</sup> Ce 4f<sup>1</sup> and Ce 3d<sup>9</sup> O 2p<sup>5</sup> Ce 4f<sup>2</sup> final states [23]. It implies that most Ce ions were Ce<sup>4+</sup> composing CeO<sub>2</sub>. Since the stoichiometric CeO<sub>2</sub> layer was verified by RBS spectra, some Ce<sup>3+</sup> cations and defective oxygen anions are thought to be randomly distributed. It was found that the ratio of Ce<sup>4+</sup> to Ce<sup>3+</sup> was not increased but rather decreased after annealing, which was the opposite tendency of reoxidation of Ce<sup>3+</sup> to Ce<sup>4+</sup> by annealing in an oxygen environment [25], whose origin is not clear yet.

In addition, the microstructure, crystal phase, and local stoichiometry of the annealed CeO<sub>2</sub> layer were confirmed using cross-sectional TEM analysis. Figure 3(a) reveals the crystalline structure of the CeO<sub>2</sub> layer with lattice images and Moiré fringes coming from the interference between projected crystalline grains. Also, it verifies that there is no perceptible interfacial layer between the CeO<sub>2</sub> and Pt electrodes. The EDS analysis in TEM with a compositional line scan in figure 3(b) also confirms the stoichiometry of CeO<sub>2</sub> without any interfacial layers. The O/Ce ratio was  $\sim$ 2 through the entire layer without apparent deviation. The selected area diffraction patterns (SADP) shown in figure 3(c) confirm that the CeO<sub>2</sub> layer has a crystalline fluorite cubic structure (JCPDS 43-1002).

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**Figure 3.** (a) Cross-sectional TEM micrographs, (b) composition by EDS line scan, and (c) SADP of the  $Pt/CeO_2/Pt$  device.



**Figure 4.** Semilogarithmic *I*–*V* curves in repeated voltage sweeps in the following orders: (a) positive voltage sweeps first: (1)  $0 \rightarrow +7 \rightarrow 0$  V ten times, (2)  $0 \rightarrow -7 \rightarrow 0$  V ten times, (3)  $0 \rightarrow +7 \rightarrow 0$  V ten times, and finally (4)  $0 \rightarrow -7 \rightarrow 0$  V ten times, (b) negative voltage sweeps first: (1)  $0 \rightarrow -7 \rightarrow 0$  V ten times, (2)  $0 \rightarrow +7 \rightarrow 0$  V ten times, (3)  $0 \rightarrow -7 \rightarrow 0$  V ten times, and finally (4)  $0 \rightarrow -7 \rightarrow 0$  V ten times, (2)  $0 \rightarrow +7 \rightarrow 0$  V ten times, (3)  $0 \rightarrow -7 \rightarrow 0$  V ten times, and finally (4)  $0 \rightarrow +7 \rightarrow 0$  V ten times.

Although the Pt/CeO<sub>2</sub>/Pt device had almost symmetric stoichiometry, microstructure, and top and bottom interfaces, it showed the polarity-dependent and asymmetric resistive switching characteristics. Figure 4(a) shows the semilogarithmic I-V curves by voltage sweeps in the following order of positive biasing first: (1)  $0 \rightarrow +7 \rightarrow 0$  V ten times, (2)  $0 \rightarrow -7 \rightarrow 0$  V ten times, (3)  $0 \rightarrow +7 \rightarrow 0$  V ten times, and finally (4)  $0 \rightarrow -7 \rightarrow 0$  V ten times. Figure 4(b) shows the opposite, with the curves in the order of negative biasing first: (1)  $0 \rightarrow -7 \rightarrow 0$  V ten times, (2)  $0 \rightarrow +7 \rightarrow 0$  V ten times, (3)  $0 \rightarrow -7 \rightarrow 0$  V ten times, and finally (4)  $0 \rightarrow +7 \rightarrow 0$  V ten times. The polarity-dependent and asymmetric resistive switching characteristics were clearly observed. In the positive biasing first condition (figure 4(a)), the current was sequentially increased in an analog fashion as repeating +V sweeps ten times, while it was gradually decreased back as subsequently repeating -V sweeps. Also, the current level at +7 V was in the range of  $10^{-5}$  A, which was higher than that



**Figure 5.** Semilogarithmic *I*–V curves in the voltage sweep (a)  $0 \rightarrow +V \rightarrow -V \rightarrow 0 V$  with increasing sweep voltage from  $\pm 3$  to  $\pm 9$  in sequence and (b) repeated sweep  $0 \rightarrow +3 \sim +10 \rightarrow 0 V$  and subsequent  $0 \rightarrow -3 \sim -10 \rightarrow 0 V$ .

in the range of  $10^{-6}$  A at -7 V, showing asymmetric diodetype characteristics. For the reverse, repeating +V sweeps increased the current again, and vice versa as repeating -Vsweeps. In the order of negative biasing first (figure 4(b)), however, the current was increased at the first sweep and then remained almost the same during the repeated -V sweeps. However, the current was continuously increased as repeating +V sweeps. After that, the tendency of decreasing current at -V and increasing current at +V was consistently observed as similar to the curves in figure 4(a). In both cases, the current was increased during the first sweep, implying that the device was initially highly resistive irrespective of the bias polarity.

The reversible and analog resistance change could be controlled by the amplitude of the repeated sweep voltage. Figure 5(a) are the semilogarithmic I-V curves formed by repeatedly sweeping  $0 \rightarrow +V \rightarrow -V \rightarrow 0V$  with increasing sweep voltage from  $\pm 3$  to  $\pm 9$  in sequence. It is observed that the current was increased after +V sweeps and it was reversibly decreased back after -V sweeps. The increase of current, i.e. resistance change, was enhanced with the increase of +V sweep amplitude. The current at +2V was increased from 0.29 to 1.46 nA after the +3V sweep. And it was



Figure 6. Second-derivative EELS spectra at Ce  $M_4$  and  $M_5$  edges through the CeO<sub>2</sub> layer in Pt/CeO<sub>2</sub>/Pt.

increased further from 3.39 nA to 5.57  $\mu$ A by three orders of magnitude after the +9 V sweep. Also, the current was sequentially increased by repeatedly increasing +V sweep amplitude and vice versa by repeating the sweep with increased -V as shown in figure 5(b). Repeating sweeps with the increase of voltage from -3 to -10 V led to a gradual decrease of current by almost three orders of magnitude.

The *I*–*V* curves in the voltage sweep condition demonstrated clearly the analog resistance change with respect to the repetition of voltage sweep with a ratio >10<sup>5</sup>. Also, the *I*–*V* curves had the asymmetric rectifying characteristics with higher current at +V by an order of magnitude than that at –V. In addition, they revealed the polarity-dependent resistance change that the current was increased as repeating +V application and vice versa as –V application. It implies that the Pt/CeO<sub>2</sub>/Pt structure is electrically asymmetric and nonuniform despite the symmetric Pt/CeO<sub>2</sub>/Pt structure having almost identical stoichiometry and structure through the entire CeO<sub>2</sub> layer.

Similar rectifying characteristics were reported by Yoon *et al* [26] and Kim *et al* [27] in  $Pt/Ta_2O_5/HfO_x/Ti$  and  $Pt/NbO_x/TiO_y/NbO_x/TiN$  structures, respectively, where different Schottky barriers between the top and bottom interfaces led to the rectifying *I*–*V* characteristics. In contrast, the structure of  $Pt/CeO_2/Pt$  in this study is symmetric with both top and bottom  $Pt/CeO_2$  interfaces, so the Schottky barriers would be identical unless they were altered by the defects near the interfaces, which will be discussed later.

To verify the origin of asymmetric *I*–*V* characteristics, the valence state of Ce cations through the layer was characterized using EELS for correlating their distribution with asymmetrical electrical characteristics. Figure 6 shows second-derivative EELS spectra at  $M_4 (3d_{3/2} \rightarrow 4f_{5/2})$  and  $M_5 (3d_{5/2} \rightarrow 4f_{7/2})$  edges of Ce through the layer from the top to bottom interface, averaged after dividing the layer by five regions in depth. The second-derivative EELS spectra show the characteristic  $M_4$  line around at ~892 eV and  $M_5$  at ~874.6 eV, not exactly the same as the reported values due to the shift during zero energy loss calibration but exhibiting the similar value of spin–orbit splitting with ~18 eV [28–30].



**Figure 7.** Replot of I-V in figure 5(b) with the form of Schottky conduction at (a) +V and (b) -V range, and SCLC at (c) +V and (d) -V range.

The larger is the ratio of  $M_4/M_5$  peak areas in the secondderivative spectra sensitive to the valence state of Ce cations, the higher is the Ce<sup>4+</sup> cation concentration in the layer [28–30]. Fortner *et al* reported that Ce(III) orthophosphate and Ce(IV) in CeO<sub>2</sub> have the  $M_4/M_5$  values of 0.78 and 1.1, respectively [28]. Referring to these values, the difference of Ce<sup>3+</sup> and Ce<sup>4+</sup> cation density was examined through the depth of CeO<sub>2</sub> layer. The  $M_4/M_5$  values are similar through the entire layer from the top to bottom interface, ranging from 0.89 and 0.98. Therefore, it is hard to conclude that asymmetric *I–V* characteristics were caused by a dissimilar density of multivalent Ce cations through the layer.

Even with an uncertain distribution of multivalent Ce states at the top and bottom interfaces, the conduction mode analysis discloses an apparent dissimilarity that might come from asymmetric interfaces. The *I*–*V* curves in figure 5(b) could roughly fit with Schottky conduction  $(\log(I) \propto V^{0.5})$  and space–charge limited conduction (SCLC,  $I \propto V^n$ ) as shown in figure 7. In this analog resistance change condition, the resistance was instantly changing during the voltage sweep, so the *I*–*V* curves could not fit perfectly in a linear form through the entire sweep voltage range. They did not fit with other

conduction modes such as Fowler-Nordheim tunneling, Poole-Frenkel conduction, and hopping conduction. The Schottky conduction and SCLC are influenced by the presence of defects. For example, the Schottky barrier height in the ideal case, presented by the *y*-intercept in  $\log(I)-V^{1/2}$  curves, is equal to the energy difference between the work function of Pt and electron affinity of CeO<sub>2</sub>. However, the Schottky barrier in actual cases is significantly affected by the presence of interface state pinning the Fermi level [31]. It implies that the top and bottom Pt/CeO<sub>2</sub> interfaces could have different Schottky barriers if they have different densities of interface and defect states, which could be caused by the deposition processing sequence that the top Pt electrode was finally deposited on the CeO<sub>2</sub> layer while the bottom Pt electrode experienced the deposition of CeO<sub>2</sub>. Similarly, Lee et al reported asymmetric current levels with respect to the voltage polarity in a Pt/(Ba,Sr)TiO<sub>3</sub>/Pt structure, which was attributed to different Schottky barrier heights between the top and bottom interfaces caused by dissimilar interface state density depending on the processing condition [32]. Also, Mojarad et al reported the asymmetric current at Pt/SrTiO<sub>3</sub>/Pt due to the internal field by

fixed charges only at the bottom electrode, though their origin was not clear [33].

Assuming the circumstance of having different densities of interface state, the higher current at +V could be interpreted by an effectively lower Schottky barrier at the bottom interface. Then, the polarity-dependent resistance change could also be associated with Schottky barrier modulation through Fermi level pinning by filling these traps. The application of +V injects a considerable amount of electrons from the bottom Pt electrode and fills more interface states, lifting up the Fermi level. As a result, the Schottky barrier is decreased and subsequently the current is increased as repeating the +V application. Also, the SCLC current through the insulator with trap states is proportional to the fraction of electrons in the conduction band as to be equilibrated with the fraction in trap states as shown in figures 7(c) and (d) [34]. As the traps are filled by electrons by repeated +V application, the fraction of electrons in the conduction band to those in the trap state is increased and consequently increases the SCLC current. Besides the contribution of electrical charging on resistive switching, the valence change of Ce cations along with redistribution of oxygen vacancies, which is commonly observed in CeO<sub>2</sub>, would cause the resistive switching. Injected electrons from the bottom Pt electrode when applying +V reduces CeO<sub>2</sub> to Ce<sub>2</sub>O<sub>3</sub> through the reaction  $2\text{CeO}_2 \rightarrow \text{Ce}_2\text{O}_3 + 1/2\text{O}_2 + \text{V}_{\text{O}}$  [17] and generates more  $\text{V}_{\text{O}}$ as n-type dopants of  $CeO_2$  [35], thereby reducing the resistance. The oxygen molecules or ions may remain inside the  $CeO_2$ layer because of the negligible oxygen solubility of oxygen in Pt [36]. The same phenomena of Schottky barrier reduction at the top interface, increased fraction of electrons in the conduction band in SCLC, and the reduction of CeO<sub>2</sub> should have also occurred when applying -V in the symmetric Pt/CeO<sub>2</sub>/Pt structure. However, counter to this the resistance was increased as applying -V. It means that the proposed models could not explain the characteristics at -V, where the reason is not identified. As discussed above, the CeO2 layer has complicated characteristics to have a substantial defect density, tends to undergo the conversion of Ce valence states, and has oxygen vacancies as an n-type dopant with high ionic conductivity. So, the discussion on the mechanism is just hypothetical at this stage and it is not conclusive yet what causes the rectifying I-Vcharacteristics and polarity-dependent analog resistive switching. A further investigation, for example, by altering the stoichiometry and defect density of CeO<sub>2</sub>, employing asymmetric structure with CeO<sub>2</sub> layer, etc, needs to be followed to clarify the mechanism.

Figure 8(a) exhibits the gradual and sequential increase of current measured at a read voltage of +2 V after repeating the pulses with the amplitude of +10 V and the width of 20 ms for 100 times. It presented the analog transition from a high to low resistance state with a ratio  $>10^5$ . This resistance change is surprisingly strong compared to previously reported values. As a reversible switching, the low resistance state returned back to a high resistance state by successively repeating -10 V pulses with a width of 1, 10, and 100 ms for 50 times, respectively. The current at a read voltage of +2 V without high voltage pulsing remained in the range of  $10^{-10}$  A (not shown here), implying the read disturbance was



**Figure 8.** Read current change after repeating (a) +10 V pulses with the width of 20 ms for a hundred times and successive -10 V pulses with the width of 1, 10, and 100 ms for 50 times, (b) pulses of increased  $\pm$ V at the fixed width, and (c) pulses of fixed  $\pm$ 10 V with varied width.

negligible. This analog decrease and increase of resistance emulates the potentiation and depression of synaptic behavior, respectively. Notably, the strongly modulated resistance change ranging from  $\sim 1 \text{ M}\Omega$  to 200 G $\Omega$  enables the artificial synapse to have a wide range of synaptic weight states for signal processing and learning/memory functions.



Figure 9. Retention for long-term memory stability after repeated pulsing +10 V for 10 ms.

The current change could be controlled by voltage pulse amplitude and width as shown in figures 8(b) and (c), respectively. The current was measured at +2 V read voltage after high voltage pulsing for 30 times. At the fixed pulse width of 10 ms, the current at the low resistance state was increased from  $\sim$ 20 to 100 nA with the increase of pulse amplitude from +7 to +10 V (figure 8(b)). Similarly, the current was increased from  $\sim$ 10 to 170 nA with the increase of pulse width from 1 to 50 ms at the fixed pulse amplitude of +10 V (figure 8(c)). In both cases, the high resistance state was reversibly obtained by applying -V pulses.

Figure 9 exhibits the retention to assess short-term or longterm memory of synapses after pulsing operation. After the current was increased tens of times by +V potentiation pulsing, it was decreased with time presenting the memory loss. It was decreased most during the first 30 s and then decreased more slowly. Nevertheless, the current was still four or five times higher than the initial value after 10 min. This is superior or comparable to the retention of short-term memory of biological systems (e.g. the human brain) acting for temporary recall of information during the process, which generally lasts from seconds to tens of minutes [37, 38]. A better retention is required for long-term memory operation. The memory loss in this system is thought to be caused by unstable electrical charging or recovery of Ce<sup>3+</sup> to Ce<sup>4+</sup> and consequent annihilation of oxygen vacancies through recombination with oxygen ions. In order to prohibit this recombination, the oxygen ions should be instantly removed to the Pt electrode. The detailed mechanism of memory loss and improvement of retention properties are under investigation.

# 4. Conclusion

The analog memristive switching with a strong resistance change with a ratio  $>10^5$  was demonstrated with a Pt/CeO<sub>2</sub>/Pt device structure. The *I*–*V* characteristics showed the polarity-dependent and asymmetric diode-type resistive

switching. The sequentially decreasing resistance at +V application emulated the synaptic potentiation and the increasing resistance at -V did the depression motion of biological synapse. In particular, the potentiation and depression motions were modulated by voltage pulses, exhibiting the resistance change ranging from a few  $\mbox{M}\Omega$  to hundreds of  $G\Omega$  with respect to the number, amplitude and width of pulsing. The strong analog memristive switching realized the wide range of synaptic weight states for signal processing and learning/memory functions. The analyses of stoichiometry and chemical bonding states using RBS, XPS, EDS, and EELS revealed that CeO<sub>2</sub> layers have mixed multivalent Ce<sup>3+</sup> and Ce<sup>4+</sup> cations. From the conduction mode analyses, it is probable that the Schottky barrier and space charge density were modulated with respect to the applied voltage through the charge trapping and detrapping that altered the barrier height and SCLC current. Also, the possible valence change of Ce cations associating the change of oxygen vacancy concentration would lead to the polaritydependent analog resistance change. These results demonstrated the potential of CeO<sub>2</sub> memristive switching for the application to artificial synaptic devices.

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