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Comprehensive separate extraction of parasitic resistances in MOSFETs considering the gate bias-dependence and the asymmetric overlap length

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ABSTRACT

Parasitic resistances cause degradation of transconductance (g_m), cutoff frequency (f_T), current driving capability, and long term reliability of MOSFETs. We report a comprehensive extraction of parasitic resistance components in MOSFETs for the contact, the spreading current path, and the lightly doped drain region caused by the process, structure, and degradation. We considered the gate bias (V_{GS})-dependence and the asymmetric overlap length ($L_{ov,SD}$) in the source and drain. We report systematically integrated extraction technique combined with the channel resistance method, the transfer length method, the dual-sweep combinational transconductance technique, the open drain method, and the parasitic junction current method. V_{GS}-independent resistances were separated to be R_{Se} = 6.8–6.9 Ω, R_{De} = 7.4–7.5 Ω, R_{SUB} = 7.4–7.6 Ω, R_{So} = 1.8–2.1 Ω, and R_{Do} = 3.2–3.5 Ω for MOSFETs with and at W/L = 50 μm/0.27 μm. V_{GS}-dependent intrinsic resistances are obtained to be R_{Si} = 1.9–4.4 Ω, R_{Di} = 1.4–3.2 Ω for the same devices. The V_{GS}-dependent intrinsic channel resistance (R_{CH}) is extracted with different channel lengths for MOSFETs with L = 0.18 μm/0.27 μm/0.36 μm.

1. Introduction

With scaling down of MOSFETs for improved performance and integration density in CMOS circuits and systems, a comprehensive separation of parasitic resistances is very important [1–5]. In scaled MOSFETs as schematically shown in Fig. 1, parasitic resistance components are indispensable due to the limited conductivity of the material, fabrication process, layout, and degradation by electrical stress during the operation. They cause voltage drops across parasitic resistances and result in a degradation of the transconductance (g_m), the current driving capability, the current gain cut-off frequency (f_T), the noise figure, and other performance parameters [6–8]. Therefore, a comprehensive and separate extraction of parasitic resistance components, fully considering the gate bias-dependence and the asymmetry of the source/drain, is very important for a robust implementation of fabrication process and systematic characterization of degradation mechanisms through accurate modeling and comprehensive extraction of characteristic parameters in MOSFETs. Although extraction techniques for separation of parasitic resistances in MOSFETs were reported [9–11], the gate bias-dependence (V_{GS}) and/or structural asymmetry in the source and drain had not been fully considered in the previous works. Otherwise, each characterization technique has not been fully combined together working independently.

In this work, therefore, we report a systematic combinational technique and provide a comprehensive separation result for the parasitic resistance components considering the V_{GS}-dependence and the possible asymmetry with the overlap length in MOSFETs. We also note that it is combined (I-V and C-V) technique overcoming any possible limit in the C-V-based technique through comprehensive I-V-based techniques. In previous works, the C-V (capacitance-voltage)-based characterization technique, which has limited applicability as an independent characterization technique for small size MOSFETs or requires a large size dummy MOS capacitor on the same wafer. In this work, we limited the C-V technique to the extraction of the overlap length in the source and drain. We also note that the asymmetry in the parasitic source and drain resistances (R_S and R_D) can be caused by the fabrication process, layout, and different degradation mechanism under bias. V_{GS}-dependence is also closely related to the long term degradation and reliability assessment of MOSFETs, CMOS integrated circuits, and systems.

First, for separation of V_{GS}-dependent intrinsic source ($R_{Si}(V_{GS})$) and drain resistances ($R_{Di}(V_{GS})$) originated from the lightly-doped region (LDD) to suppress the short channel effect, we obtain the overlap lengths in the source and drain ($L_{ov,S}$, $L_{ov,D}$) through the capacitance-voltage (C-V) curves. Then, we combine the transfer length method (TLM) with the channel resistance method (CRM) for the gate bias-

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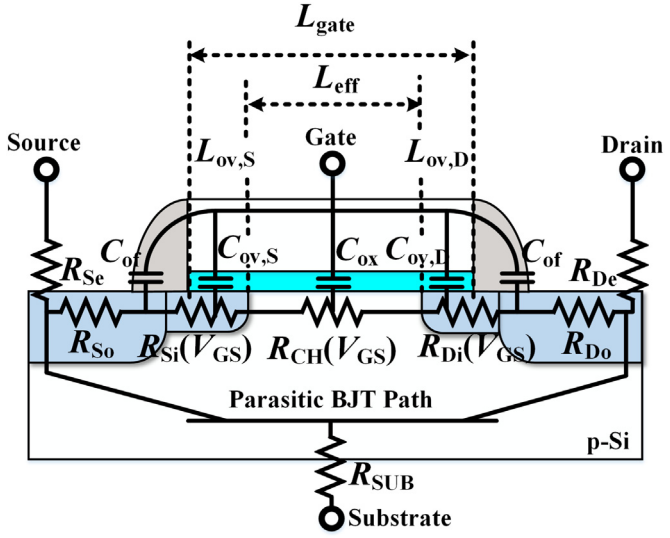

Fig. 1. Cross section of an n-channel MOSFET with an equivalent circuit for parasitic resistances and capacitances.

dependent channel resistance ($R_{CH}(V_{GS})$) [12–14]. In the next, V_{GS}-independent substrate resistance (R_{SUB}) and extrinsic source/drain resistances (R_{Se}/R_{De}) are extracted by the parasitic junction current method (PJCM) [15] combined with the open drain method (ODM) [16,17]. They are V_{GS}-independent and/or asymmetric components for the contact, the structural dependence, and hot-carrier effect as well as the fabrication process. In the next, the dual-sweep combinational transconductance technique (DSCT) is employed for extraction of the difference (R_D-R_S) between the source and drain resistances [18]. For extraction of V_{GS}-independent spreading resistance components (R_{So}, R_{Do}) as a following step, we combine the DSCT and the CRM with V_{GS}-dependent ($R_{Si}(V_{GS})$, $R_{Di}(V_{GS})$) and independent parasitic resistances (R_{Se}, R_{De}). Finally, we extract the intrinsic channel resistance (R_{CH}) as a function of the gate bias (V_{GS}) and the effective channel length (L_{eff}).

2. Fully electrical and analytical extraction of parasitic resistances

Equivalent circuit for n-channel MOSFETs with parasitic resistance components (R_{Se}, R_{So}, $R_{Si}(V_{GS})$, R_{De}, R_{Do}, $R_{Di}(V_{GS})$, R_{SUB}) is shown in Fig. 1. To separate parasitic resistance components in MOSFETs through a fully electrical comprehensive technique, we combined I-V and C-V methods described in Fig. 2. As indicated in Fig. 2, we

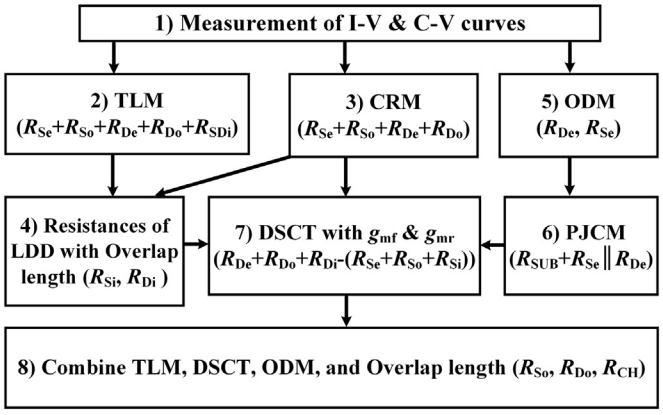

Fig. 2. Flow chart for the comprehensive extraction of parasitic resistance components in MOSFETs considering the gate-bias dependence, the overlap length, and any possible asymmetry.

extracted eight resistance components in MOSFETs considering the V_{GS}-dependence and any possible asymmetry over the operating bias range. For separate extraction of $R_{Si}(V_{GS})$ and $R_{Di}(V_{GS})$ for asymmetry caused by the fabrication process, layout, and the electrical stress during the operation, we combined the TLM and the CRM with the overlap lengths ($L_{ov,S}$, $L_{ov,D}$) obtained from the measurement of the capacitance-voltage (C-V) characteristics.

First, the V_{GS}-dependent total resistance (R_{tot}) is described as

$$R_{tot}(V_{GS}) \equiv 1/\frac{\partial I_{DS}}{\partial V_{DS}} = R_{Se} + R_{So} + R_{Si}(V_{GS}) + R_{De} + R_{Do} + R_{Di}(V_{GS}) + R_{CH}(V_{GS}) \quad (1)$$

$$R_{CH}(V_{GS}) = \frac{L_{eff}}{\mu_{eff} C_{ox} W (V_{GS} - V_T)} \quad (2)$$

$$R_{SDi}(V_{GS}) \equiv R_{Si}(V_{GS}) + R_{Di}(V_{GS}) = \frac{\Delta L_{ov,SD}}{\mu_{SD} C_{ox} W (V_{GS} - V_T)} \quad (3)$$

with $L_{eff}(\equiv L_{gate} - (L_{ov,S} + L_{ov,D}))$ as the effective channel length, V_T as the threshold voltage, C_{ox} ($=C_{ox}/t_{ox}$) as the oxide capacitance per unit area, $R_{Si}(V_{GS})(R_{Di}(V_{GS}))$ as the intrinsic source (drain) resistances, and $R_{CH}(V_{GS})$ as the V_{GS}-dependent intrinsic channel resistance. We define μ_{SD} and μ_{eff} as the bias-dependent effective mobilities in the lightly doped source/drain and the inverted channel region, respectively.

In the next, the metallic gate length (L_{gate}) is extracted to de-embed the intrinsic channel resistance ($R_{CH}(V_{GS})$) from the total resistance by the TLM through

$$R_{tot}|_{L_{gate}=L_{ov,SD}} = R_{Se} + R_{So} + R_{Si}(V_{GS}) + R_{De} + R_{Do} + R_{Di}(V_{GS}). \quad (4)$$

R_{Se}, R_{So}, R_{De}, and R_{Do}, normalized to the gate width (W) and contact area (A_c), are assumed to be the same in MOSFETs fabricated through the same fabrication process.

In the third, the sum of V_{GS}-independent components in R_S and R_D is extracted by the CRM through

$$R_{Si}(V_{GS}) + R_{Di}(V_{GS}) + R_{CH}(V_{GS})|_{V_{GS}\to\infty} \cong 0 \quad (5)$$

$$R_{tot}(V_{GS})|_{V_{GS}\to\infty} = R_{Se} + R_{So} + R_{De} + R_{Do} \quad (6)$$

with V_{GS}-dependent resistances ($R_{Si}(V_{GS})$, $R_{Di}(V_{GS})$, $R_{CH}(V_{GS})$) neglected when V_{GS} gets much larger than the threshold voltage (V_T). Combined with the previously extracted overlap lengths ($L_{ov,S}$, $L_{ov,D}$) in the source and drain, $R_{Si}(V_{GS})$ can be separated from $R_{Di}(V_{GS})$.

In Fig. 3(a), V_{GS}-dependent C-V curves are shown for 3 different gate lengths (L_{gate} = 0.18, 0.27, and 0.36 μm). The off-state minimum capacitance ($C_{min,S} = C_{ov,S} = C_{ox}WL_{ov,S}$, $C_{min,D} = C_{ov,D} = C_{ox}WL_{ov,D}$) under a large negative bias (strong accumulation state) in n-channel MOSFETs, much smaller than the flat band voltage (V_{GS}, $V_{GD} \ll V_{FB}$), is directly proportional to the overlap length ($L_{ov,S}$, $L_{ov,D}$). This allows us to have the gate-source capacitance $C_{gS}(V_{GS} \ll V_{FB}) = C_{ov,S}$ from the gate-source measurement configuration, the gate-drain capacitance $C_{gD}(V_{GD} \ll V_{FB}) = C_{ov,D}$ from the gate-drain measurement configuration, and the gate-source/drain capacitance $C_{gSD}(V_{GSD} \ll V_{FB}) = C_{ov,S} + C_{ov,D}$ from the gate-source/drain combined measurement configuration. Therefore, we note that V_{GS}-dependent L_{ov} can be extracted through the model described in [12].

We also note that V_{GS}-dependent intrinsic resistance components ($R_{Si}(V_{GS})$ and $R_{Di}(V_{GS})$) can be modeled as

$$R_{Si}(V_{GS}) = \frac{L_{ov,S}}{L_{ov,S} + L_{ov,D}} \times (R_{Si}(V_{GS}) + R_{Di}(V_{GS})) = R_{SDi}(V_{GS}) - R_{Di}(V_{GS}) \quad (7)$$

$$R_{Di}(V_{GS}) = \frac{L_{ov,D}}{L_{ov,S} + L_{ov,D}} \times (R_{Si}(V_{GS}) + R_{Di}(V_{GS})) = R_{SDi}(V_{GS}) - R_{Si}(V_{GS}). \quad (8)$$

Therefore, by combining the CRM and the TLM,

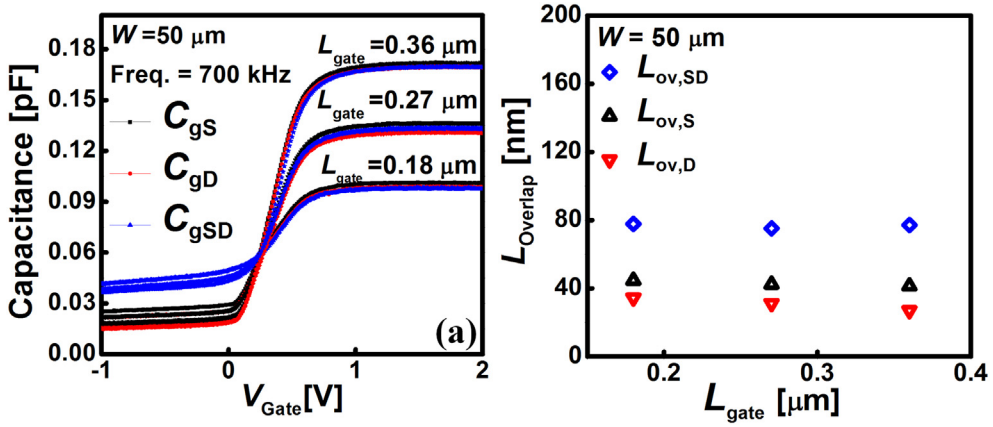

Fig. 3. (a) Measured C-V characteristics of $C_{gS}(V_{GS})$, $C_{gD}(V_{GD})$, and $C_{gSD}(V_{GSD})$ with W/L = 50 μm/0.18 μm, 50 μm/0.27 μm, and 50 μm/0.36 μm in n-channel MOSFETs. (b) Overlap lengths obtained by the C-V curves with different gate lengths.

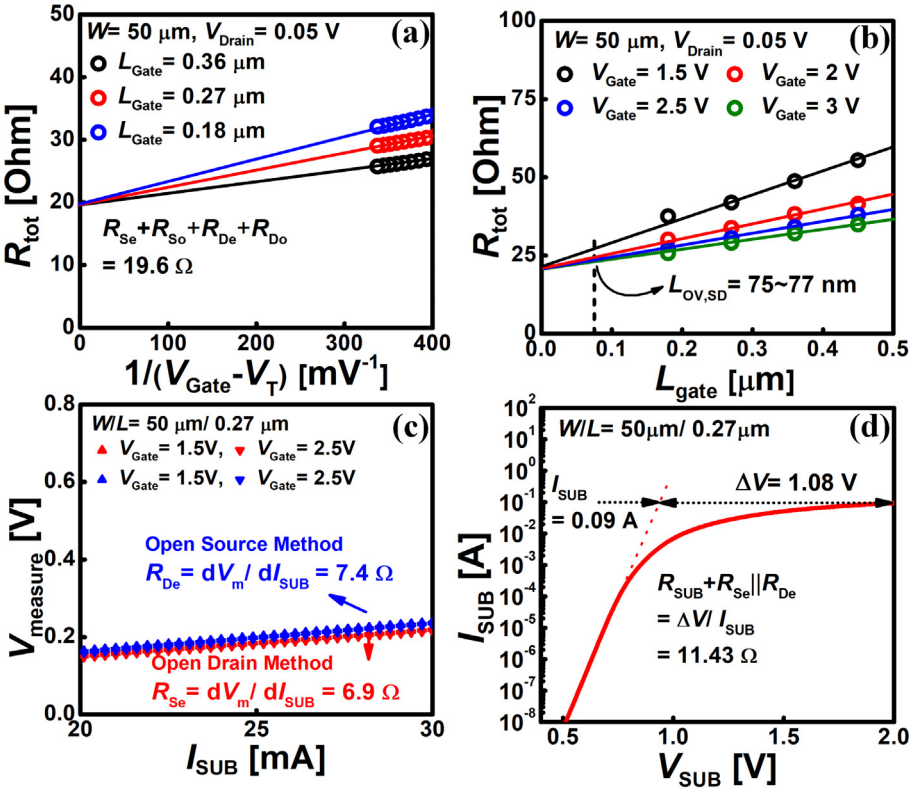

Fig. 4. (a) Measured $R_{tot}(V_{GS})$ as a function of $V_{GS}(\gg V_T)$. V_{GS}-dependent resistances go to zero due to enhanced conductivity of the channel under high gate bias. (b) The sum of parasitic S/D resistances without $R_{CH}(V_{GS})$ is extrapolated to be R_{tot} for MOSFETs with $L_{gate} = L_{ov,SD}$. (c) Measured V_{GS}-independent parasitic resistance with the ODM. (d) Measured R_{SUB} through the PJCM with a parasFitic BJT in MOSFETs.

$R_{SDi}(V_{GS}) = R_{Si}(V_{GS}) + R_{Di}(V_{GS})$ is obtained and it is separated into $R_{Si}(V_{GS})$ and $R_{Di}(V_{GS})$ in proportion to $L_{ov,S}$ and $L_{ov,D}$. As shown in Fig. 3(b), the overlap length ($L_{ov,S}$, $L_{ov,D}$, $L_{ov,SD}$) is extracted from the C-V curves in MOSFETs with different gate lengths. As expected, the overlap length is observed to be identical in MOSFETs even with different gate lengths on the same wafer fabricated through the same fabrication process.

For V_{GS}-independent extrinsic components (R_{Se}, R_{De}) as a next step, the open drain method (ODM) [17] was adopted for the n^+ source-p substrate-n^+ drain modeling as a parasitic npn bipolar junction transistors (BJT) shown in Fig. 1. We note that the Ebers-Moll model for the BJT allows us to describe the drain voltage as a function of the drain current and parasitic resistances as

$$V_{DS} = V_{th} \ln\left[\frac{I_{SUB} + I_D(1-\alpha_R)}{\alpha_R\,[I_{SUB} + I_D(1-\alpha_F)/\alpha_F]}\right] + R_{Se}(I_{SUB} + I_D) + R_{De} I_D \quad (9)$$

with V_{th} as the thermal voltage ($V_{th} = kT/q$), $\alpha_F(\alpha_R)$ as the forward (reverse) common-base current gain of the parasitic BJT. Therefore, from the measured drain voltage (V_{DS}) with the open-drain configuration, we obtain

$$R_{Se} = \left.\frac{\partial V_{DS}}{\partial I_{SUB}}\right|_{\substack{I_{DS}\to 0 \\ \text{open-drain}}} \quad (10\text{-}1)$$

$$R_{De} = \left.\frac{\partial V_{SD}}{\partial I_{SUB}}\right|_{\substack{I_{SD}\to 0 \\ \text{open-source}}} . \quad (10\text{-}2)$$

For the substrate resistance (R_{SUB}) in MOSFETs with the body contact, we employed the parasitic junction current method (PJCM) [15]. We note that, however, the parasitic junction current method (PJCM) can be only applied to MOSFETs with the body contact. As far as there is a body contact in field effect transistors (FETs) with insulated

Table 1
Gate bias-dependent and independent parasitic S/D resistances in n-channel MOSFETs with various gate lengths.

V_{Gate} [V]	R_{SUB} [Ω]	R_{Se} [Ω]	R_{De} [Ω]	R_{So} [Ω]	R_{Do} [Ω]	$R_{S,ext}$ [Ω]	$R_{D,ext}$ [Ω]	R_{Si} [Ω]	R_{Di} [Ω]	R_{CH} [Ω]
W/L = 50 μm/0.18 μm										
1.5	7.4	6.8	7.4	1.9	3.5	8.7	10.9	4.4	3.2	10.3
2				2.0	3.4	8.8	10.8	2.8	2.1	5.6
2.5				2.1	3.3	8.9	10.7	2.2	1.6	3.6
3				2.0	3.4	8.8	10.8	1.9	1.4	2.8
W/L = 50 μm/0.27 μm										
1.5	7.6	6.9	7.4	1.8	3.5	8.7	10.9	4.4	3.2	14.7
2				1.9	3.4	8.8	10.8	2.8	2.1	9.3
2.5				2.0	3.3	8.9	10.7	2.2	1.6	7.1
3				1.9	3.4	8.8	10.8	1.9	1.4	6.1
W/L = 50 μm/0.36 μm										
1.5	7.6	6.9	7.5	1.8	3.4	8.7	10.9	4.4	3.2	21.5
2				1.9	3.3	8.8	10.8	2.8	2.1	13.8
2.5				2.0	3.2	8.9	10.7	2.2	1.6	10.6
3				1.9	3.3	8.8	10.8	1.9	1.4	9.1

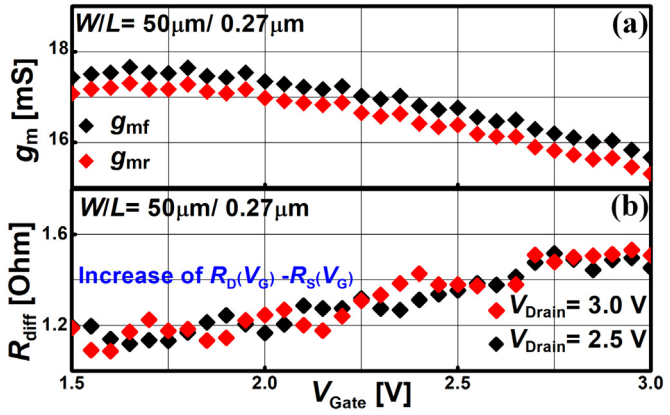

Fig. 5. (a) Transconductances extracted by the forward and reverse mode configuration transfer curves as a function of V_{GS} (b) Measured $R_{diff}(=R_D - R_S)$ obtained by the DSCT.

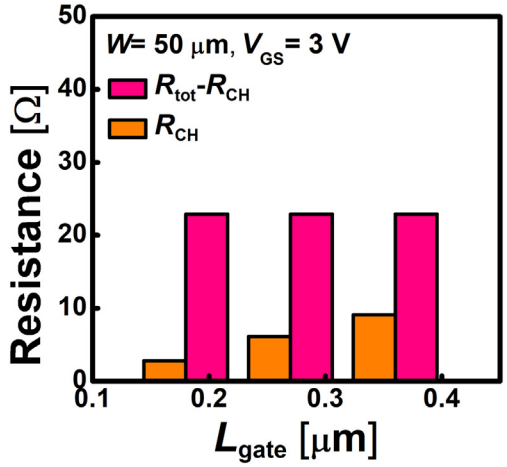

Fig. 6. Plot of R_{CH} and R_{tot}- R_{CH} $(=R_S + R_D + R_{CH})$ with stack column at V_{GS} = 3 V. R_{CH} is proportional to L_{eff} and R_{tot}-R_{CH} has a constant value.

gate structure including conventional MOSFETs, silicon-on-insulator (SOI) MOSFETs, FinFETs, and thin-film transistors (TFTs), this technique can be applied too. However, this technique cannot be applied to FETs without the body contact.

Using the dual-sweep combinational transconductance technique (DSCT) [18–20], R_D-R_S is extracted by the combination of the forward (g_{mf}) and reverse (g_{mr}) transconductances in the saturation mode ($V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T = V_{DS,sat}$). We note that the saturation current (I_{DS}) for the forward mode (the source terminal works as the source and the drain terminal works as the drain in the operation) can be described as [18].

$$I_{DS} = \frac{\mu_{eff} C_{ox}}{2} \frac{W}{L} (V_{GS} - R_S I_{DS} - V_T)^2. \tag{11}$$

The extrinsic (g_{mf}) and intrinsic (g_{mo}) transconductances under forward mode configuration of characterization is obtained as a function of V_{GS} through

$$g_{mf}(V_{GS}) = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - R_S I_{DS} - V_T)\left(1 - \frac{\partial I_{DS}}{\partial V_{GS}} R_S\right) \tag{12}$$

$$g_{mo}(V_{GS}) = \frac{\partial I_{DS}}{\partial V_{GS,int}} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - R_S I_{DS} - V_T). \tag{13}$$

By rearranging Eqs. (12) and (13), $g_{mf}(V_{GS})$ considering the degradation by the source resistance (R_S) can be modeled as

$$g_{mf}(V_{GS}) = g_{mo}(1 - g_{mf} R_S) \& g_{mo} = \frac{g_{mf}}{1 - g_{mf} R_S}. \tag{14}$$

For the reverse mode configuration, by swapping the source with the drain (the source terminal works as the drain and the drain terminal works as the source in the operation), we obtain the reverse transconductance $g_{mr}(V_{GD})$ considering the degradation by the drain resistance (R_D) as

$$g_{mr}(V_{GD}) = g_{mo}(1 - g_{mr} R_D) \& g_{mo} = \frac{g_{mr}}{1 - g_{mr} R_D}. \tag{15}$$

$R_{diff} = R_D - R_S$, in the next, can be obtained by combining g_{mf} with g_{mr} through the DSCT method as

$$R_{diff}(V_{GS}) \equiv R_D - R_S = \frac{g_{mf} - g_{mr}}{g_{mr} g_{mr}} = R_{De} + R_{Do} + R_{Di}(V_{GS}) - (R_{Se} + R_{So} + R_{Si}(V_{GS})). \tag{16}$$

We note that the substrate/body effect caused by the parasitic source and drain resistances even with the body tied the source/drain in the characterization is neglected ($g_{bo} = \partial I_D / \partial V_{BS} = 0$, $V_{BS} = -I_D R_S$) in this work. If the voltage drop across the parasitic R_S and R_D is considerable due to a large parasitic resistance and/or high drain current during the characterization, the body effect can be included in the characterization [9].

In the next step for separate extraction of bias-independent R_{So} and R_{Do}, Eqs. (7), (8), (10-1), and (10-2) are combined with the CRM and the DSCT as

$$R_{So} = \frac{R_{tot}|_{CRM} - R_{tot}|_{DSCT} + R_{Di}(V_{GS}) - R_{Si}(V_{GS})}{2} - R_{Se} \quad (17)$$

$$R_{Do} = \frac{R_{tot}|_{CRM} + R_{tot}|_{DSCT} - R_{Di}(V_{GS}) + R_{Si}(V_{GS})}{2} - R_{De}. \quad (18)$$

3. Experimental results and discussion

For securing the comprehensive extraction of parasitic resistances and experimental verification of the combined characterization techniques, we employed n-channel MOSFETs with various gate lengths (L = 0.18, 0.27, 0.36 μm), W = 50 μm, and t_{ox} = 4.7 nm. The threshold voltage (V_T) and the subthreshold slope (SS) were extracted to be V_T = 0.55–0.56 V and SS = 102 mV/dec in MOSFETs employed in this work.

In Fig. 3(b), the overlap lengths ($L_{ov,SD}$) with different gate lengths are extracted to be the same as $L_{ov,SD}(=L_{ov,S} + L_{ov,D})$ = 75–77 nm. By the comprehensive combination of the CRM and the TLM with the experimentally obtained overlap lengths, the V_{GS}-dependent parasitic resistances (R_{Si}, R_{Di}) were extracted from Eqs. (7) and (8) as shown in Fig. 4(a)–(b) and Fig. 3(b). Through the ODM and the PJCM in the next step, the V_{GS}-independent resistances were extracted to be R_{Se} = 6.8–6.9 Ω, R_{De} = 7.4–7.5 Ω, and R_{SUB} = 7.4–7.6 Ω as summarized in Fig. 4(c) and (d).

For V_{GS}-independent spreading resistances (R_{So}, R_{Do}), we combined the DSCT and the CRM with R_{Se}, $R_{Si}(V_{GS})$, R_{De}, and $R_{Di}(V_{GS})$ as summarized in Table 1. As shown in Fig. 5(a) and (b), $R_{diff}(=R_D - R_S)$ increases with increasing V_{GS} and the difference in the transconductances for the forward and reverse mode configurations shows a strong dependence on V_{GS}. We expect that this is caused by the V_{GS}-dependent change of the intrinsic part of the source and drain resistances. While $R_{Si}(V_{GS})$ and $R_{Di}(V_{GS})$ decrease by increasing the gate bias, the V_{GS}-independent parts (R_{Se}, R_{So}, R_{De}, R_{Do}) are kept constant. This means that the result of the DSCT still contains the V_{GS}-dependent resistances. Therefore, by combining the DSCT with V_{GS}-dependent resistances ($R_{Si}(V_{GS})$, $R_{Di}(V_{GS})$) we can de-embed the effect of V_{GS}-dependency as shown in Eqs. (17) and (18).

Finally, combining all of the extracted resistances with R_{tot} over the V_{GS}, we separated and summarized the V_{GS}-and L_{eff}-dependent $R_{CH}(V_{GS},L_{eff})$ in Fig. 6 and Table 1. We also note that, R_{tot}-R_{CH} has a constant value regardless of L_{eff} at V_{GS} = 3 V. This result confirms the consistency of the proposed extraction technique for parasitic resistance components in MOSFETs. The V_{GS}-independent resistances (R_{Se}, R_{So}, R_{De}, R_{Do}, R_{SUB}) were kept constant over the gate bias while V_{GS}-dependent resistances ($R_{Si}(V_{GS})$, $R_{Di}(V_{GS})$) decrease with V_{GS} due to the enhanced conductivity of the channel region. We also note that and the V_{GS}- and channel length-dependent (V_{GS},L_{eff}) is proportional to L_{eff} as expected in MOSFETs.

4. Conclusion

We reported a fully electrical comprehensive combinational (I-V and C-V) technique for separate extraction of parasitic resistance components in MOSFETs. It is fully electrical technique considering any possible asymmetry (caused by the fabrication process, the layout, the degradation due to electrical stress during the operation) and the V_{GS}-dependence over the operation bias range. In the technique for extraction of V_{GS}-dependent resistances ($R_{Si}(V_{GS})$, $R_{Di}(V_{GS})$), we combined the CRM for the total resistance and the TLM for the overlap length. We also separately extracted V_{GS}-independent resistances (R_{Se}, R_{So}, R_{De}, R_{Do}, R_{SUB}) through the ODM, the PJCM, and combination of the CRM and the TLM. V_{GS}-independent resistances are extracted to be R_{Se} = 6.8–6.9 Ω, R_{De} = 7.4–7.5 Ω, R_{SUB} = 7.4–7.6 Ω, R_{So} = 1.8–2.1 Ω, and R_{Do} = 3.2–3.5 Ω in n-channel MOSFETs with L = 0.18, 0.27, and 0.36 μm and W = 50 μm. The V_{GS}-dependent resistance components are separated to be $R_{Si}(V_{GS})$ = 1.9–4.4 Ω, $R_{Di}(V_{GS})$ = 1.4–3.2 Ω, and $R_{CH}(V_{GS})$ = 29–41.9 Ω at W/L = 50 μm/ 0.27 μm. This comprehensive and analytical technique is expected to be helpful for securing the characterization of fabrication process and modeling of electrical characteristics in MOSFETs with the body contact as well as a robust design of CMOS integrated circuits and systems. Replacing the PJCM requiring the body contact by the advanced ODM under development, we expect to report an advanced and extended technique for separate extraction of parasitic resistance components in insulated gate FETs both with and without body contact including conventional MOSFETs, SOI MOSFETs, FinFETs, and even thin-film transistors (TFTs).

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