Cost-effective Fabrication of $In_{0.53}Ga_{0.47}As$-on-Insulator on Si for Monolithic 3D via Novel Epitaxial Lift-Off (ELO) and Donor Wafer Re-use

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Abstract**—**Defect-less semiconductor-on-insulator (-OI) by a cost- effective and low temperature process is strongly needed for monolithic 3D (M3D) integration. Toward this, in this paper, we present a cost-effective fabrication of the InGaAs-OI structure featuring the direct wafer bonding (DWB) and the epitaxial lift-off (ELO) techniques as well as the re-use of the InP donor wafer. We systematically investigated the effects of the pre-patterning of the III-V layer before DWB, surface reforming (hydrophilic), and electro-chemical etching to speed up the ELO process for a fast and high-throughput process, which is essential for cost reduction. We also demonstrated the re-usability of the InP donor wafer. Finally, as a result of the high film quality of the InGaAs channel combined with DWB and ELO, fabricated InGaAs-OI MOSFETs show a **record-high** effective mobility of ~2800 cm^2/Vs among surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs reported so far.

I. Introduction

Monolithic 3D (M3D) integration is a promising pathway to reduce the interconnect delay and increase transistor density [1]. Consequently, it can reduce the power density of the chip, which allow us ultimate power scaling [1, 2]. However, the current technology has technological challenges shown in **Fig. 1**, which requires low temperature process for the fabrication of the top FET as well as low cost process [1]. On the other hand, a process temperature of III-V (such as InGaAs) FETs is typically quite low (<400°C), which induce no effect on the bottom FET and the interconnect metallization. Furthermore, the InGaAs layer is expected to be the most attractive channel for the next-node transistors due to its high electron mobility. Recent studies demonstrated high performance InGaAs-on insulator (-OI) MOSFETs, which has highly scalable and most straightforward device structure for M3D [3, 4].

Considering M3D requirements and the benefit of InGaAs-OI channel, InGaAs is expected to be a quite promising channel material for M3D. Also, using the direct wafer bonding (DWB) and epitaxial lift-off (ELO) techniques, a low cost process is possible via the re-use of the donor wafer without any external damages as seen in the smart-cut technique. However, conventional ELO techniques have been mainly studied using a GaAs donor wafer to use the lattice matched sacrificial layer of AlAs [5-8], resulting in the difficulty in the use of InGaAs due to the lattice mismatch between GaAs and In(Ga)As. Moreover, many studies showed very long processing time (low throughput) due to long lateral etching distance and hydrophobic surface, whereas process should be fast for high-throughput and practical cost reduction. Also, the wafer re-usability for InGaAs MOSFETs through the ELO technique has not been demonstrated.

Therefore, in this work, to fully utilize the benefit of M3D with the InGaAs channel, we developed the DWB and ELO techniques to form the InGaAs layer on Si substrates (**Fig. 2**). Here, we also developed the growth of the AlAs sacrificial layer on the InP donor substrate. Furthermore, we first demonstrated InGaAs-OI MOSFETs on a Si substrate fabricated through the DWB and ELO processes. For high-throughput ELO, we carefully designed and investigated a pre-patterning process of the III-V layer before DWB [9], surface reforming, and electro-chemical etching for ELO. We also experimentally demonstrated the donor wafer re-usability for the fabrication of InGaAs MOSFETs. As a result, the proposed method provides an integration pathway for cost-effective M3D using the high quality InGaAs layer.

II. Fabrication of InGaAs-OI via Wafer Bonding and ELO Introduction

InGaAs-OI on Si wafer was fabricated by DWB and ELO (**Fig. 2**). First of all, InGaAs (20 nm, undoped)/AlAs (as a sacrificial layer) layers were epitaxially grown on InP (100) substrate. AlAs thickness (T_{AlAs}) was varied between 0 and 10 nm in order to investigate the InGaAs quality and the ELO time. Subsequently, a 20 nm-thick Y_2O_3 layer was deposited both on III-V(InGaAs/AlAs/InP) and on Si wafers. Prior to DWB, the donor wafers were pre-patterned for a fast ELO via efficient gas bubble (by-product during etching) release and an enlargement of the exposed etching area [9]. Here, the typical pattern size was 100 × 100 μm^2. Then, Y_2O_3/InGaAs/AlAs/InP substrate and Y_2O_3/Si substrate were directly bonded to each other. Finally, InGaAs-OI/Si substrates and InP donor wafer were separated by the selective etching of the AlAs layer in HF solutions. To evaluate the InGaAs quality, we measured the Raman spectra of InGaAs/AlAs/InP substrate with respect to T_{AlAs} before and after the DWB (**Fig. 3**). The InGaAs peak was quite sharp for all T_{AlAs}. It is worth noting that the InGaAs peaks show a positive shift with an increase of T_{AlAs} (0, 2, 5, 10 nm) due to the compressive strain caused by the lattice mismatch between the AlAs and InGaAs layers. After DWB and ELO process, the Raman spectra of InGaAs /Y_2O_3/Si substrate shows both sharp peaks of InGaAs and Si, indicating successful fabrication of the high-quality InGaAs-OI on Si. After the ELO, a strain relaxation was observed due to the etching of AlAs layer. **Fig. 4** shows an atomic force microscopy (AFM) image of the surface of InGaAs/AlAs(T_{AlAs} = 5 nm)/InP substrate and InGaAs/Y_2O_3/Si substrate before and after surface cleaning by HCl solutions. As grown sample on InP substrate shows very smooth surface with a root mean square (R_{rms}) value of 0.32 nm. After DWB and ELO, the InGaAs surface was roughened due to the by-product by the etching reaction of AlAs layers. However, the smoother surface with an R_{rms} value of 0.22 nm was obtained after the HCl cleaning. XRD spectra of the InGaAs-OI clearly confirmed nearly perfect crystal quality of the fabricated InGaAs-OI (**Fig. 5**). Cross-sectional TEM and HAADF images of as-grown InGaAs/AlAs(T_{AlAs}=5 nm)/InP are shown in **Fig. 6 (a)** and **(b)**, respectively. The InGaAs layer was well-grown without visible defects. A thin

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AlAs sacrificial layer was clearly seen between InGaAs and InP substrates, which is also confirmed by EDX profile (**Fig. 6(c)**). A cross-sectional TEM of the fabricated InGaAs-OI on Si clearly confirms excellent crystal quality and the bonding interface (**Fig. 7**).

III. DISCUSSIONS

A. Fast ELO techniques for high-throughput process

Here, one of the purposes of this work is to develop a fast ELO process. Therefore, we considered the etching mechanism of the AlAs sacrificial layer by the HF solution, which is depicted in **Fig. 8**. To speed up the etching, two conditions are required; 1. High concentration of the un-dissociated HF to enhance the dominant reaction mechanism, 2. Hydrophilic surface for efficient flow of the etchant and reaction product [10]. These were found to have strong trade-off relationship on the GaAs surface, which makes the ELO slow. However, since InP surface shows hydrophilic for HF solution, it would be quite weak on the InP surface, indicating high possibility of a fast ELO process. To investigate the effect of the molecule concentration (pH) and surface condition, we measured the contact angle and pH of HF solutions diluted with different solutions (**Fig. 9**). The HF solution with higher pH (HF:DIW than HF:Acetone) allows a short ELO time on the InP donor wafer contrary to the GaAs donor wafer. It is due to the large contact angle of HF:DIW on GaAs, which makes the ELO slow. On the other hand, InP shows a hydrophilic surface for all of HF solutions allowing a fast ELO (**Fig. 9**). We also observed a fast ELO with thicker T_{AlAs}, whereas too thick T_{AlAs} degrades the crystal quality (**Fig. 10**), showing that appropriate design of T_{AlAs} is significantly important to simultaneous achievement of both fast ELO process and good layer quality. Furthermore, we traced the effect of the pre-patterned area. The ELO time strongly depends on the pattern size of the pre-patterned region (**Fig. 11**). Reduced pattern area accelerates the ELO as fast as approximately 8 min. at the size of 50×50 μm^2 with a 100 μm spacing. Also, using the ELO technique, a dense pattern can be fabricated by reducing the spacing between patterns, whereas it shows the trade-off with the ELO time (**Fig. 12**). These results strongly indicate that pattern design for pre-patterning before the DWB is important for a dense pattern transfer as well as fast ELO process. Inspired by the pH-dependence of the ELO time (**Fig. 9**), we tried to intentionally concentrate on the un-dissociated HF molecules (HF_2^-, $H_2F_3^-$) by applying a positive bias between HF solutions and bonded III-V/Si (ELO target) (**Fig. 13(a)**). Unambiguous advantages of the ELO time (40 % reduction) was obtained by applying 1 V of bias (**Fig. 13(b)**). Further reduction in the ELO time is expected by continuous reduction of the pattern area and applying a higher positive bias or/and combining these two methodologies.

B. Electrical properties of InGaAs-OI MOSFETs

Using the high quality InGaAs-OI on Si obtained by DWB and ELO, we fabricated InGaAs-OI MOSFETs through the process flow shown in **Fig. 14**. **Figs. 15** and **16** illustrate the transfer and output curves of InGaAs-OI MOSFETs from the sample with T_{AlAs}=5 nm. Good *I-V* curves were obtained with a subthreshold swing (*S.S.*) = 120 mV/dec and high I_{on}/I_{off} ratio(>10^6). Considering the thick EOT (Y_2O_3/Al_2O_3=10 nm/5 nm) and un-optimized process, further improvement is still possible. These results highlight the first successful operation of InGaAs-OI MOSFETs fabricated by DWB and ELO. We compared an effective mobility (μ_{eff}) of InGaAs-OI and typical InGaAs MOSFETs on InP (**Fig. 17**). Higher μ_{eff} was obtained in InGaAs-OI MOSFETs due to high InGaAs channel quality and carrier distribution more in the centroid of the channel [4]. The μ_{eff} value itself is also quite high with a peak of ~2800 $cm^2/V{\cdot}s$.

C. Re-usability of the donor wafer for cost reduction

In order to investigate the re-usability of the InP donor wafer, we mimicked the ELO process by growing InGaAs/AlAs layer on InP and etching them by H_3PO_4-based solutions, followed by re-growth. **Fig. 18** shows the AFM image of the epi-structure for InGaAs MOSFETs on fresh and re-used wafer, showing smooth surface for both samples. Raman spectra also confirmed a good layer quality from the re-used wafer (**Fig. 19**). Since the surface and the optical measurement does not guarantee the re-usability, we also compared electrical characteristics of InGaAs MOSFETs both from fresh and re-used wafers. The *I-V* curves and μ_{eff} characteristics were almost identical, indicating that the donor wafer can be re-used after the ELO process (**Fig. 20, 21**). These significantly reduce the material/process cost for InGaAs-OI formation.

D. Benchmarks of our approach with other studies

μ_{eff} of the InGaAs-OI MOSFETs was compared with that from other surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs as a function of *EOT/CET* and *S.S.* value [11-19] (**Fig. 22, 23**). Our InGaAs-OI MOSFETs shows the **record-high** μ_{eff} value among reported surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs at given EOT/CET or *S.S.*. This is attributed to the high quality of the InGaAs channel, showing our DWB and ELO processes provide nearly perfect layer quality. Also, the ELO technique is comparatively benchmarked in Table 1 [5-8]. Our ELO technique shows the fastest process time and it is the first demonstration of InGaAs MOSFETs from the InP donor wafer as well as wafer re-use. The proposed integration scheme provides both high quality InGaAs-OI with highest throughput (fast ELO) and most cost-effective process (thin AlAs, re-use of the donor wafer). Finally, Table 2 summarizes various integration schemes of III-V on Si (not limiting for M3D), showing that the proposed scheme provides high quality III-V integration on Si with a cost-effective process [3, 20-22].

IV. CONCLUSION

We demonstrated a high-throughput ELO process to fabricate InGaAs-OI MOSFETs on Si employing a pre-patterning of III-V layers before DWB, hydrophilic surface, and electro-chemical etching. We systematically investigated the ELO behavior with various HF solutions (pH), surface state, pre-patterning, and biasing on the ELO target sample. InGaAs-OI MOSFETs fabricated through DWB and ELO techniques show good electrical properties, indicating excellent film quality. Proposed scheme provides a cost-effective III-V-OI platform for M3D as well as the next generation logic circuits.

ACKNOWLEDGMENTS

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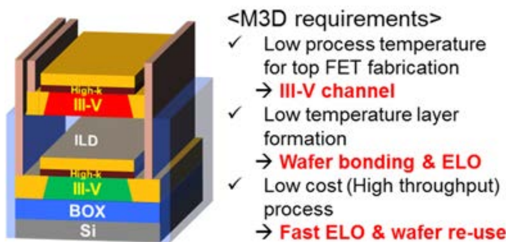

Fig.1: Schematic image of the M3D integration using III-V semiconductor.

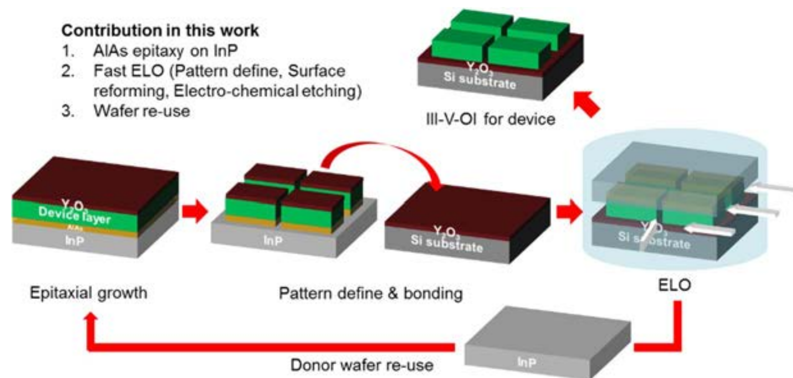

Fig.2: Process flow of the InGaAs-OI wafer by the proposed wafer bonding technique. Multi-chip/-wafer bonding can be applicable for > 300 mm wafer scalability.

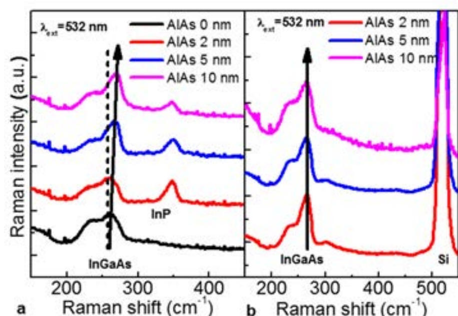

Fig. 3 Raman spectra of the InGaAs layer (a) before and (b) after the bonding as a parameter of T_{AlAs}.

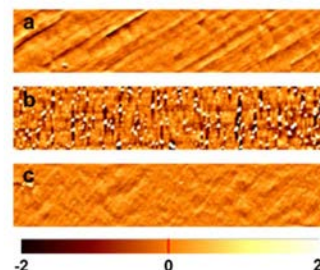

Fig. 4 AFM images of the InGaAs surface (a) before, (b) after the bonding, and (c) surface cleaning by HCl. RMS values after surface cleaning is as low as 0.2 nm.

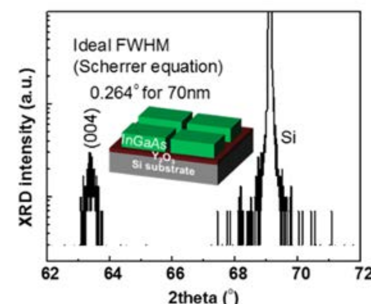

Fig. 5 XRD spectra of fabricated InGaAs-OI, showing almost ideal FWHM.

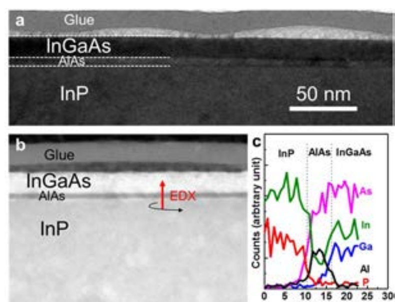

Fig. 6 Cross-sectional (a) TEM (b) HAADF image of as-grown InGaAs/AlAs/InP substrate. (c) EDX profile.

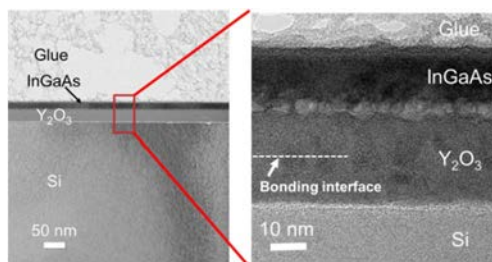

Fig. 7 Cross-sectional TEM images of InGaAs/Y_2O_3/Si and high resolution images of the sample. Clear bonding behavior was observed. No distinguishable bonding interface was seen.

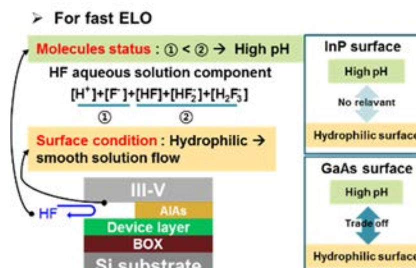

Fig. 8 Schematic illustration of the AlAs etching process. For fast ELO, high concentration of ② and hydrophilic surface are strongly required.

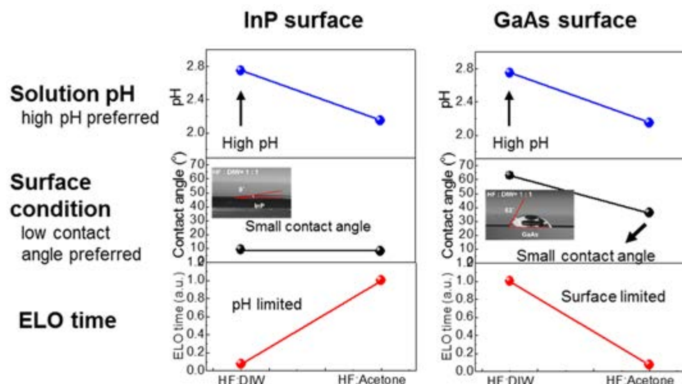

Fig. 9 Solution dependence of pH, contact angle, and ELO time. Since molecules status and surface condition has no trade-off, InP surface shows fast ELO time.

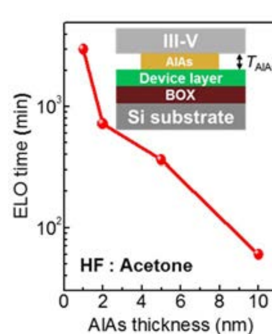

Fig. 10 T_{AlAs} dependence of the ELO time for separation of the InP from III-V-OI/Si in HF solution.

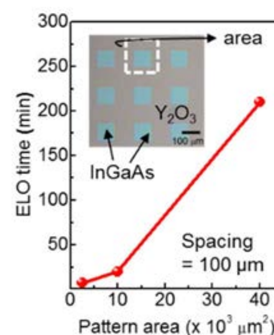

Fig. 11 Pattern area dependence of the ELO time with a spacing of 100 μm.

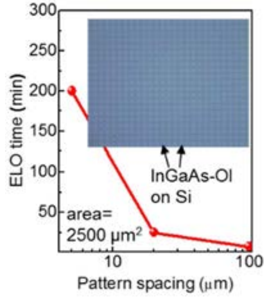

Fig. 12 Pattern spacing dependence of the ELO time with a fixed pattern area of 2500 μm^2.

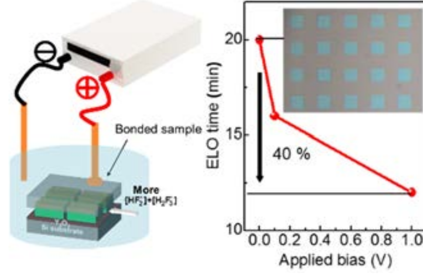

Fig. 13 (a) Schematic image of experimental setup of electro-chemical etching for ELO. (b) Applied bias dependence of the ELO time. Significant reduction in the ELO time was observed by concentrating negative HF ions.

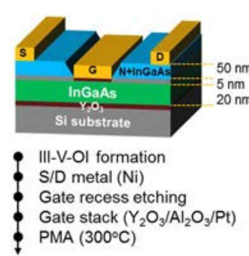

Fig. 14 Fabrication process of InGaAs-OI MOSFETs with gate recess structure (Dimensions are no to scale).

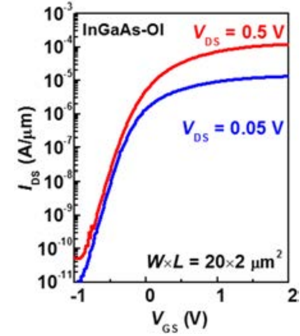

Fig. 15 Transfer curves of InGaAs-OI MOSFETs, showing good *I-V* curves with high I_{on}/I_{off}.

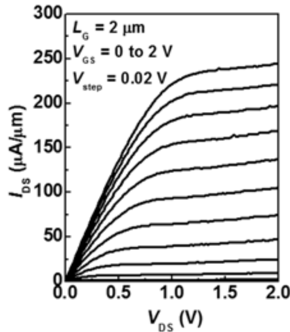

Fig.16 Transfer and output curves of InGaAs-OI MOSFETs. Clear current saturation can be seen in fabricated InGaAs-OI MOSFETs.

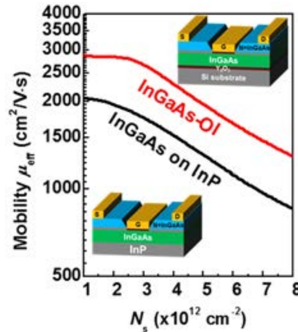

Fig. 17 The μ_{eff} characteristics of InGaAs-OI and bulk InGaAs MOSFET. High μ_{eff} was obtained in InGaAs-OI MOSFETs.

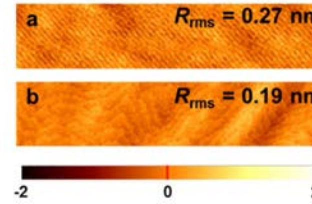

Fig. 18 AFM images of InGaAs surface grown on (a) fresh and (b) re-used InP wafer. Both surface shows low R_{rms}.

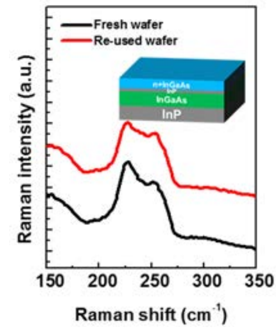

Fig. 19 Raman spectra of n+InGaAs layer grown on fresh and re-used wafer. Enhanced TO peak is due to the high doping of Si.

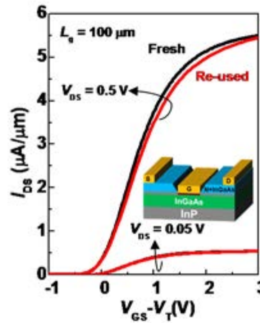

Fig. 20 The I_{DS} characteristics of InGaAs MOSFETs from fresh and re-used wafers as a function of V_{GS}-V_T

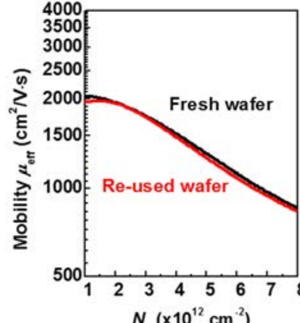

Fig. 21 The μ_{eff} characteristics of InGaAs MOSFETs from fresh and re-used wafers, showing almost identical characteristics.

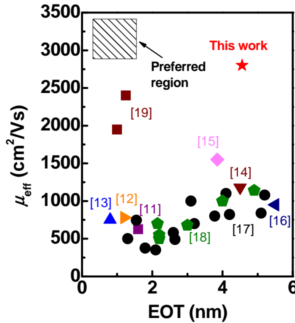

Fig. 22 Benchmarks of μ_{eff} as a function of EOT/CET for surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs at N_s of 3×10^{12} cm^{-2}.

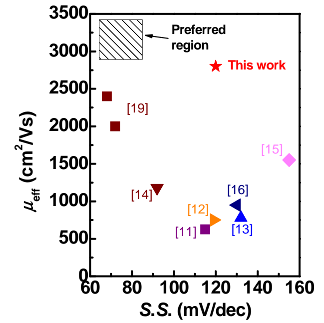

Fig. 23 Comparison of μ_{eff} – *S.S.* with other surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs at N_s of 3×10^{12} cm^{-2}.

Table. 1 Comparison of ELO techniques with other groups.

Group	IBM T.J. Watson [5]	U. Michigan [6]	U. National Chung Hsing [7]	AIST [8]	This work
Donor substrate	GaAs	GaAs	GaAs	GaAs, Ge	InP
Re-use of donor wafer	O	O	x	x	O
Sacrificial layer	InAlP (100nm)	AlAs (20nm)	AlAs (20nm)	AlAs (5-150nm)	AlAs (5nm)
ELO time	8 hours	5 hours	3 hours	5 hours	8 min
Application	LED, MOScap, Solar cell	LED, MESFETs, Solar cell	Solar cell	CMOS	CMOS

Table 2. Benchmark of the integration method for III-V/Si.

	DWB (grown on III-V sub.) [3]	DWB (grown on Si sub.) [20]	ART [21]	CELO [22]	This work
Wafer size > 300mm	X	●	●	●	●
Cost	High	Medium	Low	Low	Low
Epi-layer structure	III-V/ III-V sub.	III-V/thick buffer/ Si sub.	III-V/ buffer/ Si sub.	Lateral over growth/Si sub.	III-V/ III-V sub.
Channel quality	●	▲	▲	●	●
Back interface control	●	●	X	X	●
SCEs control	UTB or Fin	UTB or Fin	Fin	UTB or Fin	UTB or Fin

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