Halo Doping-Dependence and Structural Optimization of Short Channel Effects in Partially Insulated MOSFETs (PiFETs)


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Abstract

The effect of a halo doping on SCE in PiFET is investigated. The reduction of the separation between two PiOX layers ($L_{PiOX}$) followed by a local agglomeration of halo doing region makes the reverse short channel effect efficiently suppressed. As the $L_{PiOX}$ decreases, the subthreshold swing decreases, and the DIBL decreases. The final optimized condition is $L_{PiOX}=0.7 \times L_g-1.0 \times L_p$.

I. Introduction

As the scaling of the conventional CMOS technology proceeds, the improvement of both the performance and power consumption becomes inevitably more and more difficult. Recently, hybrid silicon-on-insulator (SOI)/bulk CMOS technologies have been extensively explored. Among various approaches, the hybrid orientation technology (HOT) has been successfully demonstrated to maximize the stress-induced mobility of both n-MOSFET and p-MOSFET, respectively. The HOT integrates an n-MOSFET in (001) silicon with a p-MOSFET in (110) silicon on the same wafer [1, 2]. In the HOT, an n-MOSFET is commonly implemented on an SOI substrate, and a p-MOSFET is done on epitaxially grown bulk silicon, respectively.

On the other hand, the recently proposed partially-insulated MOSFET (PiFET) is another promising candidate for hybrid SOI/bulk CMOS technology in spite of its more or less complicated process sequence, in that the SOI CMOSFET is able to be selectively implemented on a bulk silicon substrate [3]. It means that a cost-effective optimization of both the digital and analog part in the integrated circuits is possible, respectively. The PiFET technology has been already applied to DRAM cell array transistors [4]. In perspective of the performance, PiFET can fully take the advantages of quasi-SOI device, like body-tied FinFET [5], such as a low cost, reduced self-heating, controllable threshold voltage ($V_T$) engineering, and no floating-body effect. The partially-insulated oxide (PiOx) layer located just under the source/drain region suppresses the junction capacitance, and acts as a diffusion barrier resulting in self-induced halo regions near its edge. This phenomenon contributes to reducing both a short channel effect (SCE) and a junction leakage current [6].

In this work, the effect of a halo doping on SCE in PiFET is investigated. Furthermore, the structural optimization is performed, focused on the relation between the location of halo doing region and the separation between two PiOX layers ($L_{PiOX}$).

II. Simulation Results and Discussions

Fig. 1 shows the cross section of PiFET used in a process simulation. It was performed by ISE TCAD tool (SENTAURUS PROCESS and DEVICE 2-D simulator) [7]. Basically, the substrate doping concentration ($N_{eff}$) was $1 \times 10^{15} \text{cm}^{-3}$ and the gate was $n^+$-doped poly-silicon. The SOI thickness ($T_{SOI}$) was 20 nm, and the channel doping profile was formed by indium for super steep retrograde channel region [8]. The $V_T$ is measured by the gate voltage ($V_{GD}$) at which the drain current ($I_{DS}$) is the value of 0.1 $\mu$A/µm, and the supply voltage ($V_{DD}$) is set to be 1.5 V.

Fig. 2 shows the simulated current-voltage ($I-V$) characteristics of PiFET, bulk MOSFETs, and SOI MOSFET with the gate length ($L_g$) of 30 and 50 nm, respectively. The PiFET shows better SCE immunity than MOSFET, and comparable to SOI MOSFET. The performance parameters are summarized as shown in Table I.

In order to investigate into the halo doping effect, both $L_g$ and $L_{PiOX}$ are split in the same simulation condition. The lateral location of the peak of halo doping concentration is varied with $L_g$, and $L_{PiOX}$ is another independent parameter. This condition agrees with the actual process sequence [3, 4]. Fig. 3 shows the consequent cases in terms of the relation between the location of halo doing region and $L_{PiOX}$. As the $L_{PiOX}$ decreases, highly doped region by halo implantation is more locally agglomerated as shown in Fig. 3, which is strongly reminiscent of the self-induced halo doping in PiFET [4, 6, 9].

Fig. 4 shows the $L_{PiOX}$-dependence of both the subthreshold swing (SSW) and the drain-induced barrier lowering (DIBL). As the $L_{PiOX}$ decreases, the reduction of the depletion capacitance by the SOI-like effect becomes more dominant, followed by the decrease of SSW. Fig. 5 shows the potential contour with varying the $L_{PiOX}$. The reduction of $L_{PiOX}$ makes the electric field by a drain bias ($V_D$) be focused on highly doped halo region as shown in Fig. 3 and 4, followed by the increase of DIBL.

Fig. 6 shows the $V_T$ roll-off characteristic. The reverse SCE is minimized on the condition of $L_{PiOX}=0.7 \times L_g-1.0 \times L_p$. It results from a local agglomeration shown in Fig. 3. The optimization of reverse SCE is possible by the control of the angle of halo implantation ($T_{halo}$), as shown in Fig. 6 (b).

III. Conclusions

The effect of a halo doping on SCE in PiFET is investigated. The reduction of $L_{PiOX}$ followed by a local agglomerated of halo doing region makes the room for the optimization of SCE in PiFETs, whose optimized condition is $L_{PiOX}=0.7 \times L_g-1.0 \times L_p$. Our result shows that the $L_{PiOX}$ is a critical parameter controlling all of SSW, DIBL, and reverse SCE, which applies the good guide of the structural optimization of PiFETs for their performance improvement.

Acknowledgements

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References


Fig. 1. The schematic diagram of simulated PiFET.

Table 1. The SCE comparison among the bulk MOSFET, PiFET without halo doping, and PiFET with halo doping.

<table>
<thead>
<tr>
<th>Lg</th>
<th>Parameter</th>
<th>Bulk MOSFET</th>
<th>PiFET (w/o halo)</th>
<th>PiFET (with halo)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 nm</td>
<td>Vt (V)</td>
<td>0.1</td>
<td>0.13</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td>SSW (mV/dec)</td>
<td>80.9</td>
<td>77.5</td>
<td>78.8</td>
</tr>
<tr>
<td></td>
<td>DIBL (mV)</td>
<td>45.5</td>
<td>37.2</td>
<td>21.5</td>
</tr>
<tr>
<td>30 nm</td>
<td>Vt (V)</td>
<td>0.07</td>
<td>0.09</td>
<td>0.21</td>
</tr>
<tr>
<td></td>
<td>SSW (mV/dec)</td>
<td>103.8</td>
<td>96.3</td>
<td>89.3</td>
</tr>
<tr>
<td></td>
<td>DIBL (mV)</td>
<td>146.8</td>
<td>120</td>
<td>54.2</td>
</tr>
</tbody>
</table>

Fig. 2. The I-V characteristics of PiFET, bulk MOSFETs, and SOI MOSFET with Lg= 30 and 50 nm, respectively.

Fig. 3. The relation between the location of the halo doping region and the LPiOX. (a) LPiOX=1.0×Lg (b) LPiOX=0.5×Lg (c) LPiOX=0.3×Lg.

Fig. 4. The LPiOX-dependence of both SSW and DIBL.

Fig. 5. Potential contour distribution at the VD=1.5 V. (a) LPiOX=1.0×Lg (b) LPiOX=0.3×Lg. As the LPiOX increases, the DIBL decreases.

Fig. 6. The Vt roll-off characteristic of PiFET. (a) The LPiOX-dependence at a fixed Ttilt=75º. (b) The Ttilt-dependence of the reverse SCE.