Novel Flat Band Voltage Extraction using Optical Substrate Current and Lateral Profiling of Trapped Charges in Localized Charge Trapping Flash Memory Cells

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Abstract
We proposed a novel extraction method for the flat band voltage ($V_{FB}$) in MOSFETs by using optical excitation. Analyzing the optical substrate current ($I_{sub,photo}$) by simulation and analytical model, it has been applied to charge trapped flash (CTF) memory cells for extracting the lateral profile of trapped charges. Because $V_{FB}$ of the programmed region is higher than that of non-programmed regions in locally programmed CTF cells, there is a multi-step response in $I_{sub,photo}$-$V_G$ curves. The height and width of the multi-step are related to the programmed location and density of trapped charges and this technique is expected to be useful for lateral profiling of trapped charges.

I. Introduction
As a promising next generation EEROM, nitride-based localized trapping storage flash (CTF) memories are under active study for multi-bit operation. The spatial distribution of traps is crucial in SONOS-type CTF cells because of the spatially discrete nature in the nitride layer [1,2]. The evolution of lateral charge profile and the mismatch between programmed electrons and erased holes have a critical influence on a retention characteristic with P/E cycling [3]. There have been various lateral profiling techniques that have been used for extracting the lateral profile of charges trapped in nitride storage layer [4-7]. However, even with advantages with DC I-V and charge pumping techniques, there is still some limit to apply them to CTF memories because they inevitably induce an electrical stress during characterization and contains inherent inaccuracy in extremely scaled nonvolatile flash memories.

In this work, a lateral charge profiling technique based on the flat band voltage ($V_{FB}$) monitoring using the optically induced substrate current ($I_{sub}$) in localized trapping flash memory cells is proposed. Monitoring the change of $V_{FB}$, it is suitable for extracting the trapped charge distribution of CTF memory cells excluding the interface state density. We explain the mechanism of photo-generated substrate current ($I_{sub}$) in MOSFET and apply this technique to extract lateral distribution of trapped charges.

II. Modeling of Optical Responses in CTF Memory Cells

Photo-generated substrate current ($I_{sub,photo}$): Fig. 1(a) shows the schematic diagram illustrating the concept of proposed technique in n-type MOSFETs. Under optical excitation for optical source with $\lambda$=850 nm and $P_{opt}$=1 mW, the electron-hole pairs (ehp’s) are generated in Si substrate and the photo-generated $I_{sub}$ is induced. $I_{sub}$ depends on the gate voltage $V_G$ because the quantity of carriers (electrons and holes) contributing to the optical $I_{sub}$ is varied with the energy band bending at the Si surface.

a) $I_{sub,photo}$ under $V_G$< $V_{FB}$: $I_{Ls}$ and $I_{diff}$ in the Fig.1(a) are photo-generated current density in the source and drain depletion regions, respectively. The generated electrons and holes contribute to the drain and substrate current as described by

$$I_{Ls} = J_{Ls} = J_{si} + J_{pl}$$

(1)

where $J_{Ls}$ is generation current density in the depletion region, $J_{si}$ and $J_{pl}$ are minority carrier diffusion current density from the neutral region closed to the depletion region. $J_{diff}$ in Fig. 1(a) is diffusion current density of electron and hole to the substrate contact. If the optical source having larger than the silicon band gap ($E_g=1.12$ eV) is illuminated to the MOSFET, ehp’s are generated under the channel region. Because the excess carrier generation rate is exponentially reduced along the substrate depth, there is a diffusion current of electrons and holes to the direction of substrate contact. This photo-generated substrate current $I_{sub,photo}$ can be described by

$$I_{sub,photo} = I_{Ls} + I_{Ld} + I_{diff}$$

(2)

b) $I_{sub,photo}$ under $V_G$ > $V_{FB}$: In the case of $V_G$ > $V_{FB}$, $I_{sub,photo}$ is abruptly increased due to two reasons. In the first, as the channel depletion region starts to appear, $I_{sub,photo}$ is increased by the generated holes in the channel depletion region($I_{dir}$) and the diffusion current of minority electrons($I_{diff}$) at the depletion edge as shown Fig 1(b). Secondly, $I_{diff}$ is reduced as $I_{diff}$ because the gradient of the excess carrier distribution becomes lower than initial state as shown Fig 2(a). As a consequence, $I_{sub,photo}$ abruptly increases at the point of $V_G$ = $V_{FB}$ and has step-like response (step-wise $I_{sub}$) as shown in Fig. 2(b). $I_{sub,photo}$ under $V_G$ > $V_{FB}$ can be modeled by

$$I_{sub,photo} = I_{Ls} + J_{Ld} + J_{diff} + J_{Ls} + J_{diff,s}$$

(3)

$I_L$ and $J_{diff}$ are constant and independent of $V_G$ while $J_{Ls}$ and $J_{diff,s}$ depends on $V_G$. $J_{Ls}$ and $J_{diff}$ is expressed by

$$J_{Ls} = qG_{Ls}dx$$

(4)

$$J_{diff} = qg_{diff}L_s + \frac{qD_p}{L_c}$$

(5)

Fig. 3 shows the measurement data of $I_{sub,photo}$ and its drain bias dependence in the N-type MOSFET.

Lateral Profiling of Trapped Charges in CTF Memory: If $V_{FB}$ is varied along the channel length direction by a laterally non-uniform profile of electrons trapped in the nitride layer as shown in Fig.4(a), the multi-step response in $I_{sub,photo}$ is observed as shown in Fig. 5 with TCAD simulation result of photo-generated $I_{sub,photo}$-$V_G$ curve [8]. The reason of this multi step is shown in Fig. 4(b). $I_{sub,photo}$ is abruptly increase at $V_{FB}$ and $I_{sub,photo}$ under the program region is increased at $V_{FB}$. This means that this multi-step substrate current has information on the local charge distribution in the nitride layer. As the density of trapped charges increases, the width of second step induced by the trapped charges shifts more. In addition, as the distribution length of trapped charges at fixed channel length $L_c$ becomes longer, the height of the second step becomes more pronounced. The trapped charge density $Q_{tot}(x)$ and distribution length $\lambda$ is expressed by

$$Q_{tot}(x) = \Delta V(x) - C_{ONO}$$

(6)

$$\lambda = \frac{\Delta I_{sub,photo2} - I_{sub,photo1}}{\Delta I_{sub,photo2} + \Delta I_{sub,photo2}}$$

(7)

where $\Delta I_{sub,photo1}$ is the total change in $I_{sub,photo}$ and $\Delta I_{sub,photo2}$ is the change in $I_{sub,photo}$ under the program region as shown Fig. 5(b).

III. Experimental Results and Discussion

Photo-generated substrate current, $I_{sub,photo}$ of n-channel SONOS flash memory cell transistor($W/L=10um\times0.22um$, O/N/O layers: 40/40/40 Å) was measured with an optical source ($E_{opt}$=1.459eV). In Program conditions, CHEI ($V_{FB}$=5.5V, program time $T_p$=1ms) is used. In the reverse read operation, $V_G$ is swept from 0V to 4V at $V_{FB}$=0.1V. Other electrodes were grounded. Fig.6
shows measured data for \( I_{\text{sub,photo}} \). Because the measured devices had ESD protection diode, we could not apply negative voltage to the gate contact. So, as shown in Fig. 6, \( V_{\text{FB}} \) of the non-programmed region is not shown and only second step is observed. We could see the clear difference in \( I_{\text{sub,photo}} \) between the initial and programmed states. We are pursuing to extract the lateral profiling of trapped charges noting that \( I_{\text{sub,photo}} \) depends on the bias scheme as well as density of trapped charge. We expect to extract more reasonable results of the lateral trapped charge distribution.

IV. Conclusions

In this work, we proposed a new photonic extraction method for the flat band voltage \( V_{\text{FB}} \) in MOSFET. It is clearly verified that the abrupt transition point of \( I_{\text{sub,photo}} \) under photonic excitation is closely related to \( V_{\text{FB}} \) and verified by simulation and analytic model. We expect this technique to be useful for the extraction of lateral trapped charge profile in localized trapping storage flash memory cells. Locally increased \( V_{\text{FB}} \) by trapped charges induces the multi-step-like feature in \( I_{\text{sub,photo}} \). After verification through TCAD device simulation, we expect to obtain the lateral distribution of trapped charges from the difference of \( I_{\text{sub,photo}} \) between initial and program states.

Acknowledgements: This work was supported by the Korea Research Foundation Grant funded by the Korean Government (MOEHRD) (KRF-2006-331-D00210), and the TCAD software was supported by IC Design Education Center (IDEC).

References