Density-of-States Based Device-Circuit Co-Design Platform for Solution-Processed Organic Integrated Circuits

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Abstract

In this work, we propose the subgap density-of-states (DOS) based device-circuit co-design platform for solution-processed organic integrated circuits. For the circuit simulation, analytical I-V and C-V model were established from experimentally extracted DOS parameters, incorporated into HSPICE via Verilog-A, and verified by comparing the simulation result with the measured characteristics of inverter integrated with solution-processed polymer-based organic thin-film-transistors. Furthermore, as the case study, it was shown by using our well-calibrated simulation platform that the pass-transistor type logic was potentially promising in low-power and high-speed solution processed organic integrated circuits.

Author Keywords

Solution process; organic; polymer; thin-film transistors; density-of-states; analytical model; circuit simulation.

1. Introduction

A great deal of attention has been paid recently to organic electronics, driven by their potential applications throughout from flexible displays [1], large area sensors [2], and radio frequency identification tags [3] to flexible processors [4] and customized programmable logics [5]. In these approaches, polymer-based organic thin-film-transistors (POTFTs) are the fundamental building blocks with their advantages of low-cost, low-temperature process, and compatibility with the solution process such as spin-coating, ink-jet printing, and gravure printing. However, the circuit simulation method for the solution processed POTFTs has been rarely researched yet while a number of OTFTs with high field-effect mobility higher than 0.1 cm²/Vs have been reported using ink-jet printing [6], [7]. As their potential application becomes more diverse and challenging, the demand for device-circuit co-design, which should be described preferably only with the process/material-controlled and experimentally extracted parameters rather than fitting parameters, becomes indispensable in the solution-processed organic integrated circuits.

In this work, the subgap density-of-states (DOS) based device-circuit co-design platform was proposed. Firstly, the analytical I-V and C-V model were established from experimentally extracted DOS parameters, incorporated into HSPICE via Verilog-A, and verified by comparing the simulation result with the measured inverter characteristics. Second, with the proposed method, it was shown that the pass-transistor type logic was potentially promising in low-power and high-speed solution processed organic integrated circuits. Our results suggest that the established co-design platform is useful either for effectively optimizing the POTFT process and devices or for evaluating their effects on the circuit performance.

2. Device Fabrication and DOS extraction

The polymer-based organic semiconductor was dissolving in tetrahydronaphthalene (THN) at a concentration of 0.2 wt%, and then ink-jet printed via Dimatix printer. The fabricated POTFTs with a coplanar structure had the channel width (W)=120 μm, the gate-to-source/drain (S/D) overlap length (LGS)=10 μm, gate insulator thickness (Tg)=300 nm, and thickness of polymer film (Tpolymer)=50 nm (confirmed by FIB-SEM), respectively. A schematic illustration of integrated POTFT with a staggered bottom gate structure was shown in Fig. 1(a).

![Figure 1](image)

Figure 1. (a) A schematic illustration of the integrated POTFT with the bottom gate and bottom source/drain contact structure. (b) The frequency-dependent C-V characteristics measured by an LCR meter (HP4284A). (c) Extracted subgap DOS g(E). The subgap energy level is calculated from combining the relationship between VGS and the surface potential φS with CG,F(VGS) (in the inset) [8].

The subgap DOS (g(E) [cm⁻³eV⁻¹]) near the valence band maximum (Eᵥ) in the polymer film was extracted from the multi-frequency C-V spectroscopy [8], which used the measured frequency-dependent C-V characteristics between the gate and S/D electrodes (the bias voltage is represented by VGS) over a wide range of the small signal frequency [Fig. 1(b)]. In this work, three frequencies of f₁=1 kHz, f₂=100 kHz, and f₃=1 MHz were used for acquiring the frequency-independent C-V curve CG,F(VGS) [the inset of Fig. 1(c)]. Finally, the g(E) near Eᵥ of the active film in POTFT was extracted as indicated by the symbol in
Fig. 1(c) and modeled by a superposition of exponential tail states \([kT_D(E)]\) and exponential deep states \([g_{DD}(E)]\) [line in Fig. 1(c)] as follows:

\[
g(E) = g_{DD}(E) + g_{T_D}(E) = N_{TD} \times \exp \left( \frac{E - E}{kT_D} \right) + N_{DD} \times \exp \left( \frac{E - E}{kT_{DD}} \right) \tag{1}\]

with \(N_{TD}\) as the effective density of deep states, \(kT_{TD}\) as the characteristic energy of deep states, \(N_{TD}\) as the effective density of tail states, and \(kT_{TD}\) as the characteristic energy of tail states. The DOS model parameters were \(N_{TD}=8.0 \times 10^{18} \text{ cm}^{-3} \text{eV}^{-1}\), \(N_{DD}=1.0 \times 10^{17} \text{ cm}^{-3} \text{eV}^{-1}\), \(kT_{TD}=0.034 \text{ eV}\), and \(kT_{DD}=0.4 \text{ eV}\).

3. Analytical Model and Its Incorporation into Circuit Simulation

For the circuit simulation, an analytical \(I-V\) and \(C-V\) model were established by modifying our previous \(n\)-type metal oxide TFT model [9] into the \(p\)-type counterpart. The equations of \(I-V\) and \(C-V\) model were basically similar to [9], and the parameter-extracting procedure was illustrated in Fig. 2. Compared with [9], in this work, the model was further improved by implementing the Schottky diode-described contact model [10] as well as Frenkel-Poole field-effect mobility [11] in order to take into account the features of POTFTs such as the nonlinearity of output characteristics at a small \(V_{GS}\) (the drain-to-source voltage) and the \(V_{DS}\)-dependent output conductance \((g_D)\) [12].

The measured and calculated \(I-V\) characteristics were comparatively shown in Fig. 3(a)-(c). The calculated results agree well with the measured ones over wide range of \(V_{GS}\) and \(V_{DS}\). In addition, the output conductance was verified to agree well with the measured one [Fig. 3(d)], which suggested that the detailed nonlinearity of POTFTs was successfully reproduced with our improved model.

Figure 2. Analytical model flow: Fixed input parameters \((P_{eff}=N_{TD}, kT_{TD}, W, L, T_{OX}, \text{ Schottky barrier (}\phi_h))\).

Figure 2 supplied the concrete method of parameter-extracting. More noticeably, the parameters describing effective carrier density, i.e., \(P_{eff}\) and \(kT_{eff}\), were used by experimentally extracted values of \(N_{TD}\) and \(kT_{TD}\) [Fig. 1(c)] with their physical meanings and consistencies (see [8]-[10] for details). Our approach also made it possible to co-design with the definite relationship between the process/material and the device characteristics because most of all parameters (excluding just only three fitting parameters, i.e., \(P_{eff}, kT_{eff},\) and \(V_{in}\)) can be controlled by either the process or the material.

Figure 3. \(I_{DS}-V_{GS}\) characteristics (a) in a linear scale and (b) in a semi-log scale. (c) \(I_{DS}-V_{DS}\) characteristics and (d) output conductance \((g_D)\) are compared with the measured ones.
The proposed analytical $I$-$V$ and $C$-$V$ models were implemented into the HSPICE simulator via Verilog-A. Due to the analytical forms, a fast convergence and good stability were demonstrated. The measured voltage transfer characteristics (VTC) [Fig. 5(c)] and transient switching characteristics [Fig. 5(d)] of POTFT-based inverters [Fig. 5(a) and (b)] were compared with the simulation results. A good agreement verified that our device-circuit co-design simulation platform was well calibrated with experimentally extracted parameters. The used parameters were summarized in Table I.

### Table I. The model parameters used in POTFT inverter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Driver-TFT</th>
<th>Load-TFT</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_V$</td>
<td>$1.5 \times 10^{19}$</td>
<td></td>
<td>$[\text{cm}^{-3}]$</td>
</tr>
<tr>
<td>$J_{\text{BAND}}$</td>
<td>0.146</td>
<td></td>
<td>$[\text{cm}^{-2}/\text{V} \cdot \text{s}]$</td>
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<tr>
<td>$\phi_B$</td>
<td>0.45</td>
<td></td>
<td>$[\text{V}]$</td>
</tr>
<tr>
<td>$P_{\text{eff}}(=N_{TD})$</td>
<td>$5.2 \times 10^{15}$</td>
<td>$4.0 \times 10^{16}$</td>
<td>$[\text{cm}^{-3} \cdot \text{eV}^{-1}]$</td>
</tr>
<tr>
<td>$kT_{\text{eff}}$</td>
<td>0.031</td>
<td>0.031</td>
<td>$[\text{eV}]$</td>
</tr>
<tr>
<td>$P_{\text{eff}}$</td>
<td>$1.0 \times 10^{11}$</td>
<td>$1.0 \times 10^{11}$</td>
<td>$[\text{cm}^{-3} \cdot \text{eV}^{-1}]$</td>
</tr>
<tr>
<td>$kT_{\text{eff}}$</td>
<td>0.029</td>
<td>0.028</td>
<td>$[\text{eV}]$</td>
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<tr>
<td>$V_{\text{ON}}$</td>
<td>-1.75</td>
<td></td>
<td>$[\text{V}]$</td>
</tr>
<tr>
<td>$T_{\text{OX}}$</td>
<td>300</td>
<td></td>
<td>$[\text{nm}]$</td>
</tr>
<tr>
<td>$W/L$</td>
<td>120/12</td>
<td></td>
<td>$[\mu\text{m}]$</td>
</tr>
</tbody>
</table>

### 4. Pass-Transistor Logic for Low-Power Organic Integrated Circuits

For the low-power solution-processed POTFT-based organic integrated circuits, three types of logic gates were comparatively investigated by using our co-design platform which was established as aforementioned. This study is very important because the power consumption of POTFT-based circuits, which is implemented only with the $p$-channel TFT configuration. Moreover, the solution-processed $n$-channel TFT is still very challenging. Three types of logic gates were the conventional resistor load (CRL), Pseudo-CMOS (Pseudo), and pass-transistor (PT) respectively. The performance of logic gates were comparatively simulated for NAND, NOR, and XOR (Fig. 6). In general, the CRL type is well known for $p$-channel-TFT-only digital circuits. Meanwhile, the $V_{\text{GS}}$-zero type logic was proposed [13] for boosting both the performance and the power consumption of CRL.

![Figure 6. P-channel POTFT-only logic gate circuits (NAND, NOR, and XOR) with three types of logic gates (CRL, Pseudo-CMOS, and PT).](image)
However, the $V_{GS}$-zero type logic required the complicated process and technology with well-controlled $V_T$ because the enhancement mode driver TFT should be combined with the depletion mode load TFT. Very recently, T.-C. Huang et al. [14] reported a Pseudo-CMOS. This is similar to the behavior of the conventional CMOS-based logic operation. In this work, we chose a PT as another promising logic type for the $p$-channel-only logic design and compared it with CRL and Pseudo. Fig. 7 shows the simulation results for the transient switching characteristics of three types of logic gates at $V_{GS}$=20 V. Evaluated propagation delay, power dissipation, and output voltage ($V_{OUT}$)-amplitude (defined as the swing of $V_{OUT\text{-MAX}}$-$V_{OUT\text{-MIN}}$) were summarized in Table II.

![Figure 7. Simulated transient switching characteristics of three types of logic gates with POTFT configuration.](image)

### Table II. Comparisons of the performance parameters from the simulation results for POTFT-based logic circuits

<table>
<thead>
<tr>
<th>Logic gate type</th>
<th>Propagation delay [μs]</th>
<th>Power dissipation [μW]</th>
<th>$V_{OUT}$-amplitude [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAND CRL</td>
<td>80.9</td>
<td>37.3</td>
<td>16.86</td>
</tr>
<tr>
<td>NAND Pseudo</td>
<td>19.8</td>
<td>37.6</td>
<td>18.36</td>
</tr>
<tr>
<td>NAND PT</td>
<td>4.22</td>
<td>0.023</td>
<td>19.91</td>
</tr>
<tr>
<td>NOR CRL</td>
<td>5.77</td>
<td>9.34</td>
<td>15.49</td>
</tr>
<tr>
<td>NOR Pseudo</td>
<td>5.65</td>
<td>9.70</td>
<td>18.77</td>
</tr>
<tr>
<td>NOR PT</td>
<td>4.65</td>
<td>0.0013</td>
<td>19.76</td>
</tr>
<tr>
<td>XOR CRL</td>
<td>5.44</td>
<td>18.6</td>
<td>15.30</td>
</tr>
<tr>
<td>XOR Pseudo</td>
<td>6.70</td>
<td>19.3</td>
<td>18.31</td>
</tr>
<tr>
<td>XOR PT</td>
<td>4.94</td>
<td>0.024</td>
<td>19.77</td>
</tr>
</tbody>
</table>

The Pseudo type is slightly better than CRL in terms of the $V_{OUT}$-amplitude and the propagation delay. However, in case of the XOR, a large number of POTFTs are required for Pseudo (10 TFTs) compared with CRL (5 TFTs). It was found that the PT type is superior in all aspects among three types of logic gates. In particular, it showed noticeable advantage in perspective of the power consumption. Fig. 8 shows the simulation result for transient short circuit current of NAND gate, which is synchronized with Fig. 7. We note that the short circuit current of the PT type NAND gate flows only at the input transition. Thus, it can reduce the power consumption significantly as seen in Table II.

![Figure 8. Simulated short circuit current of NAND gate.](image)

### 5. Conclusion
Subgap DOS-based simulation platform was proposed for the device-circuit co-design of POTFT-based organic integrated circuits. The analytical $I-V$ and $C-V$ model were established from experimentally extracted DOS parameters, incorporated into HSPICE via Verilog-A, and verified by comparing the simulation result with the measured inverter characteristics. Furthermore, we found that the PT type logic was potentially promising in low-power and high-speed solution processed organic integrated circuits in comparison with CRL and Pseudo-CMOS. Our results suggest that the established co-design platform is useful not only for effectively optimizing the POTFT process and devices but also for evaluating their effects on the circuit performance.

### 6. Acknowledgements
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### 7. References