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Comparative study on the energy efficiency of logic gates based on single-electron transistor technology

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Abstract
The performance and the power consumption of single-electron transistor (SET) technology-based ultra-energy-efficient signal processing circuits are compared based on the SPICE model including non-ideal effects of the experimental data for the first time. In terms of ultra-energy-efficient logic circuits, the binary decision diagram (BDD) logic circuit is the most promising with a dissipated power of 0.29 nW at $V_{dd} = 0.1$ V and $f_{in} = 50$ MHz among the static complementary metal-oxide-semiconductor (CMOS)-like SET logic, the dynamic SET/CMOS hybrid logic, cellular nonlinear network (CNN) and BDD. This result means that the transition of a paradigm substituting the current for the voltage as a state variable of a signal processing is strongly required in post-CMOS signal processing and ultra-energy-efficient applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Single-electron transistor (SET) technologies have widely been studied as promising solutions for ultra-low-power high-density logic and memory circuits [1, 2] because their operation principle becomes more robust as the device size is scaled down. However, irrespective of the technological issue of the room temperature operation, it is not expected that SETs would replace conventional complementary metal-oxide-semiconductor (CMOS) logic devices, because of their inherent limitations such as low voltage gain and weak current drivability. From these viewpoints, the efficient use of the new functionality of SETs combined with SET/CMOS hybrid circuits becomes more strongly required in order to find a breakthrough for the nanotechnology-oriented post-CMOS signal processing and sensing scheme. Especially, the novel functionalities of SETs such as the periodic switching, multi-gate switching, negative differential resistance (NDR), single-electron charging effect and quantum dot-to-quantum dot interaction have been explored and demonstrated for extensive applications such as the quantum computer [3], quantum cellular automata [4], threshold logic gate [5], multi-valued logic [6–8], analog-to-digital/digital-to-analog converters [9–12], majority gate [13, 14], full adder [15, 16], binary decision diagram (BDD) devices [17–20], cellular nonlinear network (CNN) [21–24], etc. Nevertheless, the various approaches for the assessment of the circuit performance of

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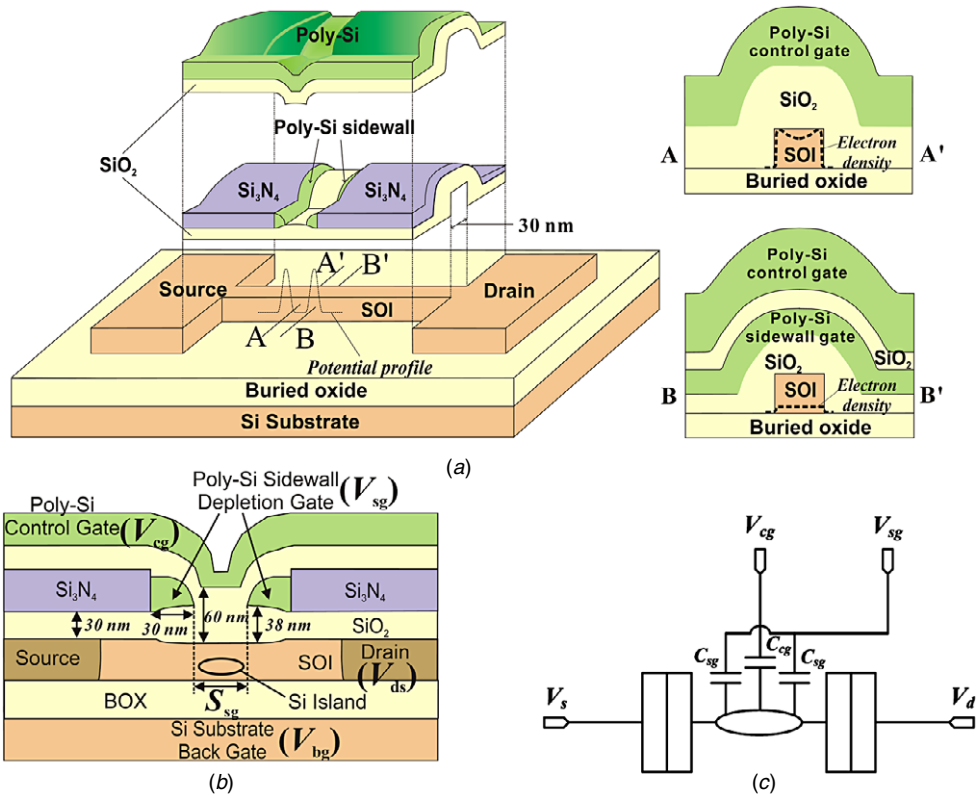

Figure 1. (*a*) Schematic diagram of the DG-SET with sidewall depletion gates on an SOI nanowire. (*b*) Cross-section of the fabricated DG-SET. (*c*) Equivalent circuit diagram of DG-SET.

SETs and SET/CMOS hybrid circuits, from Monte Carlo simulation to the analytic model and SPICE model [25–30], have been based on the ideal SET characteristics rather than the experimental data. Actually, non-ideal effects including the control gate bias dependence of the tunneling resistance, parasitic field-effect transistor (FET) operation and the phase shift of the Coulomb oscillation by the gate bias other than the main control gate have been commonly observed in previously demonstrated top–down approached Si-based SETs [31–42]. They cannot be considered in Monte Carlo simulation (e.g., SIMON [25]), the analytic and/or SPICE model based on the orthodox theory of single-electron tunneling [26–30].

In this paper, the performance and power consumption of SET technology-based ultra-energy-efficient signal processing logic gates are comparatively investigated by using the SPICE model considering non-ideal effects (peak to valley current ratio (PVCR) in Coulomb oscillation = 2.6–7.45 at $V_{dd} = 0.3$ V) in the measured data from really implemented devices, for the first time. In terms of ultra-energy-efficient logic gates, the static CMOS-like SET logic, the dynamic SET/CMOS hybrid logic, CNN and BDD are comparatively investigated.

2. Device structure, non-ideal characteristics and SPICE model

In order to investigate new energy-efficient logic circuits, a reproducible structure of Si-based SETs and SET/CMOS hybrid circuits is strongly required. Therefore, among various top–down approaches for Si SETs [31–42], the SETs based on gate-induced tunnel junctions [38–42] are very promising in terms of their strong confinement and reproducibility. Actually, the dual gate (DG)-SET with sidewall depletion gates on a silicon-on-insulator (SOI) nanowire has shown that the device parameters such as the control gate capacitance and the tunnel junction capacitance, as well as a relatively higher operation temperature, were reproducible [38].

Figure 1 shows the schematic diagram of the DG-SET structure with an equivalent circuit model. The electron channel in SOI nanowire is induced by both the control gate voltage (V_{cg}) and the back gate voltage (V_{bg}). Two tunnel barriers are electrically induced by the bias of poly-Si sidewall depletion gates (V_{sg}), and the potential in the Si island is controlled by the poly-Si top control gate bias (V_{cg}). Therefore, the size of the Si island can be controlled by both the width of SOI nanowire ($W_{ch} = 30$ nm) and the separation between two sidewall depletion gates (S_{sg}) as shown in figure 1(*b*). In figure 1(*c*), C_{cg}, C_{sg}, C_d, and C_s are the capacitance between the Si island and the control gate, the capacitance between the Si island and the sidewall depletion gate, drain tunnel junction capacitance and source tunnel junction capacitance, respectively. We note that the fabrication process is fully compatible with the conventional CMOS VLSI technology due to the sidewall patterning technique [38] which makes the DG-SET structure suitable for SET/MOSFET hybrid circuits.

Non-ideal effects in really implemented DG-SETs in [38] can be summarized in figure 2. Figure 2(*a*) shows the measured drain current (I_{ds})-V_{cg} characteristics of the fabricated Si-based SET. The temperature dependence appears on the reduced

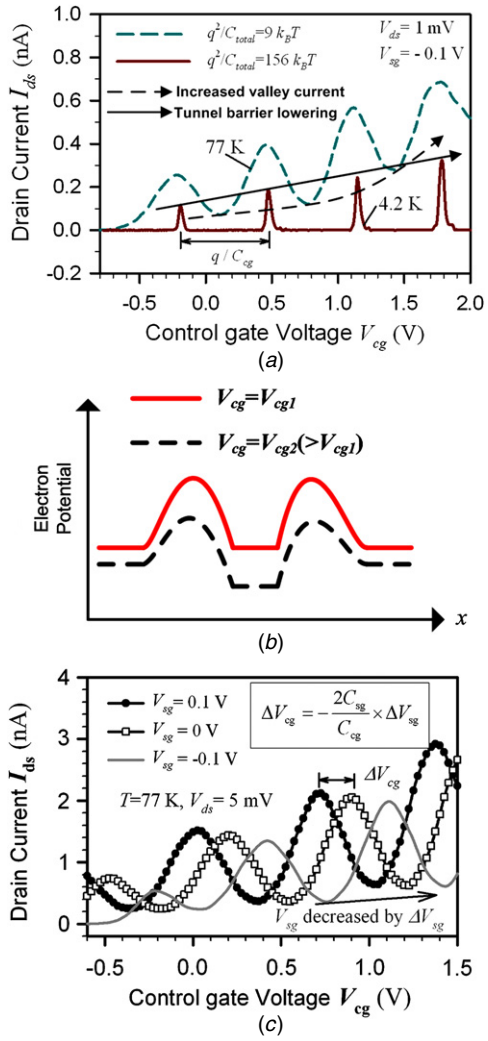

Figure 2. Non-ideal effects in really implemented SETs. (*a*) Measured tunnel barrier lowering and the parasitic FET operation. (*b*) The electron potential profile with the tunnel barrier lowering at higher V_{cg}. (*c*) Measured phase shift of Coulomb oscillation by the gate bias other than the main control gate. The inset shows the equation describing the relation between the variation of the other gate voltage ΔV_{sg} and the phase shift ΔV_{cg} by ΔV_{sg}.

PVCR in the Coulomb oscillation at elevated temperature. This is well known to be due to the smearing out of the Coulomb blockade condition by the thermal energy. As shown in figure 2(*a*), the peak current in the Coulomb oscillation increases with V_{cg} caused by the *tunnel barrier lowering effect*, and the valley current increases also with increasing V_{cg} due to the *parasitic FET operation*. This tunnel barrier lowering effect appears on the reduced PVCR with increasing V_{cg}, which results from the lowered barrier height due to the electric field effect formed by the control gate, as illustrated in figure 2(*b*). The parasitic MOSFET appears as the V_{cg}-dependent electron density in Si channel (consequently, the valley current of the Coulomb oscillation). On the other hand, the phase shift of Coulomb oscillation by the bias of gate other than a main control gate (e.g., the sidewall depletion gate voltage V_{sg} in [38]) is originated from the sharing of the Si island charge between all of the gates as shown in figure 2(*c*).

These non-ideal effects have been commonly observed not only in previously reported top–down approached Si-based SETs with the gate-controlled structure [38–42] but also in bottom–up approached SETs [43–47]. In spite of these non-ideal phenomena, the Si-based gate-controlled structure is believed to be the most promising SET structure for the controllability, reproducibility and possible integration with Si CMOS technology in the near future [48]. In the design of the SET-based or SET/CMOS hybrid circuits, therefore, these non-ideal effects should be fully considered. Moreover, the feature size in a few nm (i.e., the magnitude of input and output capacitances $\sim 10^{-19}$ F) is such beyond the state-of-the-art lithography that it is very challenging to really implement the SET technology-based circuits and systems. Nevertheless, by fast development of the process technology and the bottom–up nanotechnology, the paradigm of the post-CMOS nanodevice-oriented signal processing circuits and systems seems to emerge pretty soon. Thus, needless to say, the feasibility of ultra-energy-efficient circuits and systems based on SET/CMOS hybrid circuits should be assessed by means of the circuit model fully considering non-ideal effects in real and practical implementations.

Up to now, the incorporation of the SET theory into a circuit model has been pursued by several research groups [26–30]. Among them, Lee *et al* developed a practical SPICE model based on the physical phenomena in fabricated DG-SETs with two tunnel barriers by sidewall depletion gates [49, 50]. Lee's model reproduces the experimental characteristics of Si SETs over the wide range of temperature, the Si island size and the bias [49]. Figure 3 shows the simulated SET current contour based on the Lee's SPICE model. It is shown that the difference of a voltage gain as well as non-ideal effects described above are clearly reproduced. Parameters used in figure 3(*b*) ($C_{cg} = 0.24$ aF, $C_d = C_s = 1.3$ aF, $C_{sg} = 0.28$ aF, and resistances of tunnel junctions $R_s = R_d = 1$ MΩ) had been experimentally extracted and reproduced in [19, 38]. In our previous works, the controllability and reproducibility of various SET parameters ($C_{cg} = 0.24 \sim 2.0$ aF, $C_d = C_s = 1.25 \sim 1.5$ aF, $C_{sg} = 0.22 \sim 0.28$ aF, and $R_s = R_d = f(V_{sg})$) had been shown. Therefore, we note that Lee's SPICE model fully accounts for non-ideal effects of real Si-based SET characteristics and its physics-based nature is verified by the experimental data.

3. Device SET-based ultra-energy-efficient logic gates

In this Section, a comparative study on SET-based energy-efficient logic circuits is performed. Among the static CMOS-like SET logic, the dynamic SET/CMOS hybrid logic, CNN and BDD, the BDD logic gate is found to be most promising in terms of both the power dissipation and the performance.

3.1. Static CMOS-like SET logic

The basic approach for ultra-energy-efficient SET logic can be performed by imitating the static CMOS inverter. Figures 4(*a*) and (*b*) shows the circuit diagram of the static CMOS-like

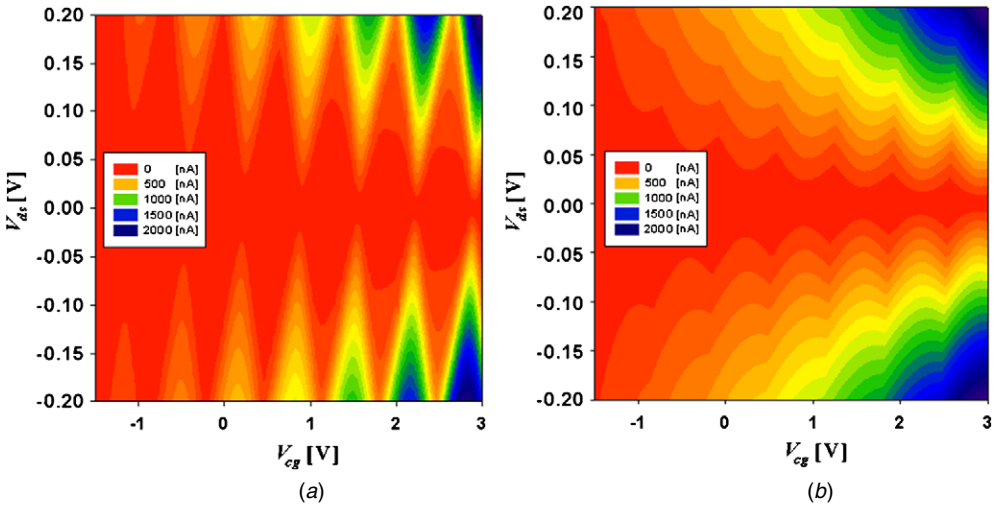

Figure 3. The contour for the absolute value of simulated SET current based on Lee's model. (*a*) $C_{cg} = 0.24$ aF, C_d and $C_s = 0.13$ aF (the case of a high voltage gain) and (*b*) $C_{cg} = 0.24$ aF, C_d and $C_s = 1.3$ aF (the case of a low voltage gain). The legend of (*a*) indicates the absolute value of SET current (Na).

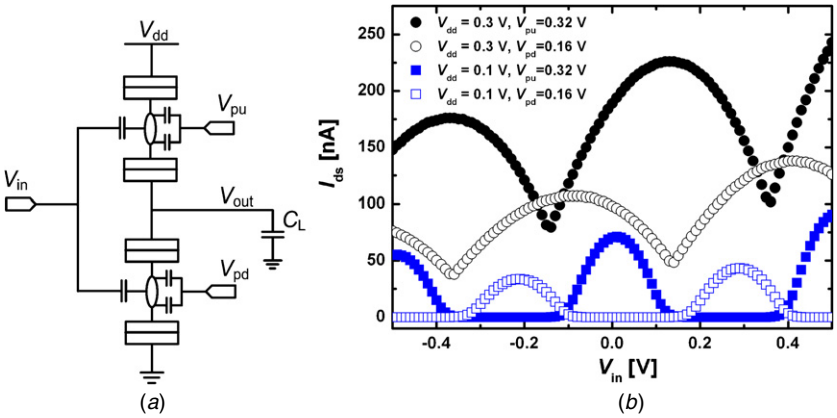

Figure 4. (*a*) Schematic circuit diagram of the static CMOS-like SET inverter. (*b*) The I_{ds}–V_{in} characteristics of the SET inverter at $T = 40$ K. PVCRs are as follows: 2.75 ($V_{dd} = 0.3$ V and $V_{pu} = 0.32$ V), 2.6 ($V_{dd} = 0.3$ V and $V_{pd} = 0.16$ V), 7.3×10^7 ($V_{dd} = 0.1$ V and $V_{pu} = 0.32$ V) and 3.4×10^7 ($V_{dd} = 0.1$ V and $V_{pd} = 0.16$ V), respectively.

inverter and $I_{ds}-V_{cg}$ characteristics of two SETs composing CMOS-like inverter, respectively. The complementary operation of DG-SET can be based on the phase of the Coulomb oscillation in the $I_{ds}-V_{cg}$ characteristic controlled by V_{sg}. Figure 4(*b*) shows that two identical SETs are available as pull-up and pull-down switches by tuning the respective V_{sg} of the two SETs (V_{pu} and V_{pd}), as is the case in the static CMOS inverter. When the upper SET turns ON, the lower SET turns OFF because SET has the inherent Coulomb oscillation characteristic with the period of q/C_{cg}. Circuit parameters in the simulation are as follows: the supply voltage $V_{dd} = 0.1 \sim 0.3$ V, $V_{pu} = 0.32$ V, $V_{pd} = 0.16$ V, $C_{cg} = 0.32$ aF (corresponding to $S_{sg} = 53$ nm), $C_{sg} = 0.28$ aF, capacitances of tunnel junctions $C_s = C_d = 0.04$ aF, resistances of tunnel junctions $R_s = R_d = 1$ MΩ, and the load capacitance $C_L = 0.1$ aF. In our previous work [19, 38], the tunnel junction parameters were found to be reproducible and controllable by using sidewall depletion gates, irrespective of the island size.

Figure 5 shows the transient response of the static CMOS-like SET inverter at $V_{dd} = 0.1 \sim 0.3$ V and $T = 40$ K. The inverter characteristic is successfully demonstrated and its voltage gain is determined by the value of C_{cg}/C_d. We note the shrunken voltage swing of the output as shown in figure 5. It is because that the PVCR of the SET becomes smaller as the temperature or V_{dd} increases. This degradation of PVCR has been commonly observed in the experimental data of Si-based SETs [31–42], and fully considered in our model as non-ideal effects. Furthermore, the shrunken output voltage swing (figure 5(*b*)) means that the signal becomes attenuated as the number of SET inverter stages increases even in the case of $C_{cg}/C_d = 8$, which is its inherent limitation. Therefore, the logic scheme of the static CMOS-like SET inverter inherently seems not to be promising, considering non-ideal effects.

Conclusively, although its complementary operation is useful, the static CMOS-like SET logic is considerably pessimistic due to a low current drivability, a low voltage gain, the degradation of PVCR followed by the small voltage swing of the output signal. Dissipated average power is observed to be 12 nW at $V_{dd} = 0.3$ V and 1.9 pW at $V_{dd} = 0.1$ V (PVCR = 2.6–2.75 at $V_{dd} = 0.3$ V and $3.4 \times 10^7 \sim 7.3 \times 10^7$ at $V_{dd} = 0.1$ V). Nevertheless, the merit of ultra-low power dissipation

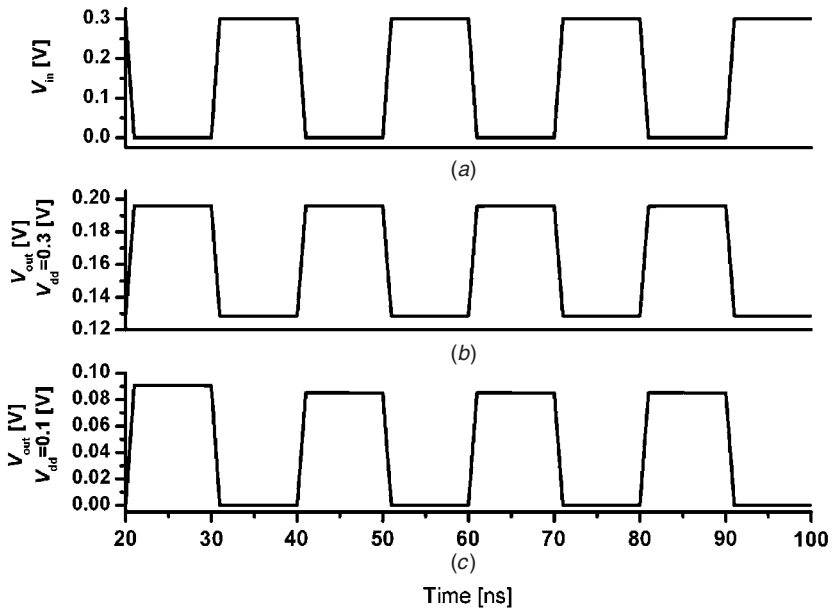

Figure 5. Simulated input–output transient characteristics of the inverter SET logic gate at $T = 40$ K. (*a*) The waveform of the input signal V_{in}, (*b*) the waveform of V_{out} at $V_{dd} = 0.3$ V and (*c*) the waveform of V_{out} at $V_{dd} = 0.1$ V. Parameters used in the SPICE simulation: $V_{pu} = 0.32$ V, $V_{pd} = 0.16$ V, $C_{cg} = 0.32$ aF (corresponding to $S_{sg} = 53$ nm for Si island size), $C_s = C_d = 0.04$ aF, $C_{sg} = 0.28$ aF, $C_L = 0.1$ aF, and $R_s = R_d = 1$ MΩ.

at $V_{dd} = 0.1$ V is diluted by abovementioned limitation of SET inverter scheme.

Here, the dissipated average power is defined by a simple product of V_{dd} and the average current through SET circuit between the common V_{dd} and ground. And then, the effect of interconnection *RC* is assumed to be negligible due to large R_s and R_d. The influence of interconnection on the power dissipation will be discussed in section 4.

3.2. Dynamic SET/MOSFET hybrid logic

In order to confirm the robustness of the operation in a static CMOS-like SET inverter, the precise control of Coulomb oscillation phases of the two SETs is strongly required. Taking the capacitance mismatch induced by the process variation and/or background charges into account, the drawback of the static CMOS-like approach becomes more significant as the number of SETs increases. With these motivations, the dynamic SET/MOSFET hybrid logic has already been demonstrated [38]. Figure 6(*a*) shows the circuit diagram of the dynamic SET/MOSFET hybrid NOR gate. Whenever V_{pre} is LOW (the precharge period), the output node V_{out} is charged up to V_{dd}, and the setup of two input signals (V_{in1} and V_{in2}) is performed. During the evaluation period (V_{pre} is HIGH), V_{out} is determined by the combination of V_{in1} and V_{in2} as a NOR function. The merit of the dynamic NOR logic is that the full voltage swing of V_{out} is possible even with a considerable SET valley current. On the other hand, the demerits is that the pull-down speed is limited by the low current drivability of SETs, and a serious feed-through arises because the capacitance of output node is relatively larger than that of the SET tunnel junctions. The simulated transient response of the dynamic NOR gate at $V_{dd} = 0.1$ V and T = 40 K is shown in figure 6(*b*) for circuit parameters with $C_{cg} = 0.32$ aF, $C_s = C_d = 0.04$ aF, $C_{sg} = 0.28$ aF, $C_L = 10$ fF and $R_s = R_d = 1$ MΩ. It is noticeable that intended mismatch between the input (V_{in1} and V_{in2}) HIGH (=0.3 V) and the output (V_{out}) HIGH (=0.1 V = V_{dd}) plays a significant role of giving the flexibility in design and optimization of SET capacitance. The HIGH-to-LOW logic delay is large due to the large load capacitance on the output node, which is required for suppression of the serious feed-through. Dissipated average power is observed to be 1.3 nW at $V_{dd} = 0.1$ V (PVCR = 3.4×10^7–7.3×10^7 at $V_{dd} = 0.1$ V).

3.3. Cellular nonlinear network (CNN) logic gate

Neural networks derived from neurobiology and adapted to integrated electronics have key features such as parallel processing, continuous time dynamics and global interaction of network elements. Some applications of neural networks include linear and nonlinear programming, associative memory, pattern recognition and computer vision. A new cellular nonlinear network (CNN) architecture, first proposed by Chua and Yang [21, 22], is a parallel computer network with exceptional speed and power performance, and has broad applications in the image and video signal processing, robotic and biological vision. A basic unit of the CNN is called as a *cell*. In its usual implementation based on the CMOS technology, it consists of linear resistors, capacitors, linear and nonlinear controlled sources and independent sources. Each cell is a dynamic system with an input, an output and a state evolving in relation to dynamical laws. A cell is coupled to neighboring cells and may interact directly with other cells within the sphere of influence.

Based on the circuit proposed by Goosens *et al* the SET realization of this 'neuron' is schematically illustrated in

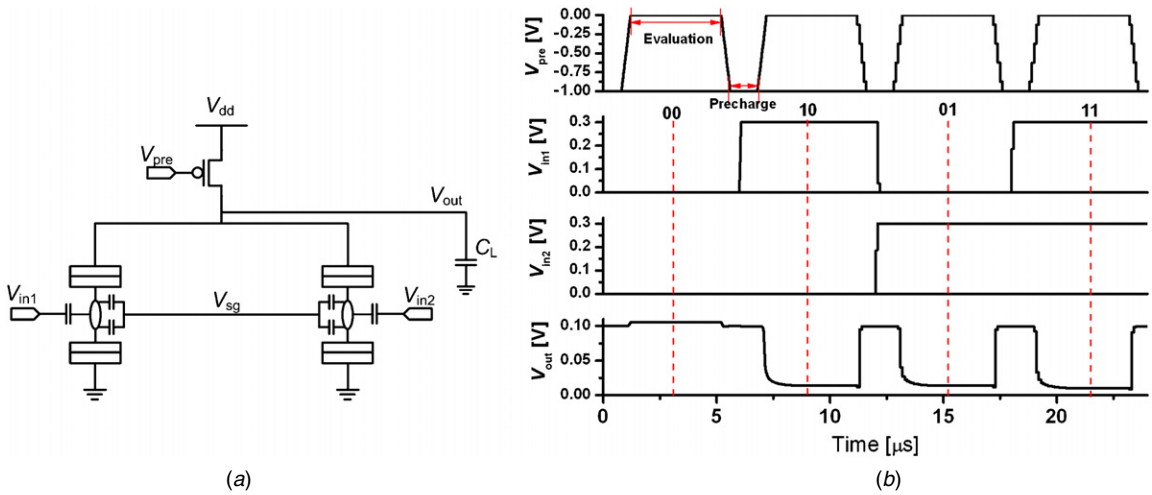

Figure 6. (*a*) Schematic circuit diagram of the dynamic SET/MOSFET hybrid NOR gate. (*b*) Simulated input–output transient characteristics of the dynamic SET/MOSFET hybrid NOR gate at $T = 40$ K. Parameters used in the SPICE simulation: $V_{dd} = 0.1$ V, $V_{sg} = 0.16$ V, $C_{cg} = 0.32$ aF (corresponding to $S_{sg} = 53$ nm), $C_s = C_d = 0.04$ aF, $C_{sg} = 0.28$ aF, $C_L = 10$ fF, and $R_s = R_d = 1$ MΩ. (PVCR = 3.4×10^7–7.3×10^7 at $V_{dd} = 0.1$ V).

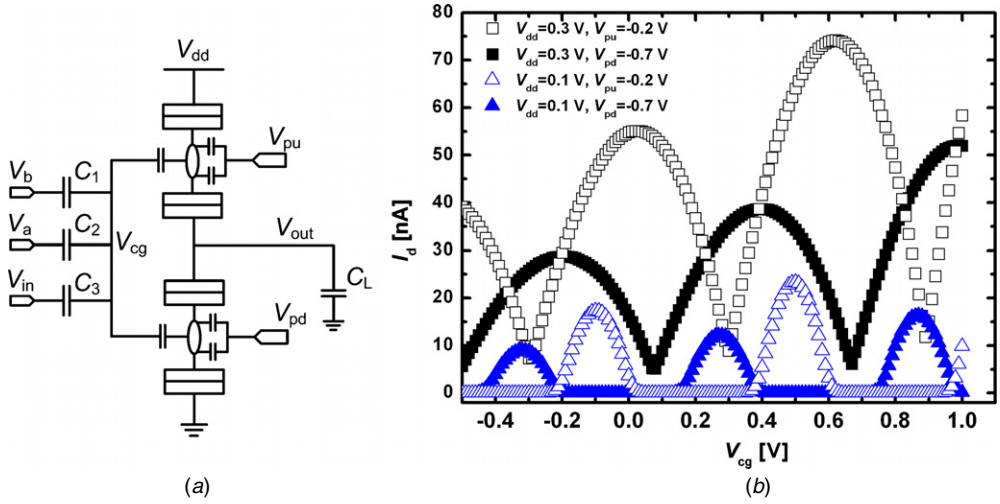

Figure 7. (*a*) Equivalent circuit diagram of a CNN gate. (*b*) The I_{ds}–V_{cg} characteristics of SET composing CNN logic gate at $T = 40$ K. PVCRs are as follows: 7.43 ($V_{dd} = 0.3$ V and $V_{pu} = -0.2$ V), 7.45 ($V_{dd} = 0.3$ V and $V_{pd} = -0.7$ V), 5×10^7 ($V_{dd} = 0.1$ V and $V_{pu} = -0.2$ V), and 3.4×10^7 ($V_{dd} = 0.1$ V and $V_{pd} = -0.7$ V), respectively.

figure 7(*a*) [51]. It consists essentially of static CMOS-like SET inverters discussed above providing a bistable behavior similar to a CMOS transducer element. It has multiple capacitive inputs to the inverter in order to form a summing node such that the input voltage is the weighted sum of the external voltages determined by the capacitance value of each input signal. Figure 7(*b*) shows I_{ds}–V_{cg} characteristics of a SET composing CNN gate at $T = 40$ K. The complementary switching of the SET current is successfully demonstrated by modulating V_{pu} (and/or V_{pd}). In addition, we note that a considerable valley current is observed even at $T = 40$ K due to non-ideal effects in real SETs. The transient response of CNN logic gate is demonstrated in figure 8. When $V_{in} = V_{dd}$ (HIGH), the CNN logic gate is operated as NAND gate with two inputs (V_a and V_b). Only when both V_a and V_b are HIGH, V_{out} becomes LOW as shown in figure 8. Therefore, NAND operation is successfully demonstrated in our simulation results including non-ideal effects in real Si-SETs. The dissipated average power is 1.1 and 3.7 nW at $V_{dd} = 0.1$ and 0.3 V, respectively, with PVCRs: 7.43–7.45 at $V_{dd} = 0.3$ V and 3.4×10^7–5×10^7 at $V_{dd} = 0.1$ V and SET parameters: $C_{cg} = 0.27$ aF (corresponding to $S_{sg} = 45$ nm), $C_s = C_d = 0.1$ aF, $C_{sg} = 0.1$ aF, $R_s = R_d = 1$ MΩ, $C_L = 0.1$ aF, and $C_{1,2,3} = 2.3$ aF. Here, the effect of interconnection *RC* is also assumed to be negligible due to large R_s and R_d.

3.4. Binary decision diagram (BDD)

While the BDD structure proposed by Asahi *et al* was based on the electron-transfer circuit known as a single-electron pump [17], the BDD unit device shown in figure 9(*a*) uses SETs as switches. In the single-electron pump, only a single electron is used as a messenger. Therefore, the amplitude of the output signal is determined only by the clock frequency. However,

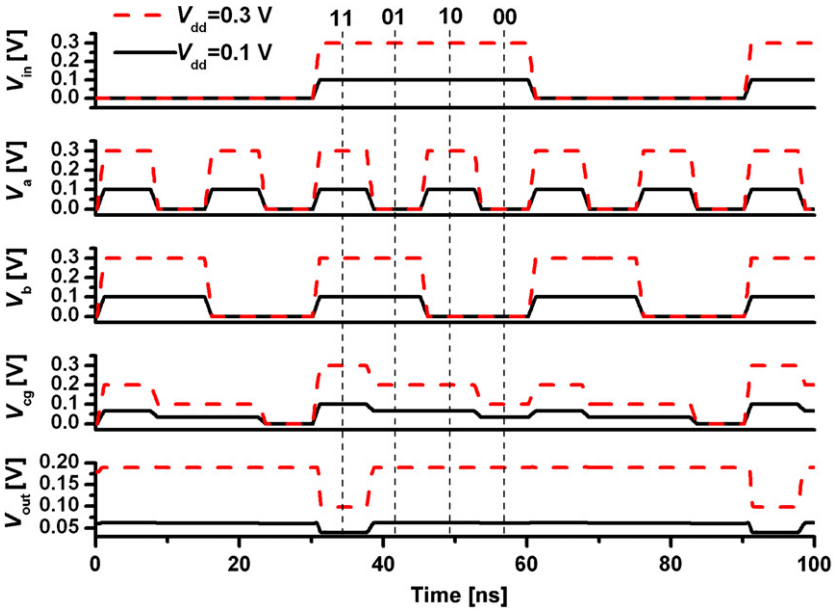

Figure 8. Simulated transient response of the CNN NAND gate at $T = 40$ K and $V_{dd} = 0.3$ and/or 0.1 V with SET parameters: $C_{cg} = 0.27$ aF (corresponding to $S_{sg} = 45$ nm), $C_s = C_d = 0.1$ aF, $C_{sg} = 0.1$ aF, $R_s = R_d = 1$ MΩ, $C_L = 0.1$ aF and $C_{1,2,3} = 2.3$ aF.

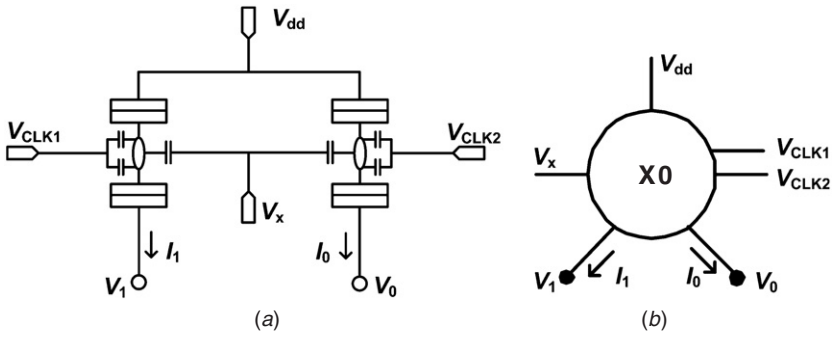

Figure 9. (*a*) The schematic diagram of the BDD unit and (*b*) its circuit symbol.

in this study, the amplitude of the output signal is determined by both the clock frequency and the bias condition, and a few electrons are transferred in 1 clock cycle. Although a single-electron pump has the merit of ultra-low power consumption, it is very difficult to implement. On the other hand, the concept of the BDD operation based on the electrical depletion of the conduction channel has already been demonstrated in a gated narrow wire defined in the δ-doped GaAs channel [18]. While they have been biased on two conditions (a pinch-off and a lift of a Coulomb blockade), SETs in our case are biased on three operational conditions; a pinch-off, the 'ON' state and the 'OFF' state of the SET.

General Boolean functions can be implemented by using the SET-based BDD structure. Figure 9 shows a symbol and the circuit diagram of the unit device for a BDD logic circuit implemented by two DG-SETs. In order to eliminate errors by unwanted tunneling events, the transfer of a single electron in the other unit devices should be synchronously blocked when the input voltage, V_x, is applied to one unit device synchronously with the clock signal V_{clk}. This requirement is guaranteed in our structure by applying a large negative V_{clk} to the sidewall depletion gates without an additional pass gate for the clock signal. The V_x-dependence of the currents in two SETs composing the BDD unit device (under a fixed V_{dd}) is shown in figure 10. When $V_{clk1} = V_{clk2} = -2$ V, the transfer of a single electron through the BDD unit is fully blocked irrespective of V_x. During the evaluation period, by controlling V_{clk1} and V_{clk2} as the sidewall depletion gate voltage V_{sg} ($V_{clk1} = -0.56$ V and $V_{clk2} = -0.13$ V in our case), the SET current would flow through one '1' and '0' branches (I_1 and I_0) controlled by V_x. PVCRs are as follows: $I_0 = 1.12 \times 10^7$ ($V_{dd} = 0.1$ V and $V_{clk} = -0.13$ V), $I_1 = 4.6 \times 10^7$ ($V_{dd} = 0.1$ V and $V_{clk} = -0.56$ V), $I_0 = 1.54 \times 10^3$ ($V_{dd} = 0.2$ V and $V_{clk} = -0.13$ V) and $I_1 = 2.09 \times 10^3$ ($V_{dd} = 0.2$ V and $V_{clk} = -0.56$ V), respectively.

Figure 11 shows the simulated transient response of I_1 and I_0 as a function of V_X, V_{clk1}, and V_{clk2}. Nonzero I_1 flows only when V_X is 'HIGH', and vice versa, which is the core operation of the BDD unit. SET parameters used in SPICE simulation are as follows: $C_{cg} = 0.25$ aF (corresponding to $S_{sg} = 42$ nm), $C_s = C_d = 0.15$ aF, $C_{sg} = 0.1$ aF, and $R_s = R_d = 1$ MΩ. Especially, the overshoot at $V_{dd} = 0.1$ V is clearly observed in I_0. It can be attributed to the capacitive coupling between the Si island potential and V_{sg}, which dominates in a

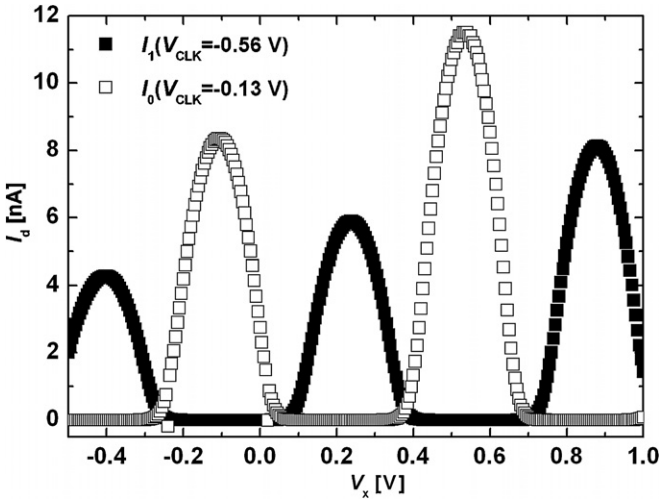

Figure 10. The V_x dependence of the currents of two SETs ($V_{dd} = 0.1$ V) composing the BDD unit. PVCRs are as follows: $I_0 = 1.12 \times 10^7$ ($V_{dd} = 0.1$ V and $V_{clk} = -0.13$ V), $I_1 = 4.6 \times 10^7$ ($V_{dd} = 0.1$ V and $V_{clk} = -0.56$ V), $I_0 = 1.54 \times 10^3$ ($V_{dd} = 0.2$ V and $V_{clk} = -0.13$ V), and $I_1 = 2.09 \times 10^3$ ($V_{dd} = 0.2$ V and $V_{clk} = -0.56$ V), respectively.

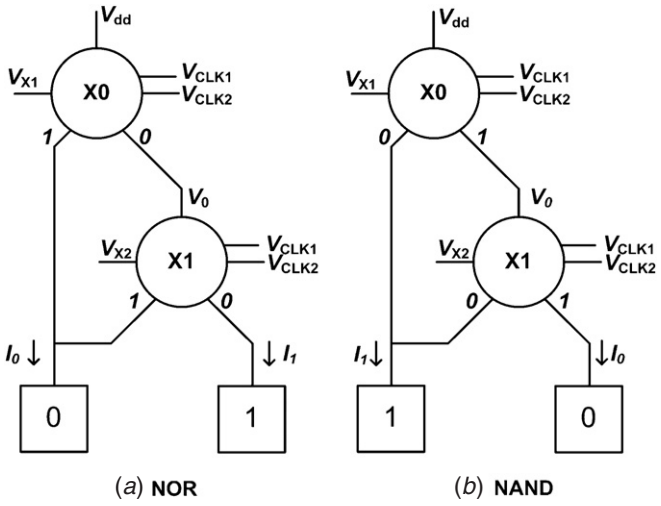

Figure 12. Two-input BDD architectures (*a*) NOR and (*b*) NAND.

low V_{dd} (=0.1 V) rather than a high V_{dd} (=0.2 V) as seen in figure 11. Actually, in the case of the BDD logic gate, the clock V_{clk} (=V_{sg}) swing is larger than those of V_X and V_{dd}. Therefore, more detailed optimization of C_{cg}/C_{sg}, C_d/C_{sg}, and the rising and falling time of V_{clk} is required for further reduction of the delay and power consumption.

Here, it should be noted that the state variable of the signal is not the voltage but the current. It means that the concept of BDD is more suitable to the SET-based logic application, because the drawback of a low current drivability and voltage gain becomes less conspicuous. Actually, using current as a state variable on behalf of the voltage has been one promising stream exploring the breakthrough for post-CMOS signal processing in the fields of the neural network, bio-inspired network and parallel processing.

Based on the operation of BDD unit in figure 9, two-input BDD NOR and NAND circuits are implemented as shown in figure 12. Finally, figure 13 shows the simulated input–output transient characteristics of BDD NOR and NAND logic gates at $T = 40$ K and $V_{dd} = 0.1$ V. SET parameters used in SPICE simulation are $C_{cg} = 0.25$ aF (corresponding to $S_{sg} = 42$ nm), $C_s = C_d = 0.15$ aF, $C_{sg} = 0.1$ aF and

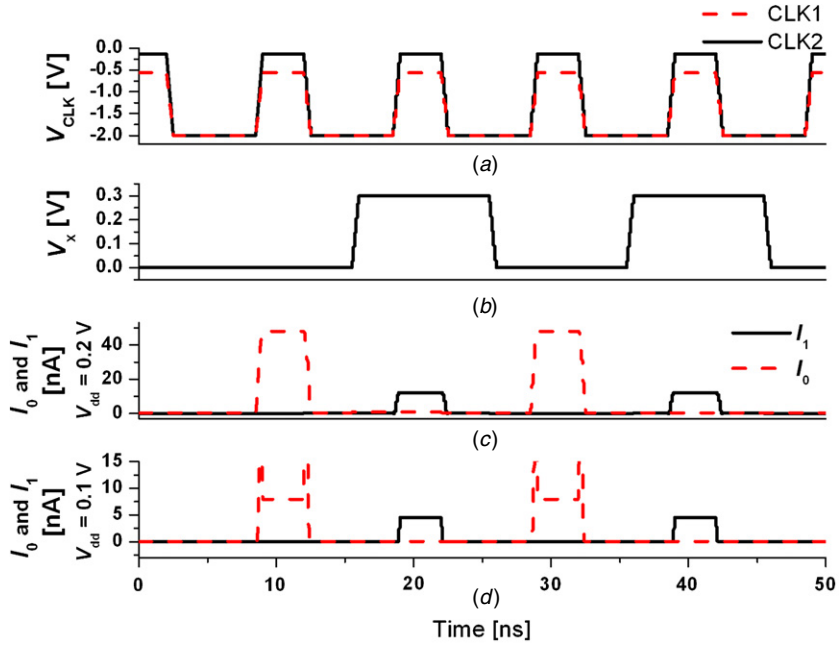

Figure 11. Simulated input–output transient characteristics of BDD unit at $T = 40$ K, $V_{dd} = 0.1$ and/or 0.2 V. Parameters used in SPICE simulation are as follows: $C_{cg} = 0.25$ aF (corresponding to $S_{sg} = 42$ nm), $C_s = C_d = 0.15$ aF, $C_{sg} = 0.1$ aF and $R_s = R_d = 1$ MΩ.

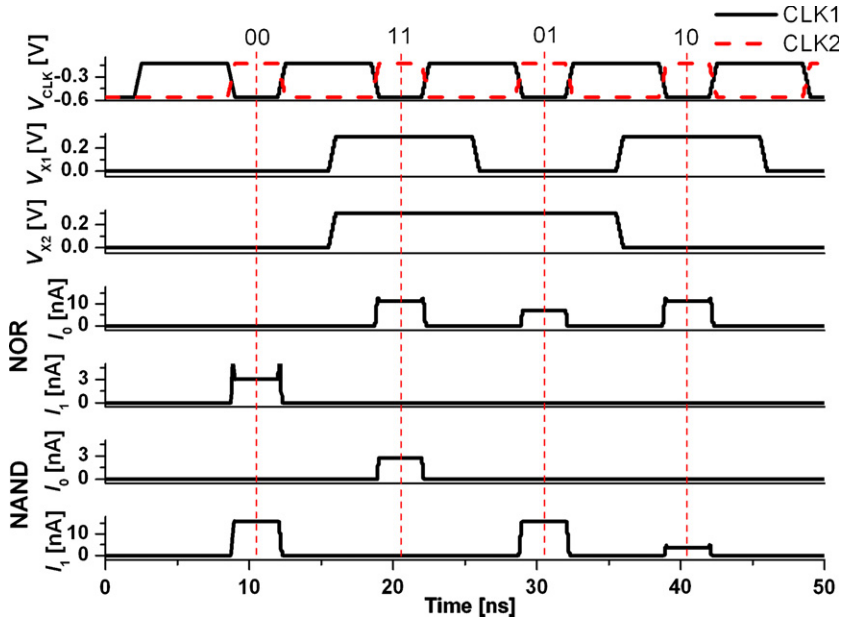

Figure 13. Simulated input–output transient characteristics of BDD NOR and NAND logic gates at $T = 40$ K and $V_{dd} = 0.1$ V. Parameters used in SPICE simulation are $C_{cg} = 0.25$ aF (corresponding to $S_{sg} = 42$ nm), $C_s = C_d = 0.15$ aF, $C_{sg} = 0.1$ aF, and $R_s = R_d = 1$ MΩ.

$R_s = R_d = 1$ MΩ. Only when both V_{X1} and V_{X2} are LOW, nonzero I_1 flows, which is the BDD NOR operation. Likewise, only when both V_{X1} and V_{X2} are HIGH, nonzero I_0 flows, which is the BDD NAND operation. Therefore, robust operations of both NOR and NAND logic are successfully demonstrated in our simulation results including non-ideal effects in real Si-SETs. The overshoot, as discussed in figure 11, is again observed in I_1. The dissipated average power is 0.29 nW (NOR) and 0.27 nW (NAND) at $V_{dd} = 0.1$ V, respectively, neglecting the interconnection *RC* effect. Considering that the SPICE model includes non-ideal effects in real Si SETs, the result in figure 13 is estimated to be very impressive.

4. Comparative description

In this section, the candidates for SET-based energy-efficient logic gates are enumerated and compared based on SPICE simulation results fully considering the non-ideal effects in real Si-based SETs. The performance parameters are summarized in table 1. Dissipated powers are compared for the input frequency $f_{in} = 50$ MHz except the dynamic NOR with $f_{in} =$ 830 kHz. Considering that the power dissipated in the CMOS inverter at $V_{dd} = 1$ V and $f_{in} = 50$ MHz is about a few hundreds of nW, that in the BDD NOR logic gate of 0.29 nW at V_{dd} $= 0.1$ V and $f_{in} = 50$ MHz is dramatically energy efficient. Although the power dissipation in SET inverter with $V_{dd} =$ 0.1 V is very much smaller than that in the BDD logic gate with $V_{dd} = 0.1$ V, CMOS-like SET inverter is not preferable due to an output swing sensitive to V_{dd} and the temperature followed by the signal attenuation, as abovementioned. In contrast, the BDD-based logic gate can operate even at a low PVCR because the difference of two current (I_0 and I_1) in a specific branch only has to be recognizable. In addition, in the case of series connection of two or three SET inverters (e.g., CMOS-like SET NAND/NOR gate), the supply voltage

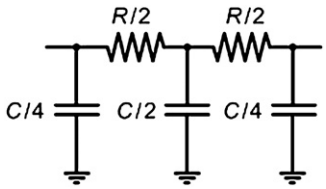

Figure 14. Used interconnection RC model.

V_{dd} is hard to be shrunken. Actually, the ultra-low power dissipation in BDD logic circuits is mainly due to the ability to reduce V_{dd}, thanks to their current-based description of logic states. Furthermore, the design and optimization become more flexible due to the release of the compromise between a voltage gain ($\sim C_{cg}/C_d$) and input level ($\sim q/C_{cg}$) because the limitation of a low voltage gain becomes insignificant.

On the other hand, in order to consider the interconnect *RC* effect, the *RC* model in figure 14 was applied to all internal interconnections in various logic circuits. Dissipated average power with interconnection *RC* (within the range of $C = C_{tot} \sim 10 \times C_{tot}$ and $R = 0.001 \times R_d \sim R_d$ defined in figure 14) P_2 is summarized in comparison with one without interconnection *RC*, i.e., P_1. It is found that P_1/P_2 has the value within the range of 0.76–1, as shown in table 1. Therefore, most of power is confirmed to be dissipated not in the interconnection but in SET itself. It is interesting that the $P_1/P_2 > 1$ is observed only CNN logic, which should be investigated as further studies. In addition, P_2 of the CNN NAND gate at $V_{dd} = 0.1$ V cannot be acquired due to the logic function fail as shown in table 1. Actually, it is also the reason that the global interconnections are excluded and only local ones are used in CNN-based neural network circuitry.

In addition, now, two points should be discussed. One is that SET parameters are different one another in various

Table 1. Comparison of performance parameters in various SET-based ultra-energy-efficient logic gate circuits.

Performance parameters	SET inverter	Dynamic NOR	BDD (NOR/NAND)	CNN NAND
Supply voltage, V_{dd} (V)	0.1/0.3	0.1	0.1	0.1/0.3
Input range (V)	0–0.3	0–0.3	0–0.3	0–0.3
Input Frequency, f_{in} (MHz)	50	0.83	50	50
Total capacitance, C_{tot} (aF)	0.68	0.68	0.65	0.57
Control gate capacitance, C_{cg} (aF)	0.32	0.32	0.25	0.27
Depletion gate capacitance, C_{sg} (aF)	0.28	0.28	0.1	0.1
Tunnel junction capacitance, C_s, C_d (aF)	0.04	0.04	0.15	0.1
Load capacitance, C_L	0.1 aF	10 fF	–	0.1 aF
Tunnel junctions resistance, R_s, R_d (MΩ)	1	1	1	1
Peak to Valley Current Ratio, PVCR	3.4×10^7–$7.3 \times 10^7/2.6 \sim 2.75$	3.4×10^7–$7.3 \times 10^7/2.6 \sim 2.75$	1.12×10^7–4.6×10^7	3.4×10^7–$5 \times 10^7/7.43$– 7.45
Temperature (K)	40	40	40	40
Dissipated power, P_1 (nW) (Without interconnection *RC*)	0.0019/12	1.3	0.29/0.27	1.1/3.7
Dissipated power, P_2 [nW] (With interconnection *RC*)	0.0025/12	1.3	0.29/0.29	–/1.96
P_1 / P_2	0.76/1	1	1/0.93	–/1.88
Delay (ns)	0.2/0.1	20	0.6/0.6	0.8/0.9
Maximum operation frequency, f_{max} (MHz)	50	0.83	100	66

SET logic circuits, which leaves behind the fairness issue in this work. However, in terms of different parameters, the discrepancy of logic schemes should be considered. In cases of SET inverter and CNN logic, the scale-down of V_{dd} should be followed by the reduction of output swing. Thus, the compromise with output swing is inevitable because the output in first stage becomes the input in the next stage of logic gate chains in the case of SET inverter and/or CNN logic. Moreover, compared with the SET inverter, in the case of CNN logic, multiple inputs are available. Therefore, the configuration of island charge (eventually the peak current through the unit SET) is different from each other between SET inverter and CNN logic, even if V_{dd}, R_s and R_d are exactly the same. On the other hand, the total capacitance C_{tot} of SET is the critical parameter playing significant roles of determining the operation temperature, energy efficiency, state-of-the-art process technology and chip density. Therefore, in this work, the parameters (SET capacitance, V_{sg}, etc) have been optimized with the pre-assumption of nearly the same total capacitance ($C_{tot} = 0.57 \sim 0.68$ aF irrespective of logic gate type (as in table 1)). Consequently, SET capacitance parameters and V_{sg} (eventually R_s and R_d) become different from each other. In conclusion, we have chosen the criteria of not mechanically the same parameter but actual circuit environments in really implemented and optimized for the minimum power dissipation.

The other is that compared with CNN gate, the dissipated average power is very sensitive to V_{dd} in the SET inverter, as shown in table 1. In terms of the V_{dd}-sensitive power consumption of SET inverter, needless to say, it is because that PVCR is sensitive to V_{dd}, which is also the same for CNN and BDD logic gates. Actually, it was found that short circuit current-induced dc power dissipation was dramatically reduced at $V_{dd} = 0.1$ V compared with that at $V_{dd} = 0.3$ V, in our simulation of the SET inverter. However, in the case of CNN NAND gate, considerable dc power dissipation was observed even at $V_{dd} = 0.1$ V as shown in table 1. It can be explained as follows: in CNN NAND gate (here, V_{in} tied to '1'), the V_{cg} value (i.e., the configuration of Si island charge) has three cases corresponding to V_a and V_b ('00', '01/10' and '11'), whereas the V_{in} value in the SET inverter has only two cases ('0' and '1'). So the CNN logic gate is more frequently placed in the state flowing a relatively larger short circuit current ('01' and '10') than CMOS-like SET inverter, as shown in figure 8. In addition, in the case of the CNN NAND gate, it appears that the output swing becomes reduced even at $V_{dd} = 0.1$ V as seen in figure 8. Eventually, instead of being more immune to PVCR, the dissipated power of multi-input CNN logic with high PVCR ($V_{dd} = 0.1$ V) is larger than that of SET-inverter with high PVCR ($V_{dd} = 0.1$ V). On the other hand, the BDD logic scheme is not only more robust to a low PVCR than SET inverter and CNN logic as mentioned in section 3.1, but also more immune to a low V_{dd} (except for the optimization issue of current overshoot), as mentioned in the first paragraph in section 4.

Conclusively, our results show that the BDD logic circuit is the most promising solution in the power consumption, the logic speed and the robustness compared with the static CMOS-like SET logic, the dynamic SET/CMOS hybrid logic and CNN logic. Therefore, a transition of the paradigm substituting the voltage with the current as a state variable in the signal processing is strongly required and further study is necessary. In this case, needless to say, appropriate differential current sense amplifiers are required for the interface between two state variables, i.e., the current and the voltage.

5. Conclusions

The performance and power consumption of various SET technology-based ultra-energy-efficient logic gate circuits are comparatively investigated by using Lee's SPICE model including non-ideal effects in really implemented SETs for the first time. Compared with the static CMOS-like SET logic, the dynamic SET/CMOS hybrid logic and the CNN logic, the BDD logic circuit is found to be the most promising

in the dissipated power of 0.29 nW at $V_{dd} = 0.1$ V and $f_{in} = 50$ MHz, which is lower by three orders of magnitude than that of the CMOS inverter with the same f_{in}. Our results show the feasibility of the current-based circuit scheme in ultra-energy-efficient SET-based post-CMOS signal processing algorithm.

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