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Highly Stable Transparent Amorphous Oxide Semiconductor Thin-Film Transistors Having Double-Stacked Active Layers

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Recently, amorphous oxide semiconductors (AOSs) have extensively been studied for applications as display devices because AOSs have many advantages over conventional amorphous and polycrystalline silicon that are used for the channel layers of thin-film transistors (TFTs).[1] As a representative AOS material, amorphous gallium-indium-zinc-oxide (a-GIZO) has intensively been studied as an active layer of TFTs for switching/driving devices in active-matrix liquid crystal display (AMLCD) and active-matrix organic light-emitting diode display (AMOLED) backplanes [2–5] because of its advantages, such as a good short-range uniformity, a high field-effect mobility (μ_{FE}), a large area uniform integration, a low cost and low temperature fabrication process, transparency, etc. Therefore, AOSs can be used in novel application areas, including transparent and/ or flexible electronic devices. Up until now, many prototype active-matrix displays have been demonstrated, including 12.1 inch wide extended graphics array (WXGA) OLED displays,[2] 15 inch XGA AMLCDs,[3] 4.0 inch quarter video graphics array (QVGA) AMOLEDs,[4] 3.5 inch quarter common intermediate format (QCIF) OLED displays,[5] 2 inch flexible black-and-white electronic papers (e-papers),[6] 4 inch front-drive structure full-color e-papers,[7,8] and flexible OLED displays that are fabricated on a 100-μm-thick stainless steel foil.[9] Now, the main research in this area focuses on attaining an improved long-term stability [10–14] in terms of the application-dependent manufacturabilities. For example, the driving current-induced threshold voltage (V_T) shift (ΔV_T) should be considered in AMOLED driver TFT applications (T1 in **Figure 1a**).[15] For switching TFTs in AMLCD backplanes (T2 in Figure 1b) and/or AMOLEDs (T2 in Figure 1a), the voltage stress-induced ΔV_T is a very challenging issue that must be taken into account in a pixel circuit design. Preferably, both the high μ_{FE} and low ΔV_T (comparable to the case for hydrogenated amorphous silicon (a-Si:H) TFTs) are indispensible for AOS TFT-based large-area high-resolution AMLCD and AMOLED backplanes.[4,16] For the bias stress-induced ΔV_T, the switch TFTs were mainly subjected to the negative gate-to-source voltage (V_{GS}) and the positive drain-to-source voltage (V_{DS}) stresses (TFTs in the off-state) under an ambient white light from a backlight unit in real AMLCD and/ or AMOLED display applications (called negative bias illumination stress: NBIS). Therefore, the NBIS stability should be guaranteed because the bias condition of the switch TFTs is in the off-state with illumination during most of the operation time in practical display pixel operation.

On the other hand, very recently, amorphous hafnium-indium-zinc-oxide (a-HIZO) TFTs have been proposed and developed as stability-enhanced AOS TFTs.[17–19] Previous reports have shown that higher amounts of Hf in the active thin films resulted in a better stability, given an identical device structure. The addition of Hf can suppress the growth of the columnar structure and drastically decrease the carrier concentration/hall mobility in the a-HIZO films. Additionally, the Hf ions might play a key role in improving the instability of the TFTs because of their high oxygen bonding ability.[17] Furthermore, the subgap density-of-states (DOS) of a-HIZO is lower than the a-GIZO thin film.[18,19] However, unfortunately, the increase in the Hf composition deteriorates the mobility and the carrier concentration.[18]

Motivated by this background information, this work used a double-stacked active layer for the first time in a-HIZO TFTs in order to obtain both a high performance as well as a good electrical/optical stability. Excellent electrical properties (high μ_{FE} and low subthreshold swing) were maintained even after

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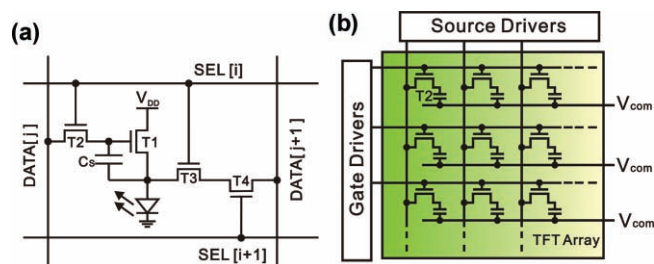Seoul, 136 – 702 (Korea)
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Figure 1. (a) A pixel circuit for the AMOLEDs.[15] (b) A typical TFT array for the AMLCDs.

very severe electrical and optical stress (stress condition under a high negative gate bias as well as an illumination of bright white color (3000 cd m^{-2})) using the Hf content-modulated double-stacked active layers in the TFTs. The overall electrical performance was well suited for the specifications of most display applications, and thus, the method that was presented in this study could readily be adopted in current and future high-performance displays.

A schematic device structure is shown in **Figure 2a**. The a-HIZO TFTs with the most commonly used staggered bottom-gate structure were used in this study. The fabrication details can be found in the Experimental section. In brief, sputtered Mo was used for both the gate and source/drain (S/D) electrodes. The gate insulator (400-nm-thick SiN$_x$/50-nm-thick SiO$_x$) was deposited through plasma-enhanced chemical vapor deposition (PECVD). The active layer (Hf-doped InZnO) was deposited through rf sputtering. Two different types of active layer configurations were employed for the TFTs. One configuration was a typical single-layered HIZO with different Hf contents (nominal thickness of 50 nm), and the other was a double-stacked HIZO

active layer. In the latter case, the active layer consisted of double layers (active 1 (beneath the passivation layer) and active 2 (on the gate insulator)), as schematically illustrated in Figure 2a. Finally, 200-nm-thick SiO$_x$ was deposited as the passivation layer. The cross-sectional transmission electron microscopy (TEM) image and the photograph of the a-HIZO TFTs that were fully processed on a 6-inch glass wafer are shown in Figure 2b and 2c. The gate, insulator, channel, and source/drain layers were well determined with an excellent thickness uniformity as well as a low surface/interface roughness. From the photograph, it is noted that most of the device areas were almost transparent or semi-transparent except for the gate/source-drain/alignment key regions. The geometrical parameters were as follows: T_{GI} (gate insulator thickness) = 400 nm/50 nm (SiN$_x$/SiO$_x$) = 273 nm (equivalent oxide thickness: EOT), W (channel width) = 25 μm, L (channel length) = 5 μm, L_{ov} (gate-to-S/D overlap length) = 10 μm, and $T_{Active1}/T_{Active2}$ (active layer thickness) = 40/10 nm. The thickness ratio of the Hf content-modulated double layers ($T_{Active1}/T_{Active2}$) was optimized using the device simulation, which is described in detail later.

First, the electrical properties of the HIZO TFTs with a single channel layer were examined for different Hf contents (T_{Active} = 50 nm). The Hf contents (x) in HIZO were 0.15 and 0.23 mol.% (denoted as x = 0.15 and x = 0.23). The HIZO TFTs exhibited quite different electrical properties depending on the Hf content. The devices were stressed under a NBIS with a negative gate bias (V_{GS} = −20 V, V_{DS} = 10 V) as well as a photo-illumination (white light with brightness of 3000 cd m^{-2}). Notably, these conditions were very severe compared to the normal operation conditions for AMLCDs and AMOLEDs. A relatively large negative ΔV_T (−2.80 V) was observed for the TFTs where x = 0.15 after the NBIS test for 11 000 s (**Figure 3a**). However, at x = 0.23, a small ΔV_T (−0.91 V) was observed, even though the NBIS was applied (Figure 3b). While the NBIS-induced ΔV_T was smaller for x = 0.23 compared to x = 0.15, the field-effect mobility μ_{FE} and the on current were higher for the HIZO TFT of x = 0.15 as shown in Figure S1. It was found the HIZO active layers with higher Hf contents exhibited a better stability but a poorer mobility than the HIZO TFTs with lower Hf contents. Therefore, there should be a trade-off between the mobility and the stability in HIZO TFTs dependent on Hf contents. The device simulation was carried out using a commercial device simulator in order to determine the nature of the HIZO TFTs with respect to the Hf content. The Hf content (x)-dependent subgap density-of-states (DOS) were incorporated into the device simulation in Figure 3c. The subgap DOS was calculated using the following equations.
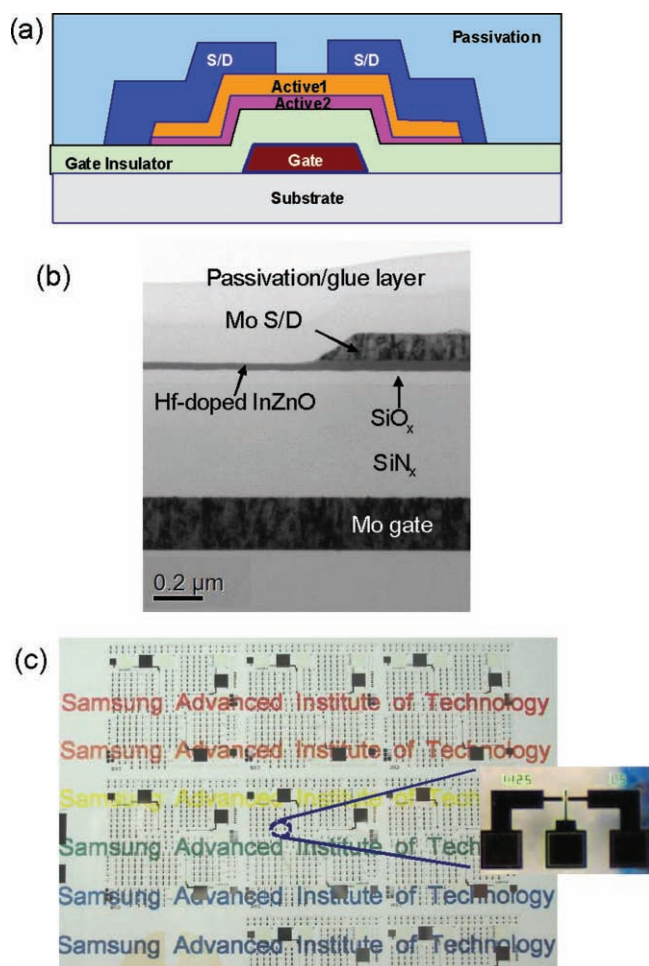

Figure 2. (a) The schematic illustration of the device structure, (b) cross-sectional TEM image of the fabricated device, and (c) photograph of the a-HIZO TFTs that were integrated on the 6-inch glass wafer and a magnified image of the TFT (inset).

$$g_A(E) = N_{TA} \times \exp\left(\frac{E - E_C}{kT_{TA}}\right)$$
$$+ N_{DA} \times \exp\left[-\left(\frac{E_{OA} - E}{kT_{DA}}\right)^2\right] \quad (1)$$

$$g_D(E) = N_{TD} \times \exp\left(\frac{E_V - E}{kT_{TD}}\right)$$
$$+ g_{ov} \times \exp\left[-\left(\frac{E_{Ogov} - E}{kT_{gov}}\right)^2\right] \quad (2)$$
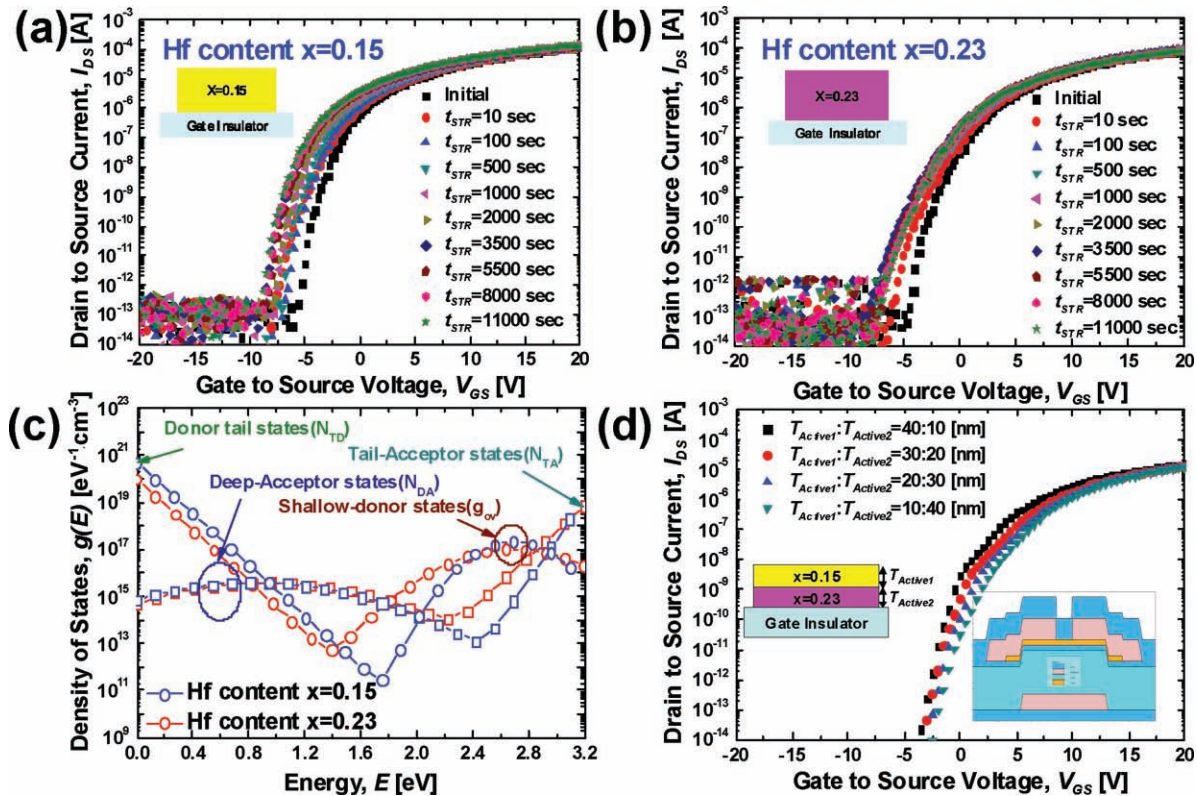
Figure 3. NBIS time-evolutions of the transfer curves for the single-layered active HIZO TFTs with (a) $x = 0.15$ and (b) $x = 0.23$. (c) The Hf content (x)-dependent subgap density-of-states (DOS). (d) The simulation results for the thickness combination ($T_{Active1}/T_{Active2}$)-dependence of the transfer curves. The optimal condition was $T_{Active1}/T_{Active2} = 40$ nm/10 nm. The inset shows the TFT structure that was used in the simulation (for detailed structure, refer to the Supporting Information).

In these equations, N_{TA} is the acceptor-like tail state density, kT_{TA} is the acceptor-like tail state characteristic energy, N_{DA} is the acceptor-like deep state density, kT_{DA} is the acceptor-like deep state characteristic energy, E_{OA} is the acceptor-like deep state average energy (in Gaussian distribution in Eq. (1)), N_{TD} is the donor-like tail state density, kT_{TD} is the donor-like tail state characteristic energy, g_{ov} is the donor state density for the oxygen vacancy and/or hydrogen, kT_{gov} is the donor state characteristic energy for the oxygen vacancy and/or hydrogen, and E_{Ogov} is the donor state average energy (for the Gaussian distribution in Equation (2)). The detailed values of the subgap DOS are listed in **Table 1** (μ_{BAND} = conduction band electron mobility, N_D = thermal equilibrium electron density, N_C = conduction band effective DOS, and N_V = valence band effective DOS). In this model, as the Hf-content x increases, the acceptor-like DOS $g_A(E)$ increases and the donor state density g_{ov} decreases.[18,19]

Additionally, the $T_{Active1}/T_{Active2}$ condition for the thickness of the double active layer was optimized using the simulation results in Figure 3d. The total thickness ($T_{Active1} + T_{Active2}$) was fixed at 50 nm. $T_{Active1}/T_{Active2} = 40$ nm/10 nm exhibited the lowest subthreshold swing and the highest on current. Therefore, this condition was used in the following experiment.

From the experimental and simulation results of HIZO TFTs having a single active layer, a novel device structure could be designed for AOS TFTs. Thus, the double-layered active structure of the TFTs was investigated in order to obtain both a

high mobility as well as a good electrical/optical stability. The effects of the Hf content-modulated active layers on the electrical properties of the TFTs were systematically investigated. Two different active stacks, i.e. structure 1 (STR1) with $x = 0.15$ for active 1/$x = 0.23$ for active 2 and structure 2 (STR2) with $x = 0.23$ for active 1 and $x = 0.15$ for active 2, were fabricated. (The thickness of each layer ($T_{Active1} = 40$ nm/$T_{Active2} = 10$ nm) was optimized using the device simulation shown in Figure 3(d).) **Figure 4a** and b show the transfer curves of the TFTs with the double-layered active structures. We also checked the variation of V_T according to the stress time (t_{STR}) shown in Figure 4c, for the four types of device structures. In this work we used V_{DS} of 10 V to measure the transfer curves and this V_{DS} condition lay in the saturation regime. So V_T was determined from the intercept of a plot of $(I_{DS})^{1/2}$ versus V_{GS} since the relationship in between I_{DS} and V_{GS} follows the equation, $I_{DS} = \frac{WC_i}{2L}\mu\left(V_{GS} - V_T\right)^2$. Figure S2 shows the plots of $(I_{DS})^{1/2}$ versus V_{GS} with different device structures, that were used to calculate the V_T. Notably, STR1 satisfied the indispensible requirements for the AOS TFT-based large-area high-resolution AMLCD and AMOLED backplanes, i.e., high on-current (Figure S1a), high μ_{FE} (≥ 15 cm^2 V^{-1}·s^{-1}) (Figure S1c), and the low NBIS-induced ΔV_T of -2.55 V (Figure 4c). Therefore, STR1 was thought to be the most promising candidate with respect to the trade-off between the electrical performance and the stability. Finally, Figure S1d shows that the simulation results accurately reproduced the

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Table 1. The simulation parameters that were used for device simulation of *a*-HIZO TFTs.

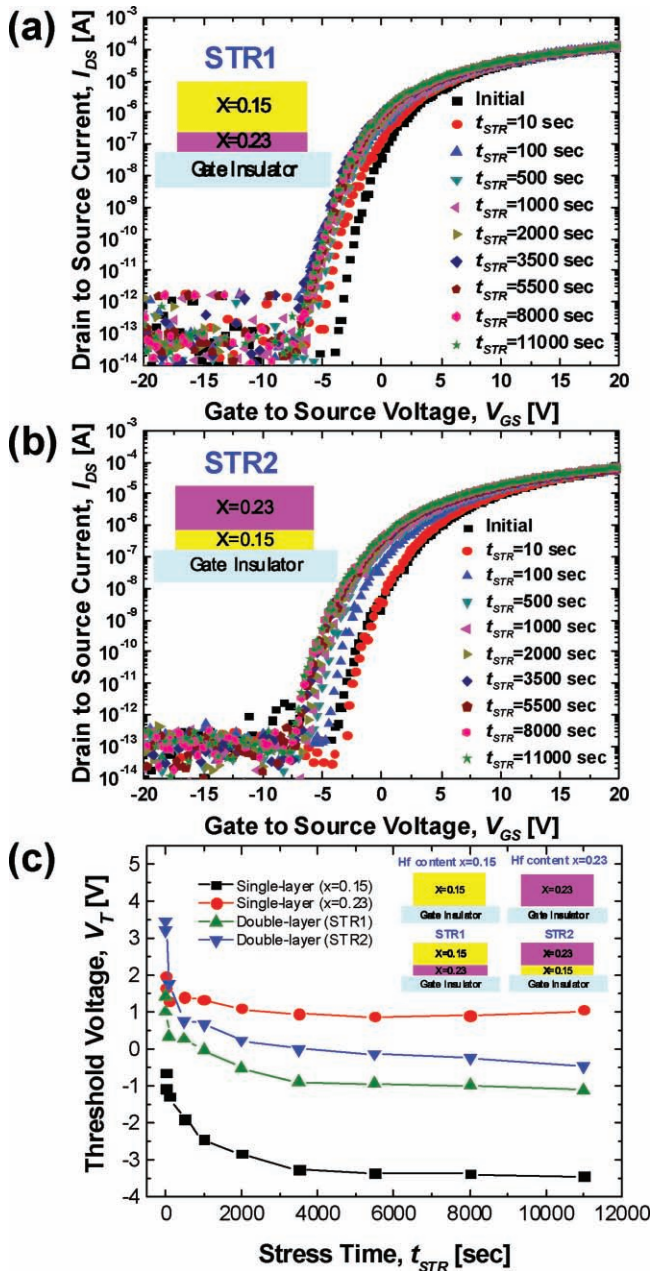|	Hf content $x = 0.23$	Hf content $x = 0.15$		Hf content $x = 0.23$	Hf content $x = 0.15$
N_{TA}	7×10^{18} [cm$^{-3}\cdot$eV^{-1}]	2×10^{18} [cm$^{-3}\cdot$eV^{-1}]	N_{DA}	3.85×10^{15} [cm$^{-3}\cdot$eV^{-1}]	3.85×10^{15} [cm$^{-3}\cdot$eV^{-1}]
kT_{TA}	0.08 [eV]	0.05 [eV]	kT_{DA}	0.65 [eV]	0.65 [eV]
N_{TD}	1×10^{20} [cm$^{-3}\cdot$eV^{-1}]	5×10^{20} [cm$^{-3}\cdot$eV^{-1}]	g_{OV}	1×10^{17} [cm$^{-3}\cdot$eV^{-1}]	2.2×10^{17} [cm$^{-3}\cdot$eV^{-1}]
kT_{TD}	0.08 [eV]	0.08 [eV]	kT_{gov}	0.4 [eV]	0.25 [eV]
N_C	6×10^{18} [cm^{-3}]	6×10^{18} [cm^{-3}]	N_D	1×10^{16} [cm^{-3}]	1×10^{16} [cm^{-3}]
N_V	1×10^{15} [cm^{-3}]	1×10^{15} [cm^{-3}]	μ_{BAND}	17 [cm^2 V$^{-1}\cdot$s^{-1}]	23 [cm^2 V$^{-1}\cdot$s^{-1}]

Figure 4. NBIS time-evolutions of transfer curves of double-layered active HIZO TFTs with (a) structure 1 and (b) structure 2. (c) The NBIS-induced V_T shifts of four kinds of TFT structures.

measured structure-dependent transfer curves before the NBIS (Figure S1b). Therefore, this simulation model and the subgap DOS parameters (Table 1 and Figure 3c) were found to be very reasonable.

It should be noted that NBIS-induced variation of the device transfer characteristics appears as a combination of flat band voltage shift and the subthreshold slope degradation. The former can be reduced by suppressing oxygen vacancies (native defects in *a*-GIZO or *a*-HIZO films) by the Hf doping. With referring to first-principle calculations, the oxygen vacancy-induced deep donor levels can act as the states trapping holes and subsequently diffuse into gate insulator/active thin-film interface.[20,21] They would lead to more significant hole trapping into the gate insulator.[22] As increase of Hf content, the density of oxygen vacancies decreases due to high oxygen bonding ability of Hf (it is also considered in donor tail states in Figure 3c). Therefore, the better stability of TFTs having higher Hf contents is thought to be very reasonable in terms of V_T shifts. Meanwhile, the latter (subthreshold slope degradation) is related to the active bulk/interface defect creation or locally trapped holes. As shown in Figure 3c, it should be noted that our DOS model and simulation results showed that the acceptor tail states increase with the increase of Hf content. As a result the increase of acceptor tail states makes the subthreshold slope degraded accordingly. Although the degradation of subthreshold swing properties is undesirable concomitant with the Hf-based oxygen vacancy control, we think that STR1 is thought to be one of the best solutions for both high performance and good stability because NBIS-induced instability and serious off-current problem (as mentioned above) is dominated by the oxygen vacancy-related hole trapping (i.e., flat band voltage shift) rather than by the subthreshold slope degradation.

The variation of subthreshold swing properties seemed to be worse in case of single layer ($x = 0.23$) & double layer (STR1) than single layer ($x = 0.15$) & double layer (STR2). However, it is noted that the change of swing properties is not severe, and furthermore, all structures showed low subthreshold swing even after severe NBIS stress. In terms of subthreshold swing properties it is also thought that STR2 can be used as a promising TFT structure if the invariant subthreshold swing under NBIS is more important than other parameters. We believe this can be realized by adequate circuit design. Further study is under the way to fabricate transparent oxide semiconductor-based TFTs having high on-current, low leakage current, small V_T shift, and little degradation of subthreshold swing under the NBIS condition by further optimization of processes and device structures based on this work.

In summary, a novel device structure was developed for high-performance and highly stable TFTs using an Hf content-modulated double-layered channel. The Hf contents in HIZO were critical for determining the initial electrical properties as well as the NBIS-induced instability under a real display operation condition. A better stability was observed at higher Hf contents in the HIZO active, but these TFTs had a poorer electrical performance than the HIZO TFTs with lower Hf contents, corresponding to a trade-off between the performance and the stability. Highly stable as well as high performance TFT devices were fabricated using a double-stacked channel with different HF compositions. The approach that was introduced in this communication could potentially be used to fabricate product-level display devices using AOS in the near future.

Experimental Section

Device fabrication: All of the samples were prepared on 6-inch glass substrates (Eagle 2000, Corning Inc.). Prior to the device fabrication, the substrates were chemically cleaned using aqueous mixtures of H_2SO_4–H_2O_2 and then rinsed with deionized water. The bottom-gate and top-contact structured TFTs were fabricated using the standard semiconductor processes. Sputter-deposited Mo was used as both the gate and source/drain (S/D) electrodes. The gate and S/D electrodes were patterned through dry etching. A 400-nm-thick SiN_x/50-nm-thick SiO_x bilayer was used as the gate insulator and was deposited through plasma-enhanced chemical vapor deposition (PECVD) at 370 °C. For the *a*-HIZO active thin-film layer depositions, HIZO targets with different Hf compositions were prepared through the conventional solid-state sintering. The composition of the prepared targets was HfO_2:In_2O_3:ZnO = 0.15:1:2 and 0.23:1:2 mol.%, respectively. The HIZO films were deposited through rf sputtering at room temperature (sputtering gases: Ar/O_2 mixture with a Ar to O_2 flow ratio of 10). During the sputtering, the chamber pressure was maintained at 5 mTorr, and the rf power was 80 W. Two different types of TFT devices were prepared. One type of device was a typical single layered HIZO with different Hf contents (nominal thickness of 50 nm), and the other was a double-stacked HIZO active layer. In this case, the active layer consisted of double layers (active 1 (beneath the passivation layer) and active 2 (on the gate insulator)). The nominal thicknesses of active 1 and 2 were 40 nm and 10 nm, respectively. Finally, 200-nm-thick SiO_x was deposited as the passivation layer. Cross-sectional TEM was used to investigate the film uniformity and thicknesses (Hitachi 7600 operating at 300 kV). The channel length, the channel width, and the gate-to-S/D overlap length were 5, 25, and 10 μm, respectively.

Electrical characterization and measurement conditions: All of the electrical properties were measured using a Keithley 4200 semiconductor parameter analyzer. The transfer curves were measured at a drain bias of 10 V. The V_T was determined from the intercept of the plot of $(I_{DS})^{1/2}$ versus V_{GS}. The electrical stress was applied at a V_{GS} of −20 V and a V_{DS} of 10 V from 0 to 11000 s. The illumination was applied using a commercial LED backlight unit with a brightness of 3000 cd m^{-2}. All of the measurements were carried under ambient conditions at 60 °C.

Device simulation: A SILVACO ATLAS-2D device simulator was used for all of the device simulations.

Supporting Information

Supporting Information is available from the Wiley Online Library and from the author.

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