Effect of channel thickness on density of states in amorphous InGaZnO thin film transistor

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We report on the origin of threshold voltage shift with the thickness of amorphous InGaZnO channel layer deposited by rf magnetron sputter at room temperature, using density of states extracted from multi frequency method and falling rates of activation energy, which of trends are entirely consistent each other in respect of the reduction of total traps with increasing the channel thickness. Furthermore, we shows that the behavior of ΔV_{th} under the positive gate bias stress and thermal stress can be explained by charge trapping mechanism based on total trap variation. © *2011 American Institute of Physics*. [doi:10.1063/1.3570641]

Thin-film transistors (TFTs) using amorphous oxide semiconductors (AOSs) have attracted considerable attention in active matrix organic light emitting diode due to their large mobility of ~10 $cm^2 (V\ s)^{-1}$ and device fabrication even at room temperature.[1,2] Also, AOSs are representative candidates to replace the conventional amorphous silicon (a-Si), since they have high optical transparency, thermal and chemical stability.[3,4] In this respect, the stability of AOSs under the bias, thermal and illumination stress has been issued for the practical applications.[5,6] In particular, the investigation for finding the origin of threshold voltage (V_{th}) shift, ΔV_{th}, with the thickness of amorphous InGaZnO (a-IGZO) channel layer has not been reported until now. In additions, the mechanism of ΔV_{th} under various stresses is in controversy. A few possible origins, such as defects in AOSs,[7] carrier tunneling,[8] interactions with oxygen[9] and water[10] at back channel surface, charge trapping[11] in AOSs and at interface, have been investigated. Moreover, AOSs have tail states and subgap density of states (DOSs) originated from structure disorder and defects.[12] Therefore, the investigation of DOSs in a-IGZO has to be carried out in respect of the stability. DOSs in various channel layers have been extracted by the numerical simulation-based fitting,[13] the optical response method,[14] the Meyer–Neldel rule,[15] and multifrequency method (MFM).[16] Among them, MFM technique is very useful for AOSs TFTs, since it is a fast, simple, and accurate method for extracting DOSs without illumination, temperature, and numerical iteration.[16]

In this work, the origin of ΔV_{th} with channel thickness of a-IGZO TFT was investigated, using DOSs and falling rates in a-IGZO. In additions, it is suggested that ΔV_{th} under bias and thermal stress can be explained by charge trapping mechanism.

Mo as gate electrode on glass substrate was deposited by dc sputter, and a-IGZO channel layers were grown by rf magnetron sputter at room temperature on 200 nm thick SiN_x as gate insulator. The a-IGZO channel layer and source/drain were defined by the photolithography and wet etching. Ti and Au as source/drain were deposited by electron beam and thermal evaporation method, respectively. The channel length and width were 200 μm and 100 μm, respectively. All of a-IGZO TFTs were annealed at 350 °C for 1 h in N_2 ambient. All I-V and C-V measurements were carried out by semiconductor parameter analyzer (ETCP-1000) and LCR meter (HP 4284A), respectively. DOSs and falling rates were extracted from MFM technique and thermal stress test, respectively.

Figure 1 illustrates transfer characteristics of a-IGZO TFTs with different channel thickness. Their Electrical properties, such as V_{th}, field effect mobility (μ_{FE}), and on/off current ratio ($I_{on\text{-}off}$ ratio) were summarized in Table I. In particular, V_{th} value of a-IGZO TFTs shifted toward negative direction as the thickness of a-IGZO channel layer increases from 30 to 85 nm. To investigate the origin of the negative V_{th} shift with increasing the channel thickness with respect to bulk and interface trap, subgap DOSs were extracted from MFM technique using C-V characteristics.[16]

Figure 2 illustrates subgap DOSs with channel thickness extracted by MFM. Acceptorlike traps were distributed in the

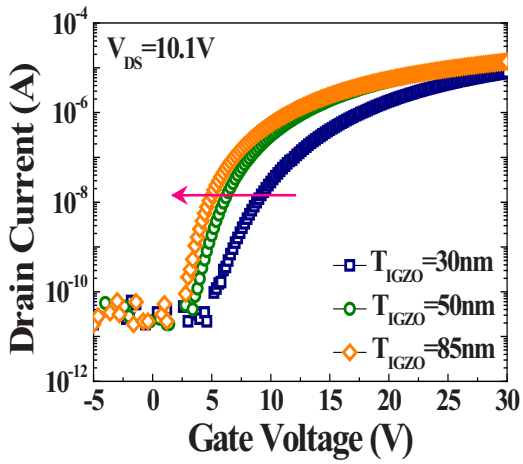

FIG. 1. (Color online) Transfer characteristics with the thickness of a-IGZO TFTs. The arrow indicates shift direction of V_{th} as the thickness of a-IGZO channel layer increases.

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TABLE I. Summarization of electrical properties of a-IGZO TFTs with 30 nm, 50 nm, and 85 nm channel thickness, respectively.

Channel thickness (nm)	V_{th} (V)	μ_{FE} (cm^2/V s)	Ion-off ratio	SS (V/decade)
30	9.1	4.8	1.91×10^7	1.22
50	3.7	6.4	3.54×10^7	0.82
85	1.9	6.4	3.34×10^7	0.65

half upper energy band gap of a-IGZO channel, since a-IGZO channel has n-type channel property. The inset in the Fig. 2 shows DOSs magnified between E_c and (E_c-0.4) eV. It is observed that DOSs in channel layer decrease as the thickness of a-IGZO increases. This result mean bulk and interface trap states are strongly dependent on the thickness of a-IGZO channel layer. Therefore, the origin of the negative V_{th} shift with the increase in the channel thickness can be explained using a-IGZO DOSs. Based on DOSs results, the a-IGZO TFT with 30 nm channel thickness has much more bulk traps and interface trap states than those of the thicker a-IGZO TFTs, indicating less carrier concentration which contributes to the channel conductivity. Consequently, V_{th} is located at more positive position than those of the thicker a-IGZO TFTs, since carriers are much less in number as the result of carrier capturing by much more traps in the case of 30 nm a-IGZO TFT. Therefore, it is believed that the reduction in total traps with increasing the a-IGZO thickness causes the negative shift in V_{th}.

Figure 3 shows V_{th} instability with the channel thickness under positive bias stress. The bias stress was applied at V_{GS}=20 V, drain to source current (V_{DS}) of 5.1 V for 2 h in air. Figure 3(d) illustrates the behavior of V_{th} with bias stress time. As a result, ΔV_{th} of a-IGZO TFT with 30 nm, 50 nm, and 85 nm channel thickness under positive bias stress were 2.5 V, 1.7 V, and 0.6 V, respectively. ΔV_{th} is reduced as the thickness of the channel layer increases. The amount of ΔV_{th} corresponds to the number of captured electrons, which are also proportional to the number of trap states. Therefore, the a-IGZO TFT with 85 nm channel thickness has much less ΔV_{th} than those of thinner a-IGZO TFTs. Based on DOSs results which showed the dependence on the channel thickness, we suggest that ΔV_{th} is originated from charge trapping

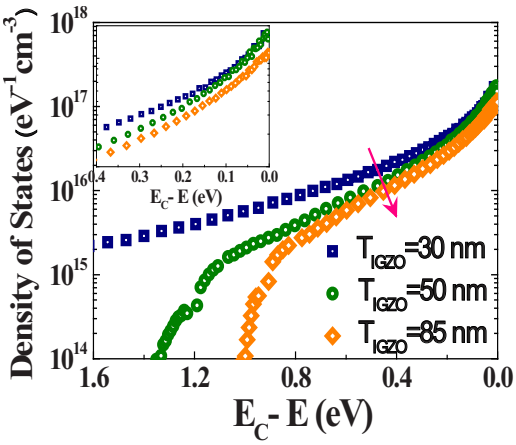

FIG. 2. (Color online) Subgap DOSs in the energy band gap of a-IGZO extracted from MFM technique. The arrow indicates DOSs distribution decreases as the thickness of a-IGZO channel layer increases. The inset shows DOSs with energy range from E_c to (E_c-0.4) eV.

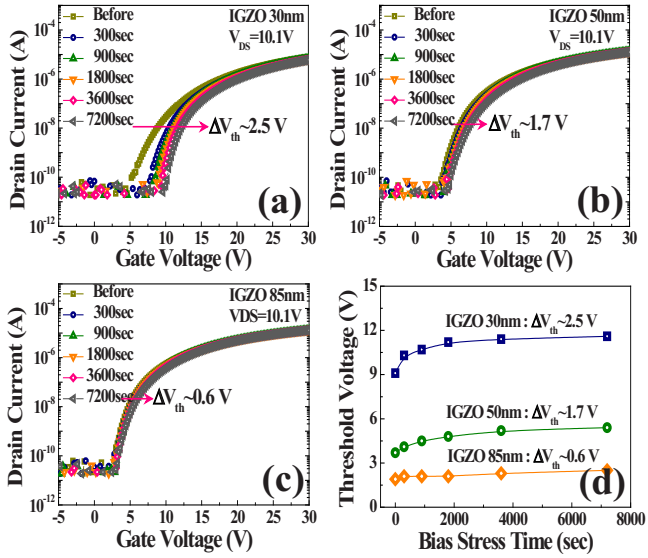

FIG. 3. (Color online) The evolutions of transfer curves with the channel thickness of a-IGZO TFTs under positive bias stress for 7200 s. (a) ΔV_{th} ~2.5 V for 30 nm a-IGZO TFT, (b) ΔV_{th} ~1.7 V for 50 nm a-IGZO TFT, (c) ΔV_{th} ~0.6 V for 85 nm a-IGZO TFT, respectively, and (d) the behavior for V_{th} shift with bias stress time for all of TFTs.

mechanism through bulk traps in a-IGZO channel and interface traps between the channel layer and the gate insulator since the reduction in ΔV_{th} with increasing the channel thickness is consistent with that in DOSs for all of a-IGZO TFTs. After the bias induced stress test for a-IGZO TFTs, a week later the recovery test for the TFTs was carried out to investigate instability by temperature induced stress. As a result, electrical properties, such as V_{th}, subthreshold swing (SS), and I_{on-off} ratio, were fully recovered, showing the same values with those for the TFTs before the bias stress. Therefore, transfer characteristics for a-IGZO TFTs with various channel thickness were matched well compared with those for the TFTs before the bias stress, indicating the robust electrical properties of a-IGZO TFTs regardless of the absence of any passivation layer.

Figure 4 shows the evolutions of ΔV_{th} with the channel thickness of a-IGZO TFTs under thermal stress from 298 to 353 K. The thermal stress was applied at vacuum of $<1.5\times10^{-2}$ Torr in dark state. As shown in Fig. 4, V_{th} shifted negatively with increasing the temperature for all of TFTs due to the generation of thermally activated carriers from traps in the band gap of a-IGZO. The I_{on-off} ratio decreased with increasing the temperature due to the noticeable increase in off-state current, whereas the SS value and the μ_{FE} were almost not changed. ΔV_{th} during thermal stress was 4.0 V for 30 nm a-IGZO TFT, 1.9 V for 50 nm a-IGZO TFT, and 1.0 V for 85 nm a-IGZO TFT, respectively. The reduction in ΔV_{th} value with increasing the channel thickness is consistent well with that when the bias is stressed. Figure 5 represents the activation energy with gate voltage for a-IGZO TFTs with different channel thickness in the subthreshold region. The drain current in the region is given as[17]

$$I_D \approx \alpha(V_G - V_{th})\exp\left[\frac{-E_A(V_G)}{kT}\right], \quad (1)$$

where E_A is activation energy, k the Boltzmann constant, and α does not depend on the temperature and the drain current. We plotted the logarithm of the $I_D/(V_G\text{-}V_{th})$ versus 1/kT.

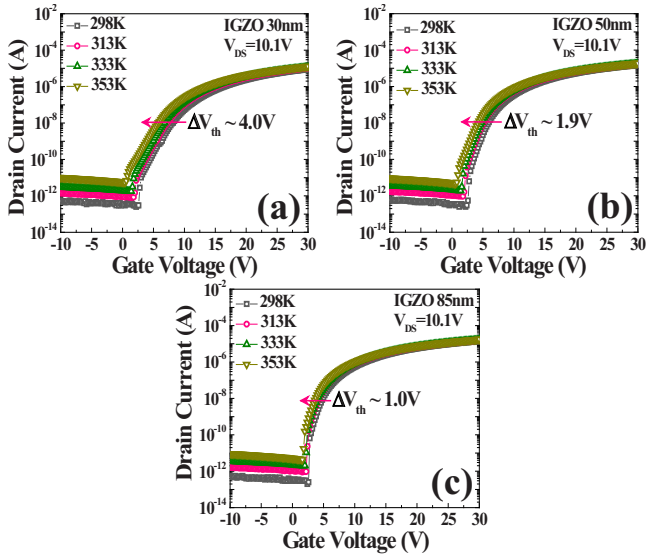

FIG. 4. (Color online) The evolutions of transfer characteristics with the channel thickness of a-IGZO TFTs under thermal stress from 298 K to 353 K. (a) $\Delta V_{th} \sim 4.0$ V for 30 nm a-IGZO TFT, (b) $\Delta V_{th} \sim 1.9$ V for 50 nm a-IGZO TFT, and (c) $\Delta V_{th} \sim 1.0$ V for 85 nm a-IGZO TFT, respectively.

From the results, we estimated the falling rates for all of TFTs. The values were 0.03 eV $(V)^{-1}$, 0.23 eV $(V)^{-1}$, and 0.93 eV $(V)^{-1}$ for 30 nm, 50 nm, and 85 nm a-IGZO TFTs, respectively. The faster falling rate means the reduction in bulk and interface trap density.[18] Therefore, total trap density decreases as the a-IGZO channel thickness increases, which is matched with the results of subgap DOSs. From results of subgap DOSs and falling rates, we found that the total trap density is reduced with increasing the channel thickness. Therefore, we suggest that ΔV_{th} with the channel thickness is originated from the variation in total trap density which affects the number of carrier concentration in a-IGZO. In a

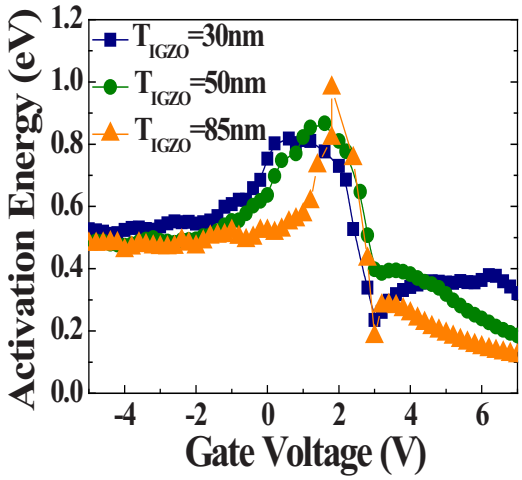

FIG. 5. (Color online) The activation energy with gate voltage for a-IGZO TFTs with various channel thickness.

physical respect based on this result, it is important to note that the reduction in total trap density of a-IGZO TFT with a thicker channel layer can be explained by the formation of more stable amorphous phase with less trap density in which the disorder is reduced. Thicker IGZO channel layer can have fewer defect states than that of thinner one. It is believed that defects in the channel during deposition process are annealed by the heat of argon plasma, which causes interface and bulk traps to be cured. Therefore, thinner IGZO with relatively short process time can have lager DOSs.

The origin of V_{th} shift with the channel thickness was experimentally provided and analyzed through the consistency of DOSs and falling rates of activation energy. It is suggested that ΔV_{th} with a-IGZO channel thickness is originated from the variation in carrier concentration, which can be changed in number by variation in the total trap density. Furthermore, it is confirmed that ΔV_{th} behavior under positive bias stress and thermal stress can be explained by the charge trapping mechanism, since the reduction in ΔV_{th} with increasing the channel thickness is consistent with the results of DOSs and falling rates.

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