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Single-Electron Transistors with Sidewall Depletion Gates on a Silicon-On-Insulator Nano-Wire

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Novel single-electron transistors with sidewall depletion gates on a silicon-on-insulator nano-wire have been fabricated by the conventional very large-scale integration technologies. The fabricated SETs show the controllable characteristics, which can be estimated from the device geometry. The electrically induced quantum dot is well defined in the intended spot and the fabricated SETs show reliable single-dot characteristics eliminating unintentionally formed potential barriers in a silicon-on-insulator nano-wire. Also, it shows multiple Coulomb oscillation peaks with a constant period, overcoming the drawbacks of the previously reported SETs based on electrically induced quantum dot. The Coulomb oscillation phase control and voltage gain larger than unity are the promising properties of our devices for practical circuit application. [DOI: 10.1143/JJAP.41.2574]

KEYWORDS: single-electron transistors, sidewall depletion gates, silicon-on-insulator, quantum dot, Coulomb oscillation, phase control, voltage gain

1. Introduction

Single-electron transistors (SETs) are promising candidates for future functional devices because of their high integration density and low power consumption. For an application of SETs as components of the integrated circuitry, there have been two fundamental issues. One is the fabrication method compatible with conventional very large-scale integration (VLSI) technologies. For a useful application of the SETs in near future, the SET-metal oxide semiconductor field effect transistor (MOSFET) hybrid circuit schemes have been proposed.[1,2] To integrate this SET-MOSFET hybrid circuits, it is strongly required that SETs should be fabricated by the conventional silicon VLSI technologies. The other issue is the controllable characteristics of SETs. In general, electronic devices should have designable geometric parameters and their fabrication methods should guarantee the reproducibility and controllability of the device geometry. Quantum dot fabrication by lithography is one of the designable and reproducible fabrication methods. From this point of view, a structure with an electrically induced quantum dot[3,4] has a promise for an optimization of the device characteristics.

In this paper, novel SETs with sidewall depletion gates on a silicon-on-insulator (SOI) wire are demonstrated, using the combination of conventional photolithography and process technologies. The uniform wire and sidewall depletion gates form an electrostatically well-defined quantum dot and eliminate the possibility of unintended quantum dot formation.[6]

2. Experimental

Figures 1 and 2 show the schematic diagram and cross-section of the fabricated device, respectively. Electron channel in the 45-nm-thick SOI wire is formed by the back gate bias (V_{BG}), and two tunnel junctions are formed by the poly-crystalline silicon (poly-Si) sidewall depletion gate bias (V_{SG}). The charge of electrically induced quantum dot is controlled by the poly-Si control gate bias (V_{CG}).

Starting material is the 60-nm-thick top layer of the 4 ×

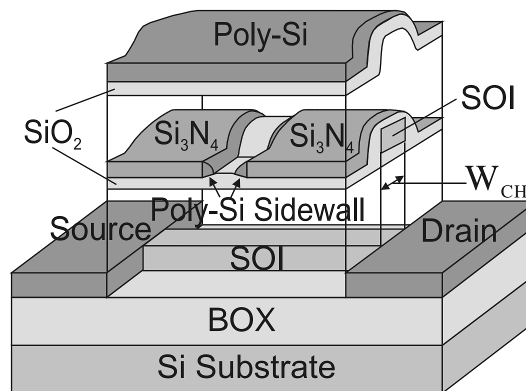

Fig. 1. Schematic diagram of the fabricated SET. Starting material was a 60 nm thick SOI film. The thickness and width of nanowire are 45 nm and 30 nm, respectivley.

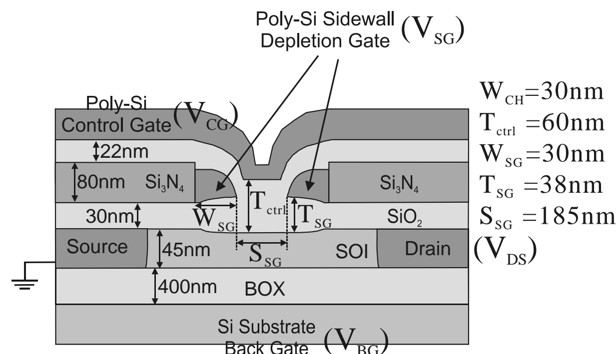

Fig. 2. Schematic cross-section of SETs with sidewall depletion gates on 30-nm-wide SOI nano-wire and its geometric parameters.

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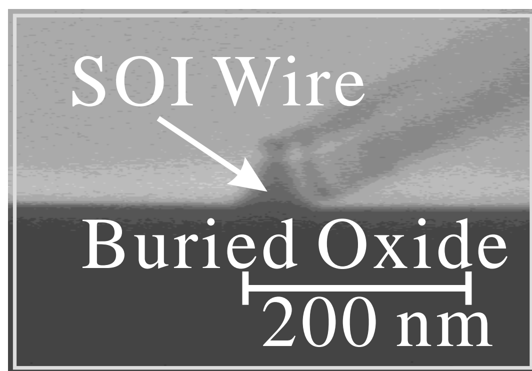
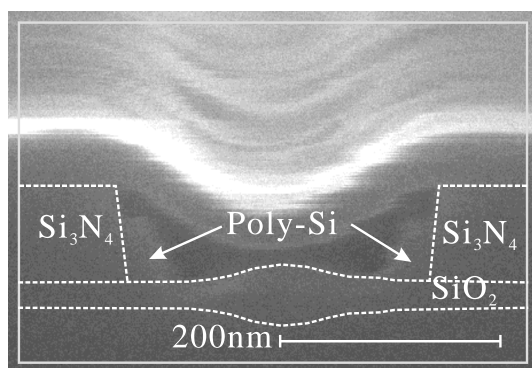


(a)



(b)

Fig. 3. SEM images of SOI wire and sidewall depletion gate (a) 30-nm-wide SOI wire (b) Poly-crystalline silicon sidewall depletion gate.

10^{15} cm^{-3} p-type SOI (100) wafer prepared by separation by implanted oxygen (SIMOX). The top silicon layer was separated from the silicon substrate by the 415-nm-thick buried oxide.

In the first stage, an SOI nano-wire is formed by the sidewall patterning technology using conventional photolithography, chemical vapor deposition (CVD) and anisotropic etching process.[5] Figure 3(a) shows scanning electron microscopy (SEM) images of 30-nm-wide SOI wire formed by the sidewall patterning technology. A good uniformity of 30-nm-wide SOI wire formed by this sidewall patterning technology effectively suppresses naturally formed tunnel junctions during the gate oxidation, in comparison with the nano-wire defined by electron-beam lithography.[6]

After the formation of the SOI wire, 30-nm-thick SiO_2 layer as the sidewall depletion gate oxide is deposited using a plasma enhanced chemical vapor deposition (PECVD) system. The 80-nm-thick Si_3N_4 layer was deposited on the sidewall depletion gate oxide, and then the groove pattern of the Si_3N_4 layer was lithographically defined. The gate oxide becomes thicker locally only under Si_3N_4 groove during the growth of 8-nm-thick SiO_2 by thermal oxidation. To form the poly-Si sidewall depletion gates, 40-nm-thick n-type highly doped poly-Si was deposited and anisotropically etched in Cl_2 reactive-ion plasma. Figure 3(b) shows the SEM images of sidewall depletion gate on the SOI nano-wire. The bias of the sidewall depletion gates electrically induces two tunnel barriers in the SOI wire. After the deposition of the control gate oxide, the poly-Si control gate was defined by the conventional photolithography. These processes are compatible with the conventional VLSI technologies.

3. Results and Discussions

3.1 Characteristics of intentional single-dot

As marked in Fig. 2, the geometric parameters of the fabricated device are: the width of SOI wire (W_{CH}), the thickness of control gate oxide (T_{ctrl}), the width of sidewall gate (W_{SG}), the thickness of the sidewall gate oxide (T_{SG}), and the separation between two sidewall gates (S_{SG}). The estimated control gate oxide capacitance (C_{CG}) from these geometric parameters is 3.2 aF, assuming an approximation of two parallel plate capacitance, since C_{CG} is the 60-nm-thick oxide capacitance with the planar area of $S_{SG} \times W_{CH}$. This C_{CG} corresponds to the Coulomb oscillation period (ΔV_{CG}) of 50 mV.

Figure 4 shows V_{CG} dependence of the drain current at 4.2 K. From Coulomb oscillation characteristics in Fig. 4, ΔV_{CG} is 68 mV and the extracted C_{CG} from this period is 2.35 aF. This value is smaller than the estimated C_{CG} from the device geometry. This difference results from the reduction of the effective area of silicon dot by the electric field effect and the increment of the effective thickness of the control gate oxide due to additional silicon capacitance. This silicon capacitance is reasonable in that the inversion layer is located at the bottom of the silicon channel by V_{BG}. This silicon capacitance is estimated to be 12.8 aF, since the silicon channel thickness is 45 nm and the area is the same one in case of C_{CG}. Incorporating this silicon capacitance into the additional component of C_{CG}, the effective control gate oxide capacitance is 2.56 aF, which is consistent with C_{CG} of 2.35 aF extracted from measured characteristics in Fig. 4.

Figure 4 also shows the clear multiple Coulomb oscillation peaks and the constant oscillation period as a function of V_{CG}. Considering that the switching characteristics of the previously reported SETs based on the electrically induced quantum dot have degraded sensitively as the gate bias increases and then only a few peaks were observed in the subthresh-

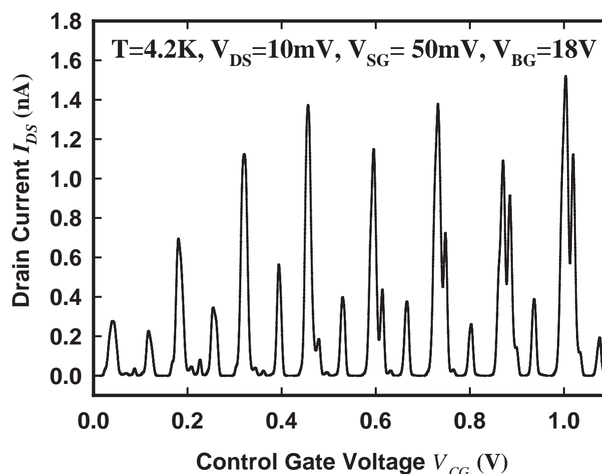


Fig. 4. Control gate voltage (V_{CG}) dependence of the drain current of the fabricated SET at 4.2 K. The oscillation period is 68 mV and the estimated C_{CG} is 2.35 aF.

old region,[3,4] the fabricated SETs are much improved and comparable to SETs based on the physically formed quantum dot.[7] These characteristics stem from 3-dimensional structure of the sidewall depletion gate wrapping SOI nano-wire. It is consistent with 3-dimensional device simulation result in Fig. 5. As shown in Fig. 5, the depletion width is nearly constant and the potential of the island is independently controlled by V_{CG}, as V_{CG} increases from 0.2 to 0.8 V.

Figure 6 shows the drain voltage (V_{DS}) dependence of drain current at 15 K. Nonlinear shape of drain current is clear, and Coulomb gap voltage at $V_{CG} = 20$ mV is about 40 mV. The magnitude and position of Coulomb gap are modulated by V_{CG} according to the orthodox theory of single-electron tunneling.

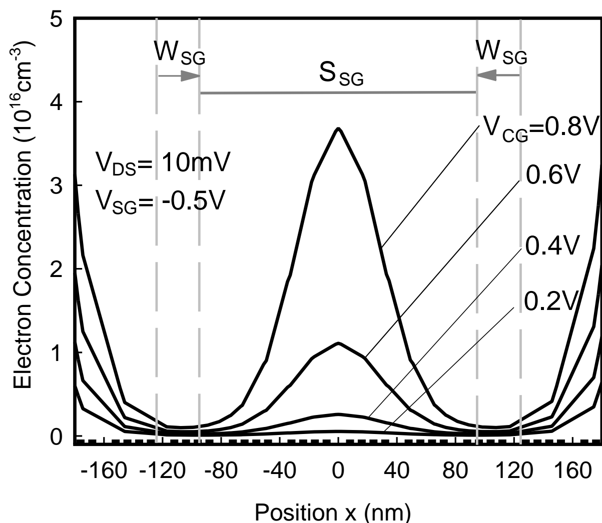


Fig. 5. Electron concentrations along the SOI nano-wire length direction at 5 nm depth beneath Si/SiO_2 interface. Poisson equation is solved by 3-dimensional device simulator DAVINCI. The geometric parameters for simulation are: $S_{SG} = 185$ nm, $W_{SG} = 30$ nm, $W_{CH} = 30$ nm, $T_{ctrl} = 60$ nm, $T_{SG} = 38$ nm, $L_{CH} = 2\,\mu$m.

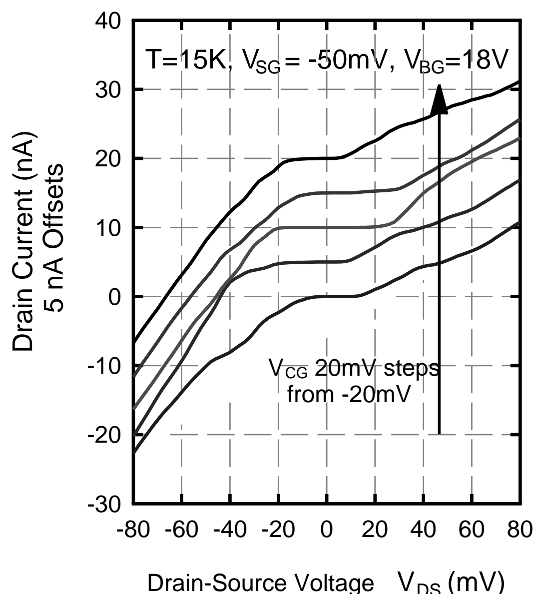


Fig. 6. Drain voltage (V_{DS}) dependence of the drain current of SET at 15 K. The drain current is shown with offset of 5 nA for clarity.

These results indicate that the electrically induced quantum dot is well defined at the intended spot on an SOI wire and the fabricated SET shows reliable single-dot characteristics as we have designed.

3.2 *Characteristics for logic circuit application*

Figure 7 shows that the phase of Coulomb oscillation is controlled by V_{SG}, while keeping its oscillation period constant. This oscillation phase control is an important feature for practical logic application. Most SET logic circuits are based on the oscillation phase control mechanism.[8,9] Our SETs' characteristics in Fig. 7 show that the shift of oscillation phase in the V_{CG} axis ($\Delta V_{CG,Shift}$) is 15 mV, when V_{SG} is increased by 50 mV step (ΔV_{SG}). This is due to the sharing of the island charge between the top control gate and sidewall depletion gates.

The sharing of the island charge can be formulated by the following simple equation.

$$\left(1 - \frac{C_{CG}}{C_T}\right) \times \Delta V_{CG,Shift} = \frac{2C_{SG}}{C_T} \times \Delta V_{SG} \qquad (1)$$

C_T: the total capacitance
C_{CG}: the control gate oxide capacitance
C_{SG}: the sidewall depletion gate oxide capacitance
$\Delta V_{CG,Shift}$: the shift of oscillation phase in the V_{CG} axis
ΔV_{SG}: the increment of V_{SG}

The simple calculation of eq. (1) makes it possible to extract the sidewall depletion gate oxide capacitance C_{SG}. Extracted capacitance C_{SG} is 0.88 aF, which is consistent with the estimated capacitance of 0.82 aF from device geometry with 38-nm-thick T_{SG} and the 2-dimensional area of $W_{SG} \times W_{CH}$. This result suggests that the peak position is controllable without additional electrodes and the electrical characteristics of our SETs can be easily optimized by T_{SG} i.e. device structure. These characteristics are very useful for the design of SET logic device. Moreover, as shown in Fig. 8, our SETs show the voltage gain of 1.3, which is given as the ratio C_{CG}/C_D at a constant current.

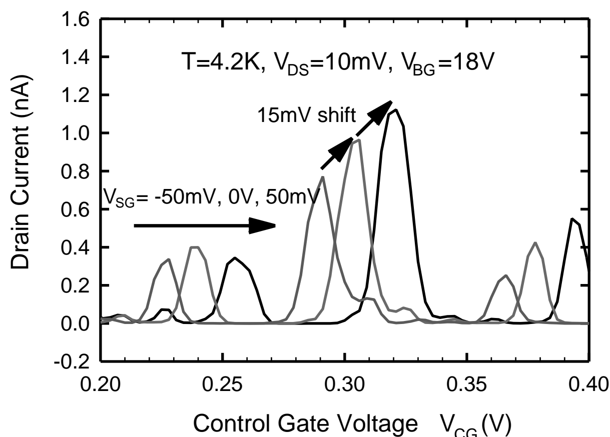


Fig. 7. Control gate voltage (V_{CG}) dependence of the drain current as a function of sidewall depletion gate voltage (V_{SG}) of the fabricated SET at 4.2 K. The Coulomb oscillation phases are modulated by $V_{SG} - 50$, 0, 50 mV, respectively.

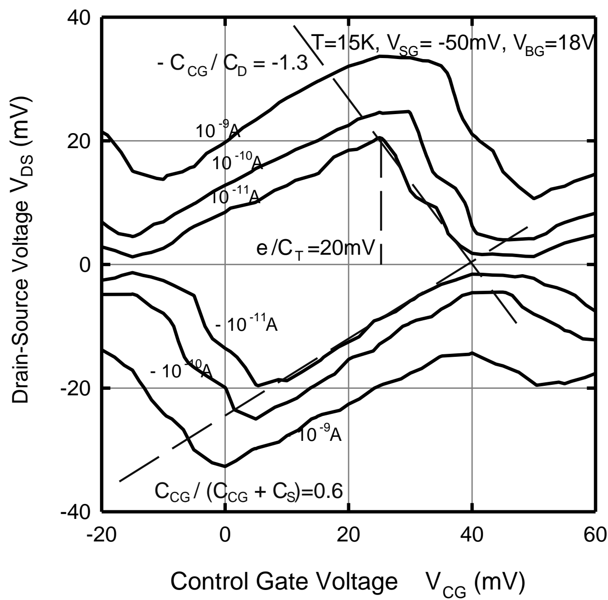


Fig. 8. Contour plots of the drain current as a function of control gate voltage (V_{CG}) and drain voltage (V_{DS}) at 15 K.

4. Conclusions

We have fabricated novel SETs with sidewall depletion gates on an SOI nano-wire using conventional silicon VLSI technologies. The fabricated SETs show reliable single-dot characteristics and the efficient suppression of unintentional potential barriers in the SOI nano-wire. The device parameters extracted from measured characteristics are consistent with the estimated values from device geometry. In addition, the multiple Coulomb oscillation peaks with a constant period indicate that our SETs overcome the drawbacks of the previously demonstrated SETs based on electrically induced quantum dot.

The Coulomb oscillation phase control without additional electrodes and voltage gain larger than unity are the promising properties of our devices for practical and reliable circuit application.

Acknowledgements

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