A Study on the Degradation of In–Ga–Zn–O Thin-Film Transistors Under Current Stress by Local Variations in Density of States and Trapped Charge Distribution

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***Abstract*— Thin-film transistors using In–Ga–Zn–O (IGZO) semiconductors were evaluated under current stress by applying positive voltages to the gate and drain electrodes. Initially, the transfer characteristics exhibit identical threshold voltages (V_T) when the source and drain electrodes are interchanged during measurement (forward and reverse V_{DS} sweep). However, as stress time increases, larger shifts in V_T are observed under forward V_{DS} sweep than under reverse V_{DS} sweep conditions. Subgap states analyses based on the photoresponse of capacitance–voltage (C–V) curves suggest that local annihilation of donor-like traps occurs near the drain electrode. Hump-like features are clearly observed in the C–V curves collected between the drain and gate electrodes, while they do not appear in the C–V data obtained between the source and the gate. Based on the above, a local charge trapping model is introduced in order to interpret the device degradation. In this model, the major carrier electrons are trapped more abundantly near the source electrode due to the presence of a Schottky junction between IGZO and the source/drain electrodes.**

***Index Terms*— Thin film transistor (TFT), In-Ga-Zn-O (IGZO), charge trapping, current stress, sub-gap states.**

I. Introduction

THIN film transistors (TFTs) incorporating amorphous oxide semiconductors such as In-Ga-Zn-O (IGZO) are currently evolving from niche to core technology in the flat panel display industry [1], [2]. The stability of oxide TFTs has been studied by numerous research groups under negative gate bias stress that is important for AMLCDs, and positive gate bias stress to simulate driving transistors in AMOLED backplanes. The shift in threshold voltage (V_T) during stress is usually interpreted in terms of charge trapping [3], defects related to oxygen vacancies [4], hot carriers or self-heating [5], [6]. However it is possible that more than one of the above phenomena may influence the device stability. The present work involves a quantitative analysis on the degradation of IGZO TFTs under positive bias stress. The distribution of sub-gap states is extracted before and after stress, based on the photoresponse of their capacitance-voltage (C-V) characteristics. The latter technique is referred to as monochromatic photonic C-V spectroscopy (MPCVS) [7], and a TCAD tool by Silvaco is used (ATLAS-2D) [8] to simulate the current-voltage (I-V) curves of the TFTs. Local charge trapping in the gate insulator near the source electrode, and a large decrease in donor-like states in the mid-gap level of the semiconductor near the drain depict well the degradation behavior of the device.

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II. Experimental Procedure

Bottom gate IGZO devices with a SiO_x etch stopper were fabricated on glass, using sputter deposited Mo as the gate and source-drain electrodes. A stack of 400 nm-thick SiN_x and 50 nm-thick SiO_x was grown by PECVD as the gate insulator, and a 50 nm-thick IGZO film was deposited by DC sputtering. A 100 nm-thick SiO_x passivation was grown by PECVD, and the transistors were annealed in air for 1 hour at 350 °C.

For the positive bias stress, the gate voltage (V_{GS}) was fixed at 20 V and the drain voltage (V_{DS}) at 10 V. To read out the I-V properties, the drain voltages (V_{DS}) was set at 10 V. Devices with channel width/length=W_{ch}/L_{ch} = 50/15 μm and gate-to-source/drain overlap length L_{OV} = 13 μm were characterized using an Agilent 4156C precision parameter analyzer in air ambient. Here, $I_{DS,F}$ is the current measured under forward V_{DS} sweep (the drain and source configuration is identical to that during current stress), and $I_{DS,R}$ is the current measured under reverse V_{DS} sweep (the drain and source settings are interchanged with respect to the current stress conditions). The C-V data were collected using a HP 4294A precision LCR meter, at a frequency of 50 kHz. The density of sub-gap states, g(E), was extracted from C-V characteristics measured both in the dark and under illumination with a monochromatic light of 532 nm wavelength.

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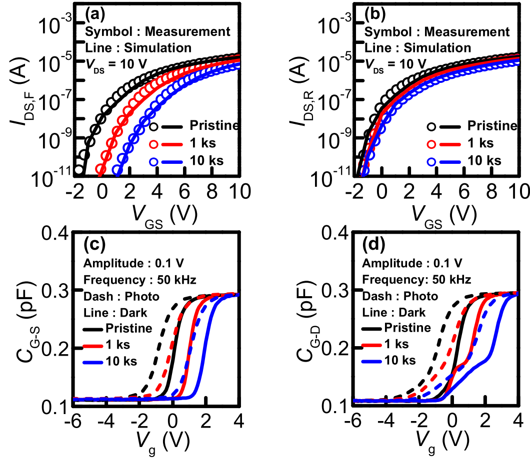

Fig. 1. Transfer characteristics of the IGZO TFT device under (a) forward and (b) reverse V_{DS} sweep conditions. C-V curves between (c) the gate-source and (d) the gate-drain electrodes.

The TCAD simulation of the sub-gap trap distributions was done using the following equations:

$$g_D(E) = N_{TD} \times \exp\left(\frac{E_V - E}{kT_{TD}}\right) + N_{GD} \times \exp\left(-\left(\frac{(E_V - E) + E_{GD}}{kT_{GD}}\right)^2\right) \quad (1)$$

$$g_A(E) = N_{TA} \times \exp\left(\frac{E - E_C}{kT_{TA}}\right) + N_{DA} \times \exp\left(\frac{E - E_C}{kT_{DA}}\right) + N_{GA} \times \exp\left(-\left(\frac{(E - E_C) + E_{GA}}{kT_{GA}}\right)^2\right) \quad (2)$$

where $g_D(E)$ denotes the distribution of donor-like traps and $g_A(E)$ the distribution of acceptor-like traps.

III. Results and Discussions

The open symbols in Fig. 1(a) and (b) consist of the measured values of $I_{DS,F}$ and $I_{DS,R}$ respectively. Here, V_T is defined as the gate voltage that induces a drain current of 10 nA. The V_T values under forward V_{DS} sweep shift in the positive direction with increasing stress time (t_{str}). On the other hand, they remain relatively constant before and after stress under reverse V_{DS} sweep. This implies that the local V_T values near the source and drain electrodes evolve differently during stress.

The C-V data measured between the gate and source ($C_{G\text{-}S}$) and between the gate and drain ($C_{G\text{-}D}$) electrodes are shown in Fig. 1(c) and (d) respectively. The C-V curves also shift towards positive V_G values, however hump-like features appear and become more pronounced as t_{str} increases in the C_{G-D} measurements. The sub-gap state distributions before and after stress were extracted by using the photoresponse of the measured C-V curves (Fig. 1(c) and (d)) and MPCVS, of which the detailed procedure is explained in a former publication [7].

The extracted values of trap densities (N_{TD} = 4×10^{19} [$cm^{-3}eV^{-1}$], kT_{TD} = 0.35 [eV], N_{TA} = 5×10^{18} [$cm^{-3}eV^{-1}$], and kT_{TA} = 0.007 [eV] for the pristine device in Fig. 2(b)) are within the range of the values reported in the literature [9]–[11]. The broad Gaussian acceptor-like trap peak that is visible in Fig. 2(a) and (b) is determined by the N_{GA} term in (2), and may be associated with oxygen interstitials [12] or excess oxygen [11]. The mid-gap $g_D(E)$ undergoes a large decrease ($N_{TD} = 3\times10^{19}$ and 2×10^{18} at t_{str} = 1 ks and 10 ks in Fig. 2(b)) followed by a small increase in the acceptor-like tail trap density ($N_{GA} = 2 \times 10^{16}$ and 4×10^{16} at t_{str} = 0 and t_{str} = 1 ks in Fig. 2(b)). This suggests that the mid-gap donor-like traps related to ionized oxygen vacancy defects (i.e. V_O^0, V_O^+, and V_O^{2+} [4], [13]) may recombine during bias stress with the free electron carriers and a fraction of them is redistributed as shallow acceptor-like traps below E_C. Such an increase in shallow defects is consistent with the creation of cation interstitials [14], oxygen interstitials [12], or the formation of excess oxygen [11]. The net decrease in donor-like states is suggested to result in decreased current levels and positive V_T shifts. It is also worthy of note that the donor-like trap sub-peak near $E_C-0.3$ eV, which is likely to originate from ionized oxygen vacancy V_O^{2+} [13], [15], becomes more apparent during bias stress as shown in Fig. 2(b). This suggests that the V_O^{2+} defects may have a relatively higher energy barrier for the recombination with electrons than those of the other oxygen vacancy defects (V_O^0 or V_O^+).

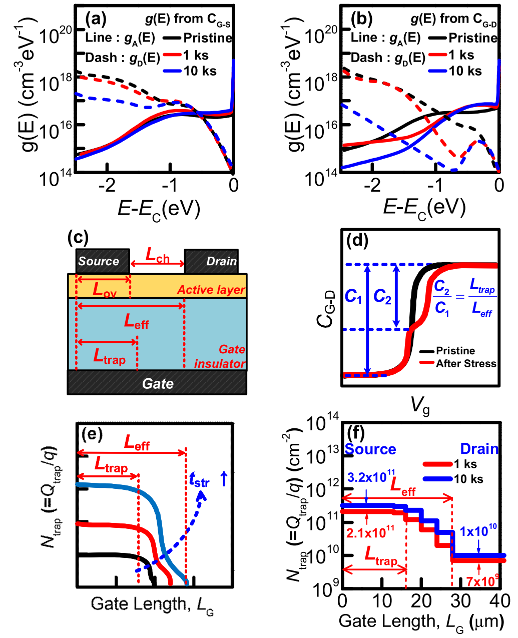

Fig. 2. Extracted DOS distributions in the IGZO semiconductor bandgap near the (a) source and (b) drain electrodes before and after stress. (c) Schematic cross sectional diagram of the device indicating L_{eff}, L_{OV}, and L_{trap}. (d) Schematic illustrating the distribution of C-V curves before and after stress. (e) Schematic illustrating the distribution of trapped electrons with respect to tstr, and (f) the profile of the trapped charge used for the simulation.

The humps observed in the C_{G-D} data of Fig. 1(d) are indicative of a more rapid increase in local V_T over current stress near the source electrode as compared with the drain region. In order to interpret this phenomenon, a local charge trapping model is suggested as follows. A Schottky barrier is formed between the source-drain electrodes and

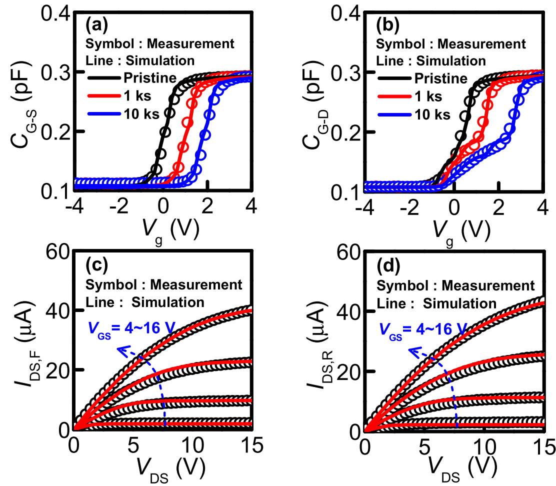

Fig. 3. Experimental and simulated C-V curves between (a) the gate-source and (b) the gate-drain electrodes. Experimental and simulated output (I_{DS} vs. V_{DS}) curves under (c) forward and (d) reverse V_{DS} sweep.

the IGZO semiconductor. Consequently, high energy electrons are present near the source region under positive bias stress conditions (V_{GS} = 20 V, V_{DS} = 10 V). Once a high vertical field is induced by V_{GS}, it would attract the high energy electrons towards the gate insulator near the source region, thereby stimulating local charge trapping into the gate insulator. If a distribution of charge per unit area trapped in the gate insulator is defined as Q_{trap}, the spatial distribution of Q_{trap} can be profiled by using the relationship $C_2/C_1 = L_{trap}/L_{eff}$ as shown in Fig. 2(c) and (d), where L_{eff} and L_{trap} denote respectively the effective channel length being modulated during the C-V measurement and the length over which Q_{trap} is distributed. L_{trap} was extracted to be 16 μm, starting with $L_{eff} = L_{OV}+L_{ch} = 28$ μm in the initial design of the device, and the C-V measurements providing $C_1 = 0.297$ pF and $C_2 = 0.17$ pF. Note that the concept of L_{eff} is valid only for the C-V evaluation, whereas for the I-V measurement the channel length would simply be equal to L_{ch}. As illustrated in Fig. 2(e), the actual concentration of electrons trapped in the gate insulator would decrease gradually from the source towards the drain region. Fig. 2(f) is the distribution of locally trapped electrons that was incorporated into the TCAD simulation.

The g(E) and Q_{trap} data from Fig. 2(a), (b) and (f) were used to perform the simulations, which are shown as solid lines in Fig. 1(a)~(b), and Fig. 3(a)~(d). The simulated C_{G-S} and C_{G-D} curves reproduce well the experimental results (Fig. 3(a) and (b)). Also, the output and transfer characteristics simulated under both forward and reverse V_{DS} sweep conditions match with the measurement results (Fig. 1(a)~(b), and Fig. 3(c)~(d)). Therefore, it is necessary to include both the variation in g(E) and the locally trapped electrons in order to exactly reproduce the effects of bias stress in the I-V characteristics, including $I_{DS,R}$ and C_{G-D}.

IV. Conclusion

In this letter, the degradation of IGZO TFTs under positive bias stress was studied based on I-V and C-V measurements. The local V_T near the source electrode increased and the net density of donor-like states decreased with stress time. While the former is due to a Schottky junction-related local electron trapping near the source electrode, the latter is anticipated to occur by the annihilation of unstable oxygen vacancy-related defects (V_O^+ or V_O^0) recombining with free electron carriers and the partial transition into shallow acceptor-like traps. The trapped charge density, Q_{trap}, was successfully profiled from hump-like features in the C_{G-D} curves. Subsequent TCAD simulations that include both the variation in g(E) and the Q_{trap} distribution reproduced well the experimental results before and after bias stress. Our results indicate that the degradation mechanism of TFT devices under current stress is quite complex. Analytical studies must therefore be carried out by thoroughly examining the variations in sub-gap states and the local distribution of trapped charge in order to understand the physical phenomena occurring in operating AMOLED driving transistors. The methodology presented in this letter will provide valuable insight on the optimal design of stable IGZO TFTs for AMOLED-oriented flat panel displays.

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