Bias-Dependent Effective Channel Length for Extraction of Subgap DOS by Capacitance–Voltage Characteristics in Amorphous Semiconductor TFTs

Hyunjun Choi, Jungmin Lee, Hagyoul Bae, Sung-Jin Choi, Dae Hwan Kim, *Member, IEEE*, and Dong Myong Kim, *Member, IEEE*

***Abstract*— Bias-dependent effective channel length [$L_{\text{eff}}(V_G)$] is empirically modeled with a channel conduction factor [$\alpha(V_G)$] for a consistent capacitance–voltage (C–V) characterization of the intrinsic subgap density of states (DOS) over the bandgap with the sub-bandgap photoresponsive C–V technique in amorphous thin-film transistors. We define the effective channel length $L_{\text{eff}}(V_G)$ through the product of the empirical channel conduction factor [$\alpha(V_G)$] and the metallurgical channel length (L_m). We confirm that the gate bias-dependent channel conduction effect is significant in the subgap DOS far from the conduction band edge (E_C) due to the low conductivity of the channel under subthreshold bias.**

***Index Terms*— Amorphous, channel conduction factor, effective channel length, gate bias-dependent, InGaZnO, subgap density of states (DOS), thin-film transistor (TFT).**

I. Introduction

AMORPHOUS oxide semiconductor (AOS) thin-film transistors (TFTs) are under active research and development for flexible and/or transparent displays with good uniformity, high productivity, low-cost manufacturing process, and enhanced carrier mobility [1], [2]. For consistent characterization and modeling of AOS TFTs, extraction of the subgap density of states (DOS) over the bandgap ($E_V < E < E_C$) is very important for electrical properties and long-term instability under various stress conditions [3]–[7]. In extracting the subgap DOS [the donor-like DOS $g_D(E)$ and the acceptor-like DOS $g_A(E)$] per unit volume through the capacitance–voltage (C–V) measurement, it is necessary to normalize the result by the effective volume considering the metallurgical channel length (L_m), the width (W), and the active layer thickness (T_{IGZO}) regardless of the gate voltage [5], [8].

In previous works, the DOS result per unit volume from the C–V characterization was simply normalized by the volume $\upsilon = L_m \cdot T_{\text{IGZO}} \cdot W$ all over the gate bias (V_G) conditions whatever the active region is partially conductive ($V_{\text{OFF}} < V_G < V_T$), or fully depleted ($V_G < V_{\text{OFF}}$), or highly conductive ($V_G > V_T$) by the gate bias (V_{OFF} as the cutoff voltage and V_T as the threshold voltage). However, the normalization should be performed by the V_G-dependent effective volume (υ_{eff}) considering the conductivity of the active region connected to the source and the drain contacts during the C–V characterization. Moreover, a normalization to L_m was performed without considering the gate-to-source/drain ($C_{G\text{–SD}}$) overlap length (L_{ov}) (assuming $L_{\text{ov},S} = L_{\text{ov},D} = L_{\text{ov}}$) during the extraction of the subgap DOS. These approaches cause inaccuracy in the subgap DOS and result in inconsistent characterization and modeling of TFTs.

In this brief, we propose a channel conduction factor [CCF: $\alpha(V_G)$] for the empirical modeling of the effective channel length [$L_{\text{eff}}(V_G)$] and report a C–V-based characterization of the intrinsic subgap DOS combined with the photoresponsive C–V technique under the sub-bandgap ($E_{\text{ph}} < E_g$) optical excitation [5]. In the characterization, in addition to the channel conduction factor and $L_{\text{eff}}(V_G)$, we also deembedded capacitances for the overlap of the source ($L_{\text{ov},S}$) and drain ($L_{\text{ov},D}$) with the gate.

II. Experimental C–V Characteristics and V_G-dependent Channel Conduction Factor Model

Experimental C–V curves, normalized by the maximum value ($C_{\max}$) of the total capacitance, are comparatively shown in Fig. 1 for the gate-to-source ($C_{G\text{–}S}$), the gate-to-drain ($C_{G\text{–}D}$), and the $C_{G\text{–SD}}$ measurement configurations of a-IGZO TFTs with a cross-sectional view as an inset.

$C_{G\text{–}S}$ is the measured capacitance between the gate and the source with the drain floated, and $C_{G\text{–}D}$ is the measured capacitance between the gate and the drain with the source floated. In the measurement of $C_{G\text{–SD}}$, the source and the drain

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H. Choi, J. Lee, S.-J. Choi, D. H. Kim, and D. M. Kim are with the School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea (e-mail: dmkim@kookmin.ac.kr).

H. Bae was with the School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea. He is now with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea.

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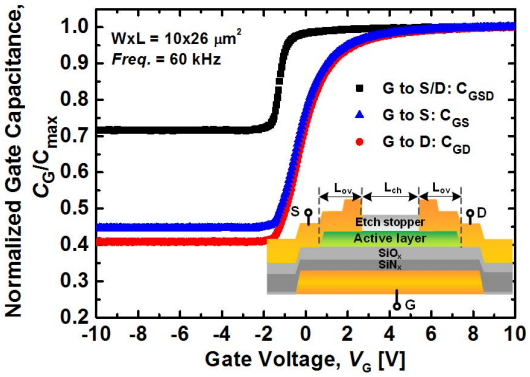

Fig. 1. Experimental C–V characteristics of a-IGZO TFTs for three different measurement configurations with C_{G-S} for the gate-to-source, C_{G-D} for the gate-to-drain, and $C_{G-\mathrm{SD}}$ for the gate-to-source/drain in common. Inset: cross-sectional view.

terminals are connected in common, and the capacitance is measured between the gate and the S/D in common.

As experimentally observed in Fig. 1, the minimum ($C_{\min}$) of the total capacitance under $V_G (\ll V_{\mathrm{OFF}})$ strongly depends on the configuration ($C_{G-S}|_{\min} \neq C_{G-D}|_{\min} \neq C_{G-\mathrm{SD}}|_{\min}$). This is because the active region is fully depleted and completely isolated from the S/D contacts for the G–S/D C–V characterization. It can be equivalently modeled as overlap capacitances ($C_{\mathrm{ov},S} + C_{\mathrm{ov},D} = C_{\mathrm{ov}}$ [F]) for S/D contacts, as shown Fig. 2(a). There are two parallel capacitance components in the substrate capacitance ($C_S = C_{\mathrm{Sd}} + C_{\mathrm{Sm}}$) in a series with the oxide capacitance (C_{ox}): 1) the depletion capacitance (C_{Sd}) for the depletion/space charge (Q_{SD}) modulation and 2) the diffusion capacitance (C_{Sm}) for the mobile charge (Q_{Sm}) modulation by the gate bias as

$$C_S(V_G) = C_{\mathrm{Sd}}(V_G) + C_{\mathrm{Sm}}(V_G) \tag{1}$$

$$C_{\mathrm{Sd}}(V_G) \equiv \left| \frac{dQ_{\mathrm{Sd}}(V_G)}{dV_G} \right| \tag{2}$$

$$Q_{\mathrm{Sd}}(V_G) \equiv A \int_0^{X_{\mathrm{dep}}(V_G)} q\left(N_d^+(x) - N_a^-(x)\right) dx \tag{3}$$

$$C_{\mathrm{Sm}}(V_G) \equiv \left| \frac{dQ_{\mathrm{Sm}}(V_G)}{dV_G} \right| \tag{4}$$

$$Q_{\mathrm{Sm}}(V_G) \equiv A \int_0^{X_{\mathrm{dep}}(V_G)} q\left(p(x) - n(x)\right) dx. \tag{5}$$

For an n-type substrate, the substrate capacitance $C_{S,\mathrm{dep}}$ in the depletion bias ($V_{T,\mathrm{inv}} < V_G < V_{\mathrm{FB}}$ or $2\phi_F < \psi_S < 0$; $C_{\mathrm{Sm}} \sim 0$) with ψ_S as the V_G-dependent surface potential and $\phi_F = -V_{\mathrm{th}} \cdot \ln(N_D/n_i)$ as Fermi potential is

$$C_{S,\mathrm{dep}}(V_G) \cong C_{\mathrm{Sd}}(V_G) = \frac{d\,|Q_{\mathrm{Sd}}(V_G)|}{dV_G} = \frac{\varepsilon_s A}{X_{\mathrm{dep}}(V_G)} \tag{6}$$

$$X_{\mathrm{dep}}(V_G) = \sqrt{\frac{2\varepsilon_s}{qN_D}\psi_S(V_G)} : \text{depletion width} \tag{7}$$

while the substrate capacitance $C_{S,\mathrm{acc}}$ in the strong accumulation bias ($V_{\mathrm{FB}} < V_{T,\mathrm{acc}} < V_G$ or $0 < 8V_{\mathrm{th}} < \psi_S$; $C_{\mathrm{Sd}} \ll C_{\mathrm{Sm}}$)

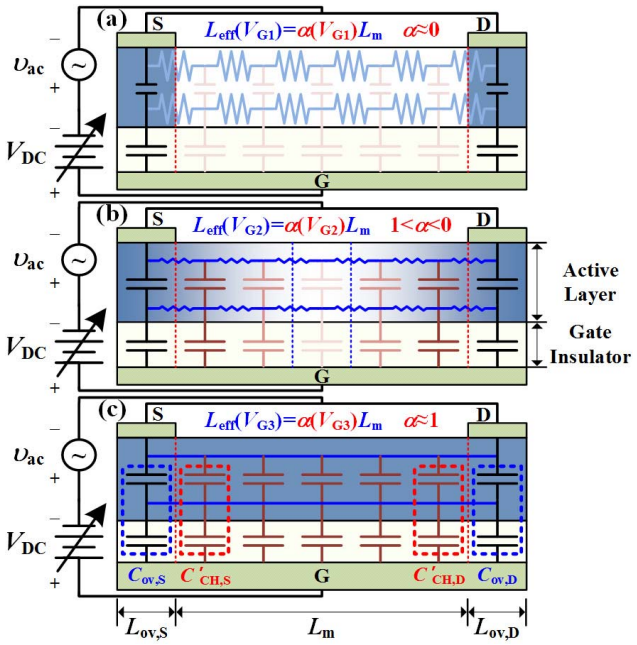

Fig. 2. Schematic with the distributed model with resistances and capacitances considering the channel conductivity of a-IGZO TFTs. (a) Cutoff state ($V_G \ll V_{\mathrm{OFF}}$). (b) Transition state ($V_{\mathrm{OFF}} < V_G < V_T$). (c) Turn-ON state ($V_G \gg V_T$). $C'_{\mathrm{CH},S}$ and $C'_{\mathrm{CH},D}$: localized channel capacitance per unit area [F/cm^{-2}] from the S/D electrode.

can be described as

$$C_{S,\mathrm{acc}}(V_G) = C_{\mathrm{Sd}}(V_G) + C_{\mathrm{Sm}}(V_G) \cong C_{\mathrm{Sm}}(V_G) \tag{8}$$

$$C_{\mathrm{Sd}}(V_G) = \frac{\varepsilon_s A}{X_{\mathrm{dep}}(V_G)} \left(\propto \frac{1}{\sqrt{\psi_S(V_G)}} \right) \quad (\ll C_{\mathrm{Sm}}(V_G) \propto \exp(\psi_S(V_G)/2V_{\mathrm{th}})) \tag{9}$$

$$Q_{\mathrm{mob}}(V_G) \cong -qA \int_0^{X_{\mathrm{ch}}(V_G)} n(x) dx. \tag{10}$$

We also note that the substrate capacitance $C_{S,\mathrm{inv}}$ in the strong inversion bias ($V_G < V_{T,\mathrm{inv}} \ll V_{\mathrm{FB}}$ or $\psi_S < 2\phi_F < 0$; $C_{\mathrm{Sd}} \ll C_{\mathrm{Sm}}$) for an n-type substrate, if properly implemented in a-IGZO TFTs, is

$$C_{S,\mathrm{inv}}(V_G) = C_{\mathrm{Sd}}(V_G) + C_{\mathrm{Sm}}(V_G) \cong C_{\mathrm{Sm}}(V_G) \tag{11}$$

$$Q_{\mathrm{mob}}(V_G) \cong +qA \int_0^{X_{\mathrm{dep}}(V_G)} p(x) dx. \tag{12}$$

In Fig. 2(c), it is a capacitance model for the strong accumulation state with a high diffusion capacitance [$C_S = C_{\mathrm{SD}} + C_{\mathrm{Sm}} \sim C_{\mathrm{Sm}} \gg C_{\mathrm{ox}}$ and $C_G = (C_S C_{\mathrm{ox}}/(C_S + C_{\mathrm{ox}})$]. Therefore, it is the correct capacitance model for the accumulation mode of the gate bias. When the drain bias is applied, this accumulated carriers form a high conductivity channel and result in a large drain current.

Therefore, the active region does not contribute to the total capacitance under the cutoff state with $V_G \ll V_{\mathrm{OFF}}$. On the other hand, $C_{\max}$ is independent of the configurations for the C–V measurement resulting $C_{G-S}|_{\max} = C_{G-D}|_{\max} = C_{G-\mathrm{SD}}|_{\max} = C_{\max}$. This is because, under strong accumulation with $V_G \gg V_T$, all of the active region from the source to the drain is highly conductive and fully contribute to the total capacitance, regardless of the

measurement configurations. It can be electrically modeled, as shown in Fig. 2(c).

In the case of $V_{OFF} < V_G < V_T$, the active region is in a limited conductivity. It can be described by the distributed resistances and capacitances, as shown in Fig. 2(b). Therefore, the total capacitance obtained from the C–V measurement is dominated by the capacitances close to S/D contacts. The increasing channel conductivity with the gate bias can be empirically mapped to the contribution of the localized channel capacitance (C_{CH} [F]) in the active region to the total capacitance with $\alpha(V_G)$. We assume that $C_{CH}(V_G)$ is a sum of the contribution from the source and the drain sides [$C'_{CH,S}(V_G)$ and $C'_{CH,D}(V_G)$]. Assuming a symmetric structure of the source and the drain contact to the active region, the contribution to each side is counted to be $L_{eff}(V_G)/2$. With increasing the gate bias to the threshold voltage, the contribution of the capacitance for the active region far from the S/D contact increases, finally reaching C_{max} at $V_G \gg V_T$ regardless of the G–S, G–D, and G–SD measurement configurations.

Under $V_{OFF} < V_G < V_T$, which is the main bias condition for the C–V characterization, therefore, $\alpha(V_G)$ and $L_{eff}(V_G)$ are obtained empirically modeled as

$$\alpha(V_G) = \left(\frac{C_G(V_G) - C_{ov}}{C_{ox} W L_m - C_{ov}}\right) = \left(\frac{C_{CH}(V_G)}{C_{ox} W L_m - C_{ov}}\right) \quad (13)$$

$$L_{eff}(V_G) = \alpha(V_G) \times L_m \quad (14)$$

with C_{ox} [F/cm^2] as the oxide capacitance. The effective volume (v_{eff}) for the subgap DOS can also be modeled as $v_{eff} = \alpha(V_G) \cdot v = \alpha(V_G) \cdot L_m \cdot T_{IGZO} \cdot W$. We note that the effective channel length $L_{eff}(V_G)$ in this brief is related to the gate bias (V_G)-dependent effective channel length during the C–V characterization, which is different from the drain bias (V_{DS})-dependent effective channel length in the I–V characteristics under the saturation mode of operation with the gate bias V_{GS} is greater than the threshold voltage. The channel length modulation by V_{DS} is severe in short channel TFTs under above-threshold ($V_{GS} > V_T$) condition, while the gate bias-dependent effective channel length modulation is predominant under the depletion or cutoff state with $V_G < V_T$.

By applying the empirical CCF model in (1) to the experimentally obtained C–V data for $C_{G\text{–}SD}$ in a-IGZO TFTs, we finally obtain $\alpha(V_G)$ over the gate voltage from the cutoff state through the depletion state to the above-threshold ON state, as shown in Fig. 3. Therefore, the effective intrinsic length [$L_{DOS}(V_G)$] of the active region for the C–V-based extraction of the intrinsic subgap DOS is described by

$$L_{DOS}(V_G) = L_{eff}(V_G) + 2L_{ov}. \quad (15)$$

The electrical C–V and I–V characterization techniques only allow the V_G-dependent net-charge response $Q_{sub}(V_G)$ from the net subgap charge density $\rho_{sub}(V_G)$ [$= \rho_{sub,d}(V_G) + \rho_{sub,a}(V_G)$] from the subgap states. The total subgap states $g(E)$ [$= g_D(E) + g_A(E)$] are composed of the donor-like states [$g_D(E)$] and the acceptor-like states $g_D(E)$ over the subgap energy level ($E_V < E < E_C$). The donor-like subgap states [$g_D(E)$] are neutral in the charge density if they are filled with electrons while positively charged ($+q$) if empty.

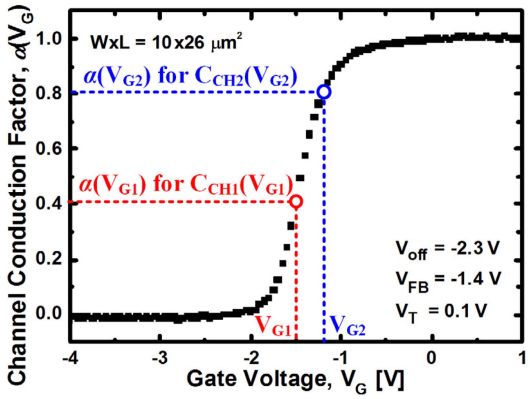

Fig. 3. Channel conduction factor $\alpha(V_G)$ as a function of the gate voltage. It is ~0 at $V_G \ll V_{FB}$ and ~1 at $V_G \gg V_T$ for an a-IGZO TFT with $W = 10$ μm, $L = 26$ μm, $T_{IGZO} = 30$ nm, and $T_{GI} = 200$ nm.

The acceptor-like subgap states [$g_A(E)$], on the other hand, are negatively charged ($-q$) if filled with electrons while neutral if empty.

In practical, a-IGZO TFTs with a thin active channel layer (T_{IGZO}), the subgap charge density $\rho_{sub}(V_G)$, and the V_G-dependent net-charge response $Q_{sub}(V_G)$ are described as the following equations:

$$\rho_{sub}(V_G)[C/cm^3] = \rho_{sub,D}(V_G) + \rho_{sub,A}(V_G) \quad (16)$$

$$\rho_{sub,D}(V_G) = +q \int_{E_F(V_G)}^{E_C} g_D(E) dE \quad (17)$$

$$\rho_{sub,A}(V_G) = -q \int_{E_V}^{E_F(V_G)} g_A(E) dE \quad (18)$$

$$Q_{sub}(V_G) \equiv \int_{x=0}^{T_{IGZO}} \rho_{sub}(V_G, x) dx \cong \rho_{sub}(V_G) T_{IGZO}. \quad (19)$$

If the quasi-Fermi level (E_F) under the applied gate bias gets closer to the conduction band edge (E_C), whatever they are either donor-like states or acceptor-like states, the net-charge contribution from the subgap states becomes more negatively charged, because the positively charged empty subgap states decrease while the number of the neutral subgap states filled with electrons increases. When E_F gets closer to the valence band edge (E_V), on the other hand, the subgap states are more positively charged, because the negatively charged subgap states filled with electrons decrease while the empty neutral subgap states are increase. We note that the subgap states can be either donor-like states or acceptor-like states strongly depending on the fabrication process, including composition ratio, gas flow rate, substrate temperature, chamber pressure, and so on. In n-channel a-IGZO TFTs, the subgap states close to E_C are usually known to be acceptor-like states, and the subgap states close to E_V are acceptor-like states.

We note that the operation mode is divided at the flat band condition. The surface potential and resulting the bending of the energy band can be easily modulated by the gate bias under the depletion mode of operation with the gate voltage smaller the flat band voltage ($V_G < V_{FB}$). On the other hand, the surface potential change and the band bending is very

limited even with a large change of the gate bias under the accumulation mode of operation with the gate voltage higher than the flat band voltage ($V_G > V_{FB}$). This is the region why we chose the flat band condition ($V_G = V_{FB}$, $\psi_S = 0$, and $E = E_{FB}$) as the boundary for the mapping of the surface potential to the subgap energy through the experimental C–V data.

We extract the intrinsic subgap DOS considering the CCF and $L_{DOS}(V_G)$ using the sub-bandgap photoresponsive C–V technique. Therefore, the subgap states close to E_C extracted from the experimental photonic C–V data are noted to be $g_A(E)$, and those far from E_C are noted to be $g_D(E)$. For the extraction of $g_D(E)$ far from the conduction band edge (E_C) under $V_G < V_{FB}$, the measured total capacitances under dark states and photonic states (C_{mD} [F] and C_{mP} [F]) are described by

$$\frac{1}{C_{mD}(V_G)} = \frac{1}{C_{ov}} + \frac{1}{C_{dep}(V_G)} \tag{20}$$

$$\frac{1}{C_{mP}(V_G)} = \frac{1}{C_{ov}} + \frac{1}{C_{dep}(V_G) + C_{ph,D}(V_G)} \tag{21}$$

with $C_{dep}(V_G)$ [F] as the V_G-dependent depletion capacitance. Therefore, the photoresponsive depletion capacitance $C_{ph,D}$ [F] by optically excited charges from the subgap DOS can be obtained from

$$C_{ph,D}(V_G) = \frac{C_{mP}(V_G)\times C_{dep}(V_G) + C_{ov}\times C_{mP}(V_G) - C_{dep}(V_G)\times C_{ov}}{C_{ov} - C_{mP}(V_G)}. \tag{22}$$

For the differential bias range of $\Delta V_G = V_{G1} - V_{G2}$, we obtain the photonic depletion capacitance $\Delta C_{ph,D}$ as

$$\Delta C_{ph,D} = C_{ph,D}(V_{G1}) - C_{ph,D}(V_{G2})(V_G \le V_{FB}). \tag{23}$$

In the same way, for the extraction of $g_A(E)$ close to E_C for $V_G > V_{FB}$, C_{mD}, C_{mP}, and $C_{ph,A}$ [F] can be obtained through

$$\frac{1}{C_{mD}(V_G)} = \frac{1}{C_{ox}WL_m} + \frac{1}{C_{acc}(V_G)} \tag{24}$$

$$\frac{1}{C_{mP}(V_G)} = \frac{1}{C_{ox}WL_m} + \frac{1}{C_{acc}(V_G) + C_{ph,A}(V_G)} \tag{25}$$

$$C_{ph,A}(V_G) = C_{ox}WL_m\left[\frac{C_{mP}(V_G)}{C_{ox}WL_m - C_{mP}(V_G)} - \frac{C_{mD}(V_G)}{C_{ox}WL_m - C_{mD}(V_G)}\right] \tag{26}$$

with C_{acc} [F] as the capacitance for the accumulated electrons. Therefore, $\Delta C_{ph,A}$ can be obtained from

$$\Delta C_{ph,A} = C_{ph,A}(V_G + \Delta V_G) - C_{ph,A}(V_G)(V_G > V_{FB}). \tag{27}$$

Considering the CCF and $L_{DOS}(V_G)$ for the active region, we finally obtain $g_D(E)$ and $g_A(E)$ [eV^{-1}cm^{-3}] through

$$g_D(E) = \frac{(d\Delta Q_{ph,D}(E)/dE)}{v_{eff}\times q} = \frac{\Delta C_{ph,D}(V_G)}{q^2 T_{IGZO} W L_{DOS}(V_G)} \tag{28}$$

$$g_A(E) = \frac{(d\Delta Q_{ph,A}(E)/dE)}{v_{eff}\times q} = \frac{\Delta C_{ph,A}(V_G)}{q^2 T_{IGZO} W L_{DOS}(V_G)} \tag{29}$$

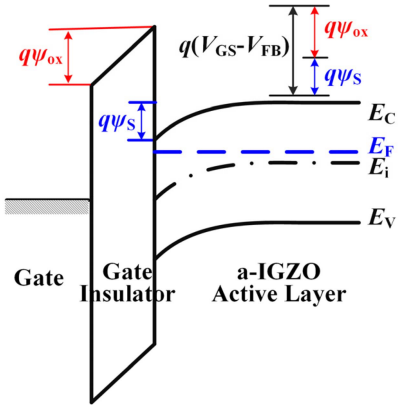

Fig. 4. Energy band diagram and V_{GS}-dependent ψ_S across the MIS system in a-IGZO TFTs.

with v_{eff} as the effective volume defined as

$$v_{eff} \equiv T_{IGZO} W L_{DOS}(V_G) = T_{IGZO} W(\alpha(V_G)L_m + 2L_{ov}). \tag{30}$$

The relationship between the gate bias (V_G) and the surface potential (ψ_S) for the mapping to the energy level across the MIS system in Fig. 4 is described as

$$V_G - V_{FB} = \psi_{mg}(V_G) + \psi_{ox}(V_G) + \psi_S(V_G) \cong \psi_{ox}(V_G) + \psi_S(V_G) = \psi_S(V_G)\left(1 + \frac{C_S(V_G)}{C_{ox}}\right) \tag{31}$$

$$\psi_S(V_G) = \frac{V_G - V_{FB}}{m(V_G)}; \quad m(V_G) \equiv \left(1 + \frac{C_S(V_G)}{C_{ox}}\right) \tag{32}$$

with ψ_{mg} as the potential across the metal gate, ψ_{ox} as the potential across the gate oxide, V_{FB} as the flat band voltage, and Q_S as the substrate charge.

We note that the flat band voltage (V_{FB}), as the gate voltage for the surface potential to be zero ($\psi_S = 0$) and for the energy band to be flat all over the MIS system, is experimentally obtained from the C–V data at the maximum point of the gate voltage in the differential C–V graph through

$$V_{FB} \equiv V_G|_{|dC_G/dV_G|_{max}}. \tag{33}$$

At the flat band voltage ($V_G = V_{FB}$), the bias condition changes from the depletion state to the accumulation state in n-channel accumulation type TFTs. In the depletion state ($V_G < V_{FB}$ & $\psi_S < 0$), the substrate charge Q_S is dominated by the depletion charge (Q_{Sd}) and proportional to the square root of the surface potential, while Q_S in the accumulation state ($V_G > V_{FB}$ & $\psi_S > 0$) is dominated by the accumulated electrons (Q_{Smn}) and exponentially proportional to ψ_S. Therefore, the gate capacitance as a function of the gate bias changes abruptly at the flat band bias. This is why we obtain the flat band voltage from the maximum point of the gate bias in the differential C–V graph from the experimental C–V data.

The flat band voltage (V_{FB}) is used as a reference voltage for the nonlinear mapping of the gate voltage (V_G) to the surface

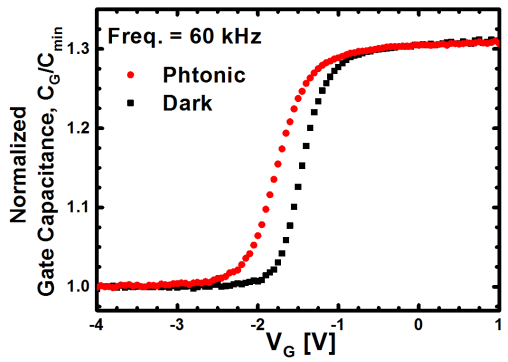

Fig. 5. Measured C_G–V_G (normalized to $C_{\min}$) characteristics of a-IGZO TFTs with an inverted staggered bottom-gate having W/L_m =10/26 μm under dark (black closed line) and sub-bandgap ($E_{\rm ph}$ = 2.6 eV, $P_{\rm opt}$ = 10 mW) photonic (red line) states.

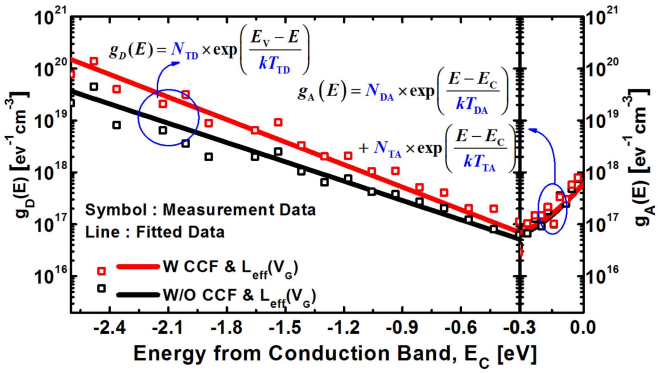

Fig. 6. Extracted subgap DOS though the sub-bandgap photoresponsive C–V technique with exponential DOS models. (a) Donor-like DOS. (b) Acceptor-like DOS. Black line: before considering $L_{\rm eff}(V_G)$. Red line: after considering $L_{\rm eff}(V_G)$.

potential (ψ_S) and finally to the energy level ($E - E_C$) through

$$\psi_{S,A}(V_G) = -\int_{V_{\rm FB}}^{V_G}\left(1+\frac{C_S(V_G)}{C_{\rm ox}}\right)dV_G : (V_G > V_{\rm FB}\ \&\ \psi_{S,A} > 0) \tag{34}$$

$$\psi_{S,D}(V_G) = -\int_{V_{\rm FB}}^{V_G}\left(1+\frac{C_S(V_G)}{C_{\rm ox}}\right)dV_G : (V_G < V_{\rm FB}\ \&\ \psi_{S,D} < 0) \tag{35}$$

from V_G-dependent experimental C–V data. We finally map the experimentally obtained surface potential from the C–V data to the V_G-dependent energy level [$E(V_G)$] through

$$E(V_G) = E_C - E_{\rm FB} + q\psi_S(V_G) \tag{36}$$

with $E_F(V_G)$ as the $V_{\rm GS}$-dependent quasi-Fermi level and $E_{\rm FB}$ defined as $E_C - E_F$ at $V_G = V_{\rm FB}$.

We note that the border energy ($E_C - E_{\rm FB}$) for the calculation of the surface potential to the energy was obtained at the flat band condition ($V_G = V_{\rm FB}$ and/or $\psi_S = 0$) as a reference for the nonlinear mapping of the gate voltage to the energy level through the surface potential. It is obtained from

$$E_C - E_{\rm FB} = kT\ln\left(N_C/n_o|_{\substack{\rm Flat\\ \rm Band}}\right) = kT\ln(N_C/N_D). \tag{37}$$

III. Experimental Results and Discussion

In order to experimentally extract the intrinsic subgap DOS considering the CCF model and $L_{\rm eff}(V_G)$ in Fig. 3, we employed a-IGZO TFTs with an inverted staggered bottom-gate having W/L_m = 10/26 μm, the thickness of the gate insulator (SiO_2) $T_{\rm GI}$ = 200 nm, the active layer thickness $T_{\rm IGZO}$ = 30 nm, and the $C_{G\text{–SD}}$ overlap length $L_{\rm ov} = L_{{\rm ov},S} = L_{{\rm ov},D}$ = 6 μm. As shown in Fig. 5, we obtained experimental C_G–V_G characteristics under dark and photonic states at low frequency (60 kHz) using the HP4284A LCR precision meter. For C–V measurement under photonic excitation, we applied a sub-bandgap optical source ($E_{\rm ph}$ = 2.6 eV) with the optical fiber diameter d = 50 μm and the optical power $P_{\rm opt}$ = 10 mW.

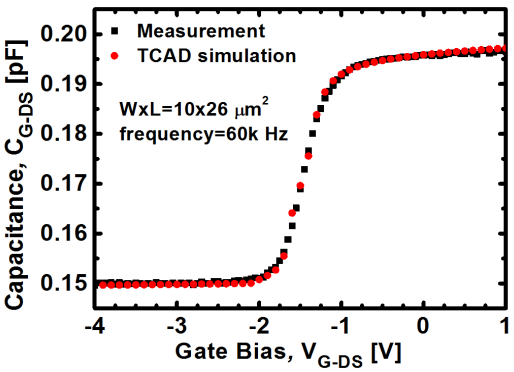

Fig. 7. TCAD simulation result for the $C_{G\text{–SD}}$ capacitance ($C_{G\text{–SD}}$–V_G) with extracted subgap DOS though the sub-bandgap photoresponsive C–V technique compared with exponential DOS models ($N_{\rm TD}$ = 1.5 × 10^{20} eV^{-1}cm^{-3}, $kT_{\rm TD}$ = 0.25 eV, $N_{\rm TA}$ = 5 × 10^{17} eV^{-1}cm^{-3}, $kT_{\rm TA}$ = 0.08 eV, $N_{\rm DA}$ = 1.2 × 10^{17} eV^{-1}cm^{-3}, and $kT_{\rm DA}$ = 0.4 eV.

Fig. 6 shows the extracted intrinsic subgap DOS considering the empirical CCF model and $L_{\rm DOS}(V_G)$ with a superposition of deep and tail states in exponential forms as

$$g_D(E) = N_{\rm TD}\exp\left(\frac{E_V - E}{kT_{\rm TD}}\right) \tag{38}$$

$$g_A(E) = N_{\rm DA}\exp\left(\frac{E-E_C}{kT_{\rm DA}}\right) + N_{\rm TA}\exp\left(\frac{E-E_C}{kT_{\rm TA}}\right). \tag{39}$$

Extracted parameters for the supposed exponential DOS models are $N_{\rm TD}$ = 1.5 × 10^{20} eV^{-1}cm^{-3} with $kT_{\rm TD}$ = 0.3 eV for $g_{\rm TD}(E)$ far from E_C, $N_{\rm TA}$ = 5 × 10^{17} eV^{-1}cm^{-3} with $kT_{\rm TA}$ = 0.08 eV for $g_{\rm TA}(E)$, and $N_{\rm DA}$ = 1.2×10^{17} eV^{-1}cm^{-3} with $kT_{\rm DA}$ = 0.4 eV for $g_{\rm DA}(E)$ close to E_C with $E_{\rm FB} - E_C$ = −0.3 eV for $N_C/N_D \sim 10^5$. The V_G-dependent channel conduction factor is significant in the gate-bias below the threshold, which is the main bias condition for the extraction of deep and tail state subgap DOS in AOS TFTs through the C–V characterization.

TCAD simulation result considering the empirical channel conduction factor $\alpha(V_G)$ for the $C_{G\text{–SD}}$ capacitance ($C_{G\text{–SD}}$–V_G) characteristics is compared with the experimental

data in Fig. 7. The simulated C–V characteristics are consistent with the measured C–V characteristics all over the gate bias.

IV. Conclusion

We reported an empirical channel conduction factor model [$\alpha(V_G)$] and the effective channel length [$L_{\text{eff}}(V_G)$] for the extraction of the intrinsic subgap DOS in AOS TFTs through the C–V measurement. We defined $L_{\text{eff}}(V_G)$ through the product of the CCF and the metallurgical channel length. We note that the gate bias-dependent channel conductivity effect is significant in the subgap DOS on the energy level far from E_C due to the low conductivity of the channel below the threshold gate bias. We also note that it is important to consider the CCF model with $L_{\text{eff}}(V_G)$ for the C–V-based characterization and modeling of the intrinsic subgap DOS in amorphous semiconductor TFTs.

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Hyunjun Choi received the B.S. and M.S. degrees in electrical engineering from Kookmin University, Seoul, Korea, in 2012 and 2014, respectively.

He is currently with LG Display Company, Ltd., Seoul. His current research interests include nanoCMOS and oxide thin-film transistors devices.

Jungmin Lee received the B.S. degree in electrical engineering from Kookmin University, Seoul, Korea, in 2014, where he is currently pursuing the M.S. degree with the Department of Electrical Engineering.

Hagyoul Bae received the B.S. and M.S. degrees from Kookmin University, Seoul, Korea, in 2007 and 2009, respectively. He is currently pursuing the Ph.D. degree with the Korea Advanced Institute of Science and Technology, Daejeon, Korea.

His current research interests include characterization and modeling of silicon nanostructure devices, flash memory devices, amorphous oxide semiconductor thin-film transistors, and their device physics.

Sung-Jin Choi received the M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2012.

He is currently an Assistant Professor with the School of Electrical Engineering, Kookmin University, Seoul, Korea.

Dae Hwan Kim (M'08) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2002, respectively.

He joined the School of Electrical Engineering, Kookmin University, Seoul, in 2005, where he is currently an Associate Professor.

Dong Myong Kim (S'86–M'88) received the B.S. (*magna cum laude*) and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1986 and 1988, respectively, and the Ph.D. degree in electrical engineering from the University of Minnesota, Twin Cities, MN, USA, in 1993.

He has been with the School of Electrical Engineering, Kookmin University, Seoul, since 1993.