

High performance amorphous oxide thin film transistors with self-aligned top-gate structure

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Abstract

We have demonstrated self-aligned top-gate amorphous oxide TFTs for large size and high resolution displays. The processes such as source/drain and channel engineering have been developed to realize the self-aligned top gate structure. Ar plasma is exposed on the source/drain region of active layer to minimize the source/drain series resistances. To prevent the conductive channel, N₂O plasma is also treated on the channel region of active layer. We obtain a field effect mobility of 5.5 cm²/V·s, a threshold voltage of 1.1 V, and a sub-threshold swing of 0.35 V/decade at sub-micron a-GIZO TFTs with the length of 0.6 μm. Furthermore, a-IZO TFTs fabricated for gate and data driver circuits on glass substrate exhibit excellent electrical properties such as a field effect mobility of 115 cm²/V·s, a threshold voltage of 0.2 V, a sub-threshold swing of 0.2 V/decade, and low threshold voltage shift less than 1 V under bias temperature stress for 3 hr.

Introduction

According to recent liquid crystal display (LCD) and organic light emitting display (OLED) technology trends, displays become bigger and bigger over 100 inch and the resolution of LCD TV and information display will be increased from 1920x1080 to 4096x2160 level for a high quality of image.[1,2] In addition to that, a frame rate is also enhanced from 60 Hz to 120 Hz to improve a motion-picture quality.[2-4]

As for the pixel switching thin-film transistors (TFTs), higher resolution and faster driving speed, i.e. higher frame rate, make a “turn-on-time (t_{on})” of TFT be shorter. We refer the turn-on-time of TFT as a theoretical period of time available for charging each pixel. For example, the t_{on} is reduced from 15 μs of FHD (1920x1080) resolution to 8 μs of UHD (ultra high definition, 4096x2160) one for 60 Hz-driving. If the frame rate of UHD display is increased from 60 Hz to 120 Hz, the t_{on} is decreased again to 4 μs. As the display size is increased, actual t_{on} become much shorter due to an increased signal RC(resistance-capacitance, τ_{RC}) delay of gate and data line. This means that a pixel TFT should operate faster enough to charge the pixel within the shorter period. Thus, low parasitic capacitance and high mobility of

switching TFT are required. For that reason, oxide TFT which has recently attracted considerable attention for high mobility is selected. So far, oxide TFTs have been generally developed only as a normal bottom-gate structure or a normal top-gate structure, as shown in the Fig. 1. However, they are unsuitable for the pixel transistors of large size and high resolution display because they have a high parasitic capacitance due to gate-source/drain overlap, a poor device scalability, and the sharp degradation of drain current by gate-source/drain misalignment, as shown in the Fig. 2. Therefore, the development of the self-aligned top-gate structure is necessary. In this study, we intend to investigate how to effectively fabricate the self-aligned top-gate oxide TFTs and their electrical properties. In addition, we intend to research the effect of various plasma treatment applied on the source/drain region of active layer for lowering the series resistance between source/drain metal and channel, and the effect of oxygen plasma treated for protecting the channel region of active layer from hydrogen. These processes are very simple and cost-effective compared with silicon technology which doping and activation processes need. Oxide semiconductor materials used in here are amorphous GaInZnO (a-GIZO) and amorphous InZnO (a-IZO).

Experimental

A schematic cross section of an integrated oxide TFT is shown in Fig. 3. The TFT structure used is of the self-aligned top-gate type. All the processes were performed at a low temperature of less than 200 °C in order to avoid the shrinkage problem of glass substrates. In order to fabricate this structure, an a-GIZO (or a-IZO) active layer was first sputtered by radio frequency (rf) magnetron sputtering at room temperature and then wet-etched with diluted HF (hydrofluoric) acid. After the N₂O plasma was treated on the active layer, 100-nm-thick layer of a-SiO₂ as the gate insulator was deposited without vacuum break at 150 °C by plasma enhanced chemical vapor deposition (PECVD) on the active layer. A 100-nm-thick layer of molybdenum (Mo) as the gate metal was sequentially sputtered at room temperature. These two layers were continuously dry-etched using a gate pattern. This process was followed by Ar (or NH₃) plasma treatment on the source/drain region (n⁺) of the

active layer to obtain the low series resistance. Then, a 200-nm-thick a-SiO₂ interlayer dielectric (ILD) was deposited by PECVD at 150 °C and then dry etched. Finally, a 200-nm-thick layer of Mo as the source/drain metal was sputtered at room temperature and then patterned by dry etching.

Results and Discussion

Ar and NH₃ plasmas were treated on the source/drain region of the a-GIZO active layer to reduce the source/drain parasitic resistances such as sheet and contact resistances Fig. 4 (a) and (b) show the resistivity of the source/drain region of a-GIZO TFT as a function of plasma treatment time for Ar and NH₃ plasmas; Fig. 4 (c) and (d) show the sheet resistance of the source/drain region of a-GIZO TFT as a function of a-GIZO thickness for Ar and NH₃ plasmas. Both exhibit a similar resistivity of 0.01 Ω·cm and a similar sheet resistance of 1 kΩ/□ while NH₃ plasma is faster than Ar plasma with respect to saturation start value, that is, 40 s and 30 nm for Ar plasma, 20 s and 20 nm for NH₃ plasma. Fig 5 shows voltage-current curves for Ar and NH₃ plasmas at the source/drain contact between plasma treated a-GIZO and Mo. These also exhibit a similar contact resistivity of 5×10^{-5} Ω·cm². Fig 6(a) shows the RBS spectra of chemical elements as a function of the Ar plasma treatment time. In all the samples, the concentrations of gallium, zinc, and oxygen remain almost unchanged, while that of indium In changes considerably. This result shows that the sharp reduction in sheet resistance is due to the increased concentration of segregated In at the surface of a-GIZO thin film. The concentration of In in the In-excessive region slightly increases near the surface with the Ar plasma treatment time, maintaining a constant thickness of about 3 nm. It appears that the relatively weak In–O bonds are preferentially broken by ion bombardment and then In atoms collect near the surface owing to the positive mixing enthalpy and high surface energy. Fig 6(d) shows the high-resolution elastic recoil detection analysis (HR-ERDA) spectra of hydrogen in a-GIZO thin films with different plasma treatment times. The concentration and the intrusion depth of hydrogen in the a-GIZO thin film continuously increased as the NH₃ plasma treatment time increased from 20 to 120 s. In the case of the sample treated for 120 s, the detectable hydrogen-rich region was about 4 nm from the surface, and the average concentration of hydrogen in that region was about 10 at%. From these results, we can infer that the NH₃ plasma treatment changed the a-GIZO thin film from a semiconductor to a conductor, i.e., the hydrogen dissociated from the NH₃ plasma diffused into the a-GIZO active layer and acted as a shallow donor in a-GIZO semiconductor.

Since hydrogens dissociated from SiH₄, one of input gases on depositing gate insulator, make the electrical properties of oxide TFTs conductive, N₂O channel-passivation process was conducted to recover the conductive characteristics of a-GIZO. N₂O gas (1.73 eV) was selected, because the enthalpy for oxygen formation is much lower with O₂ gas (4.13 eV);

thus, it can avoid a-GIZO from becoming conductive via ion bombardment, because plasma can be generated at low RF power. Fig. 7 shows the effect of N₂O surface treatment before the deposition of gate insulator. Oxygens dissociated from N₂O effectively prevent the heavy intrusion of hydrogen into the channel depth. Fig. 8 shows transfer and output curves of N₂O passivated a-GIZO TFTs for Ar and NH₃ source/drain plasma treatments. Both show similar TFT characteristics. They exhibit good transfer TFT characteristics at a drain voltage of 10.1 V such as subthreshold swing of 0.2 V/decade, minimum off current of 1 pA, threshold voltage of 0.2 V, field effect mobility of 5~6 cm²/Vs, and on/off ratio of 7. In addition, the output curve exhibits a good output resistance in the saturation region. Fig 9 shows the electrical properties of a-GIZO TFTs as a function of channel length. N₂O channel-passivated and Ar source/drain-treated sub-micron a-GIZO TFTs show a field effect mobility of 5.5 cm²/V·s, a threshold voltage of 1.1 V, and sub-threshold swing of 0.35 V/decade. To apply oxide TFT to be integrated on glass substrate for gate and data driver, oxide TFTs with higher mobility are needed and they can be achieved by using oxide semiconductor materials with high carrier density. a-IZO as an active layer is selected. As shown in Fig. 10, a-IZO TFTs exhibit excellent device performances such as a field effect mobility of 115 cm²/V·s, a threshold voltage of 0.2 V, a sub-threshold swing of 0.2 V/decade, and a threshold voltage shift of 0.5 V against negative bias temperature stress (off-state driving condition of LCD panel) for 3 hr. Because transistors of LCD panel are mostly placed under off-state stress condition, stable electrical characteristic for many hours against negative bias temperature stress (NBTS) is very important.

Conclusion

We successfully fabricated self-aligned top-gate oxide TFTs and obtained good electrical properties. It is important to reduce the series resistances of the source/drain region, protect channel from hydrogen and increase the carrier density of active layer in order to acquire good TFT characteristics for a self-aligned top-gate structure. Therefore, Ar plasma for source/drain engineering and N₂O plasma for channel engineering are applied. a-IZO TFTs fabricated by these processes show a field effect mobility of 115 cm²/V·s, a threshold voltage of 0.2 V, a sub-threshold swing of 0.2 V/decade. In addition, their threshold voltage is not nearly shifted at the bias temperature stress for 3 hr.

References

- [1] S. W. Lee, FPD international 2007 Forum, keynote lecture S-1 (2007)
- [2] S. S. Kim, N. D. Kim, B. H. Berkeley, B. H. You, H-S. Nam, J-H. Park, and J-P. Lee, Digest of Tech. Papers of Society for Information Display (SID), vol.38, 1003 (2007).
- [3] T. Kurita, Digest of Tech. Papers of Society for Information Display (SID), 986 (2001).
- [4] Y. Igarashi, T. Yamamoto, Y. Tanaka, J. Someya, Y. Nakakura, M. Yamakawa, S. Hasegawa, Y. Nishida, and T. Kurita, SID symposium digest-2003, 1039 (2003).

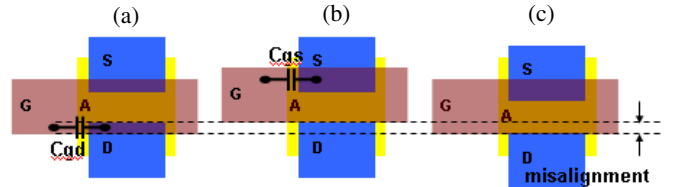
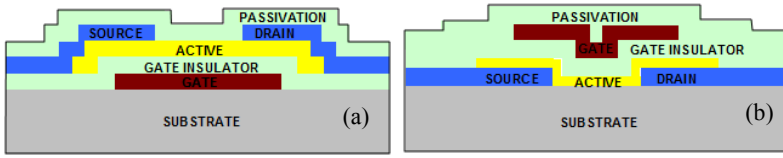


Fig. 2. (a) Top-view, (b) gate misalignment, and (c) source/drain misalignment of normal bottom-gate/normal top-gate structure on the photolithography

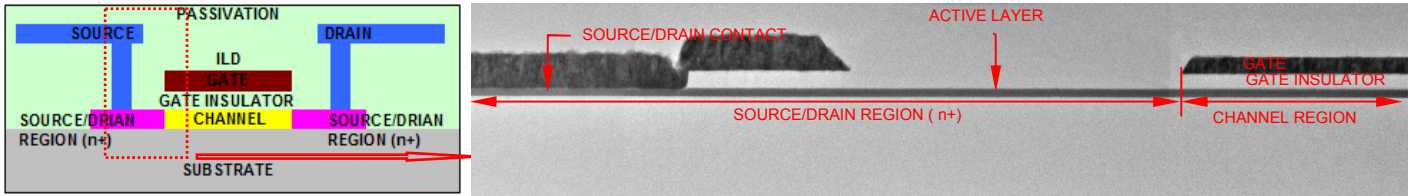


Fig. 3. Cross sectional TEM (Transmission Electron Microscope) image of self-aligned top-gate structure

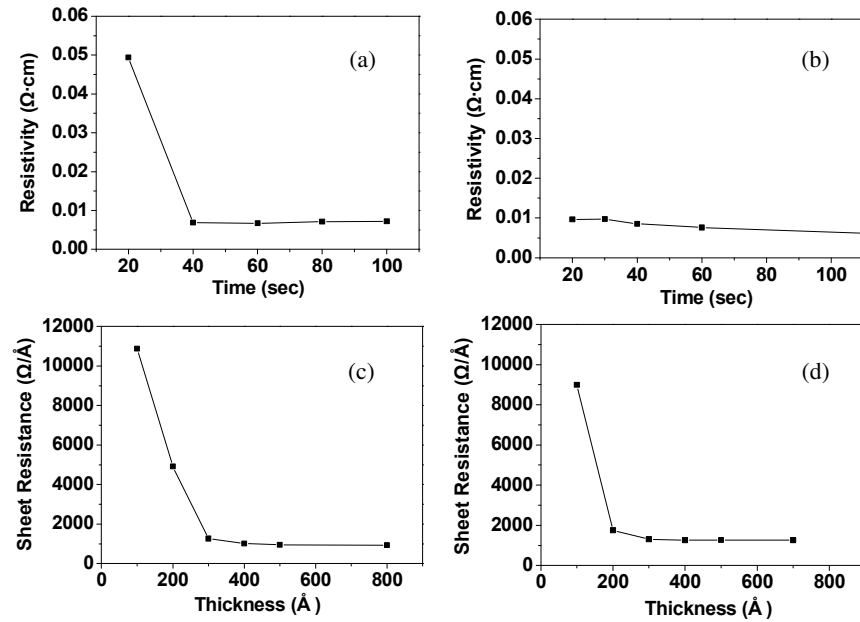


Fig. 4. The resistivity as a function of (a) Ar plasma treatment time and (b) NH_3 plasma treatment time at a fixed a-GIZO thickness of 70 nm. The sheet resistance as a function of the a-GIZO thickness for (c) Ar plasma and (d) NH_3 plasma at a fixed plasma treatment time of 60 s.

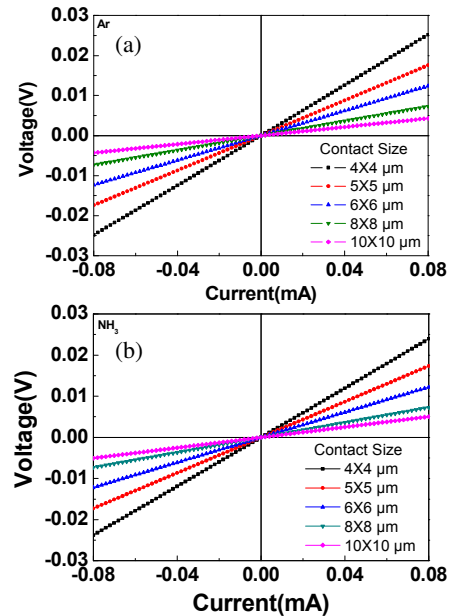


Fig. 5. The voltage-current curves of a-GIZO/Mo contacts for (a) the Ar plasma treatment and (b) the NH_3 plasma treatment with the different contact sizes. The a-GIZO thickness and the plasma treatment time are 70 nm and 60 s, respectively.

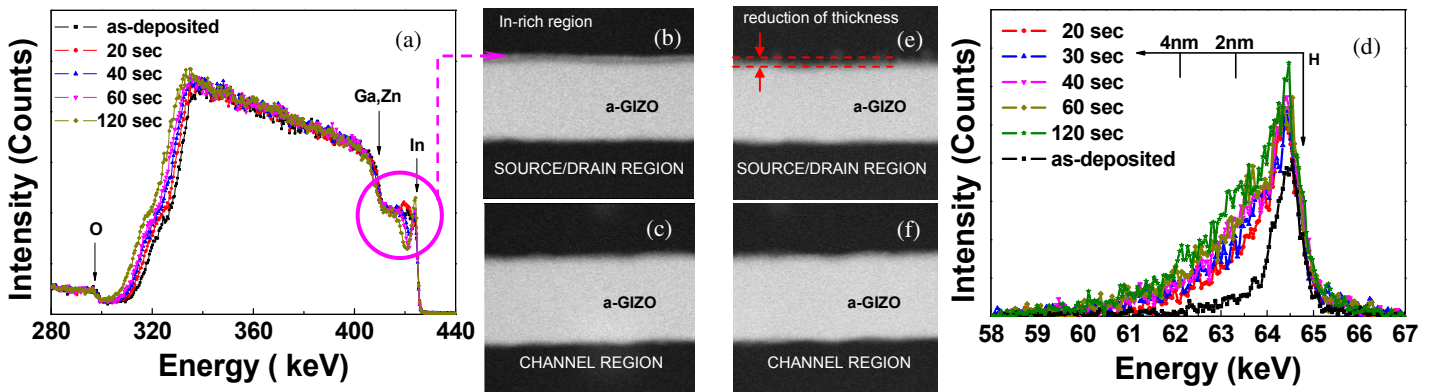


Fig. 6. (a) RBS (rutherford backscattering spectroscopy) spectra of source/drain region; TEM images of (b) source/drain region and (c) channel region of an a-GIZO active layer for the Ar plasma treatment. (d) RBS spectra of source/drain region; TEM images of (e) source/drain region and (f) channel region of an a-GIZO active layer for the NH_3 plasma treatment. The a-GIZO thickness and the plasma treatment time are 70 nm and 60 s, respectively.

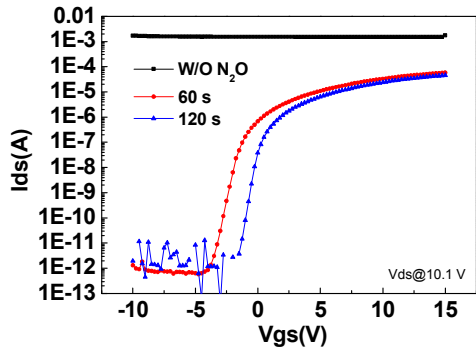


Fig. 7. The transfer characteristics with and without N_2O channel-passivated plasma on the active layer of a-GIZO TFT before the deposition of gate insulator. The source/drain region is treated by the Ar plasma for 60 s. The width/length of a-GIZO TFTs used is $10/10 \mu m$.

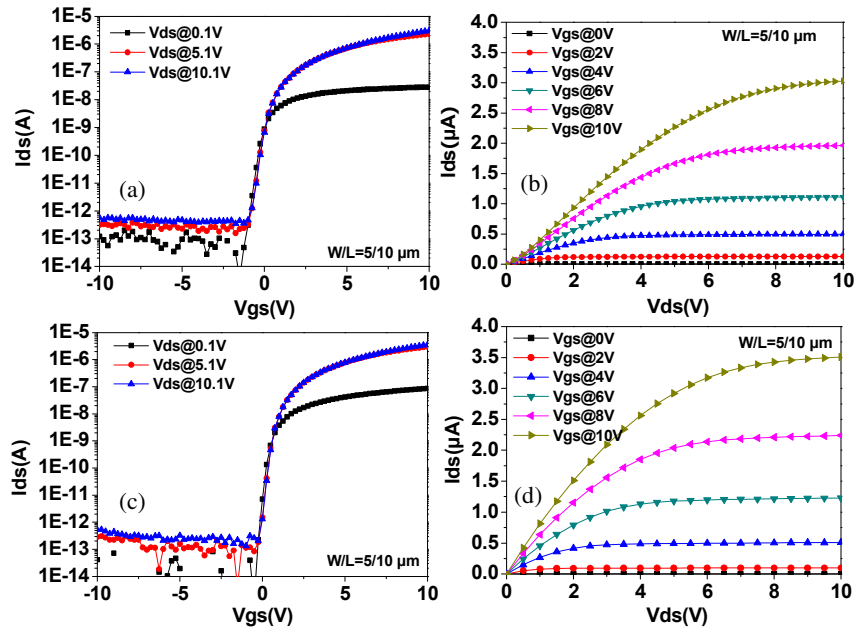


Fig. 8. (a) I_{ds} - V_{gs} curves and (b) I_{ds} - V_{ds} curves of Ar source/drain plasma treatment. (c) I_{ds} - V_{gs} curves and (d) I_{ds} - V_{ds} curves of NH_3 source/drain plasma treatment. The width/length of a-GIZO TFTs is $5/10 \mu m$. The a-GIZO thickness and the source/drain plasma treatment time are 70 nm and 60 s, respectively.

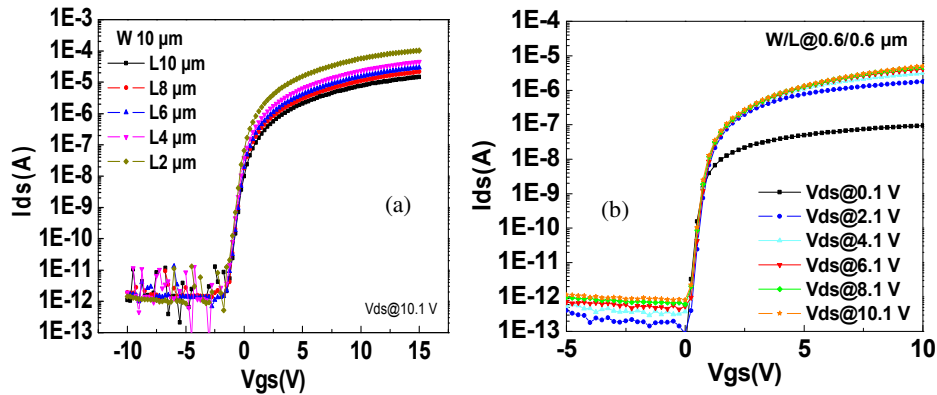


Fig. 9. (a) The transfer curves of a-GIZO TFT as a function of channel length with the fixed channel width of 10 μm . (b) The transfer curves of a-GIZO TFT in terms of drain voltages with the channel width/length of $0.6/0.6 \mu m$. The a-GIZO thickness and the Ar source/drain plasma treatment time are 70 nm and 60 s, respectively.

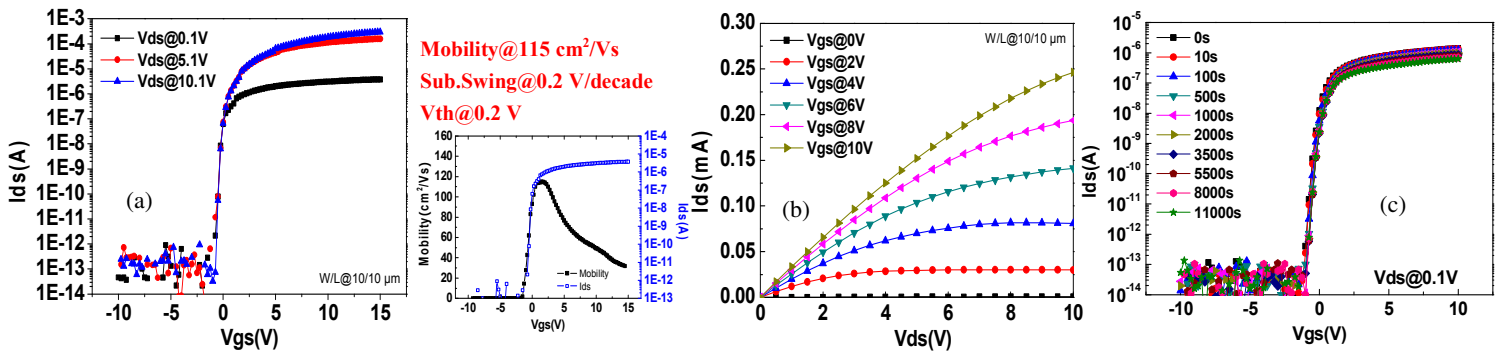


Fig. 10. (a) The transfer curves, (b) the output curves, and (c) NBTS (negative bias temperature stress) characteristic of a-IZO TFT with the channel width/length of $10/10 \mu m$. The a-IZO thickness and the Ar source/drain plasma treatment time are 50 nm and 60 s, respectively. NBTS conditions are V_g of -20 V, V_d of 0.1 V, V_s of 0 V, temperature of $60^\circ C$, and stress time of 3 hr.