# Dual-Sweep Combinational Transconductance Technique for Separate Extraction of Parasitic Resistances in Amorphous Thin-Film Transistors

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***Abstract*— We report a dual-sweep combinational transconductance technique for separate extraction of parasitic source ($R_S$) and drain ($R_D$) resistances in thin-film transistors (TFTs) by combining forward and reverse transfer characteristics. In the proposed technique, gate bias-dependent total resistance [$R_{TOT}$ ($V_{GS}$)] and degradation of the transconductance due to the parasitic resistance at the source terminal during the dual-sweep characterization are employed. Applying the proposed technique to amorphous oxide semiconductor TFTs with various combinations of channel length ($L$) and width ($W$), we successfully separated $R_S$ and $R_D$. A model for the $W$- and $L$-dependences of the extracted parasitic resistances is also provided.**

***Index Terms*— Parasitic resistance, source resistance, drain resistance, thin film transistors, dual-sweep, TFT.**

## I. Introduction

AMORPHOUS Indium-Gallium-Zinc-Oxide (a-IGZO) thin film transistors (TFTs) have recently emerged as prospective devices for next generation active matrix-liquid crystal display and active matrix-organic light emitting diode due to low temperature process, good uniformity, and high carrier mobility [1], [2]. As the demand for various a-IGZO TFT-based applications explosively increases, accurate modeling and separate extraction of the parasitic source and drain resistances ($R_S$ and $R_D$) of a-IGZO TFTs become indispensable for a robust characterization of degradation mechanisms and a systematic design of a-IGZO TFT-based circuitry. In particular, the $R_{SD} = R_S + R_D$ is comparable to the channel resistance ($R_{ch}$) in the "ON"-state of TFTs. This result in considerable voltage drop across the resistance to be considered in the operation and characterization of TFTs. The asymmetric property of $R_S$ and $R_D$ is also caused by layout, process variation, and long term device degradation.

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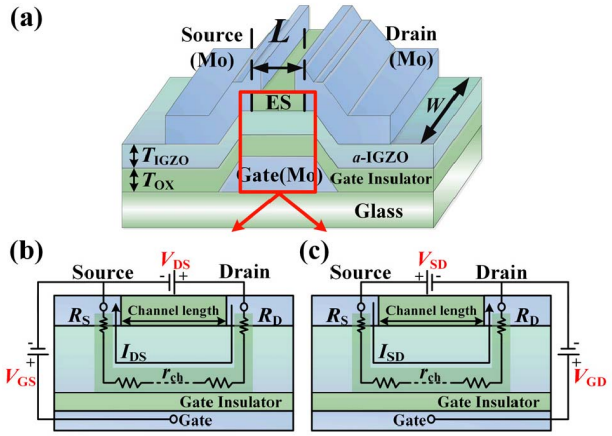


Fig. 1. (a) Schematic view of a-IGZO with an inverted staggered bottom-gate structure. Cross-sectional view and equivalent circuit for a-IGZO TFTs with $R_S$ and $R_D$ in (b) the forward operation mode and (c) the reverse configuration.

Therefore, the separate extraction technique is significantly important for characterization of relevant physical mechanisms. There have been reports on analysis of total parasitic resistances in TFTs [3]–[5]. In previous techniques employing capacitance-voltage (C-V) characteristics, there is a limit in the separate extraction of $R_S$ and $R_D$ due to the frequency-dispersive C-V characteristics [6] and severe fluctuation measured data at low frequency.

We report a current-voltage (I-V)-based combinational transconductance technique for separate extraction of $R_S$ and $R_D$ in a-IGZO TFTs. Through the proposed technique combining the degradation of the transconductance caused by the parasitic resistance at the source terminal during the forward and reverse (bi-directional) measurement of transfer characteristics $R_S$ and $R_D$ can be separated with consistent measurement. The proposed fully I-V-based technique is useful in separate extraction of $R_S$ and $R_D$ for amorphous TFTs compared with C-V-based techniques. Also, the proposed technique based on the measurement of a single device is useful for separate extraction of $R_S$ and $R_D$ because the asymmetry may vary from device to device.

## II. Dual-Sweep Combinational Transconductance Technique

As shown in Fig. 1, parasitic resistances in a-IGZO TFTs can be characterized by the equivalent circuit with $R_S$ and $R_D$ connected in series with its intrinsic source and drain nodes.

We note that there are voltage drops across the parasitic resistances ($R_S$ and $R_S$) and that the intrinsic gate ($V_{GS,int}$) and drain ($V_{DS,int}$) voltages should be implemented as $V_{GS,int} \equiv V_{GS} - I_{DS}R_S$ and $V_{DS,int} \equiv V_{DS} - I_{DS}(R_S + R_D)$, respectively. Therefore, the saturated drain current ($I_{DS}$) can be described as

$$I_{DS} = \frac{\mu_{eff} C_{OX}}{2} \left(\frac{W}{L}\right) (V_{GS} - I_{DS}R_S - V_T)^2 \quad (1)$$

with $V_T$ as the threshold voltage, $\mu_{eff}$ as the channel carrier mobility, $C_{OX}$ as the oxide capacitance, and $(W/L)$ as the channel width-to-length ratio. Considering voltage drops across $R_S$ and $R_D$ under saturation region, the extrinsic ($g_m$) and intrinsic ($g_{mo}$) transconductances as a function of $V_{GS}$ are obtained through

$$g_m(V_{GS}) = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) \times (V_{GS} - I_{DS}R_S - V_T)\left(1 - \frac{\partial I_{DS}}{\partial V_{GS}} R_S\right) \quad (2)$$

$$g_{mo}(V_{GS}) = \frac{\partial I_{DS}}{\partial V_{GS,int}} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) (V_{GS} - I_{DS}R_S - V_T). \quad (3)$$

This allows us to relate $g_{mo}$ [7] to $g_m$ as

$$g_{mo} = \frac{g_m}{(1 - g_m R_S)} \quad \text{or} \quad g_m = \frac{g_{mo}}{(1 + g_{mo} R_S)}. \quad (4)$$

We note that these equations are correct even if $\mu_{eff}$ is dependent on $V_{GS}$. The intrinsic variables are the same for both forward and reverse mode configurations, except the possible asymmetry in $R_S$ and $R_D$. In each configuration for the dual-sweep combinational transconductance characterization, $g_{mo}$ reflects the voltage drop across the parasitic source resistance. Therefore, $R_S$ and $R_D$ are considered in $g_{mo,fwd}$ and $g_{mo,rev}$ of the forward and reverse configurations (the drain terminal in the forward mode works as the source terminal in the reverse mode, and vice versa), respectively, as in Eq. (4). Because that $g_{mo,fwd}$ and $g_{mo,rev}$ are subject only to the intrinsic variables and hence does not include the effect of $R_S$ and $R_D$, $g_{mo,fwd}$ is equal to $g_{mo,rev}$. Through the same $g_{mo}$ in the bi-directional dual-sweep configurations, the difference $(R_S - R_D)$ between $R_S$ and $R_D$ can be experimentally obtained from

$$(R_S - R_D) = \frac{g_{m,rev} - g_{m,fwd}}{g_{m,rev} g_{m,fwd}} \equiv R_{diff} \quad (5)$$

with $g_{m,fwd}$ as the transconductance obtained from the forward mode ($I_{DS}$–$V_{GS}$) transfer characteristics and $g_{m,rev}$ from the reverse mode ($I_{SD}$–$V_{GD}$). This is the key idea in the proposed dual-sweep combinational transconductance technique for separate extraction of $R_S$ and $R_D$ in insulated gate amorphous TFTs based on the transconductance degradation due to the parasitic resistance at the source terminal during the characterization.

We also note that, in the linear mode of operation under small drain voltage ($V_{DS}$), the drain current is described by

$$I_{DS} = \frac{\mu_{eff} C_{OX} W}{L} \left[(V_{GS} - I_{DS}R_S - V_T) \times (V_{DS} - I_{DS}(R_S + R_D))\right] \quad (6)$$

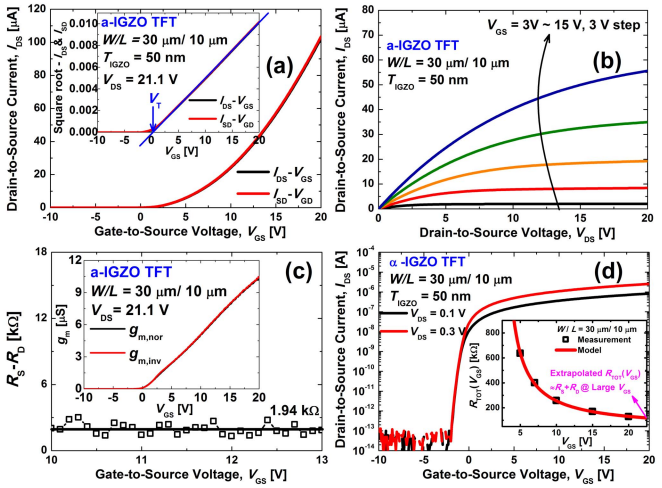


Fig. 2. (a) Measured transfer curves in forward and reverse configurations. Inset is the extracted $V_T$ from square root-$I_{DS}$. (b) Output curve of an a-IGZO TFT with $W/L = 30\ \mu m/10\ \mu m$. (c) The difference between $R_S$ and $R_D$ ($R_S - R_D$) calculated from the bi-directional transconductances ($g_{m,fwd}$ and $g_{m,rev}$). $g_{m,fwd}$ and $g_{m,rev}$ are obtained from measured transfer curves in forward and reverse modes, respectively, shown as an inset. (d) Measured transfer characteristics at small drain voltages. Inset is the experimental $R_{TOT}(V_{GS})$ with the extrapolated $R_S + R_D$.

with $R_S$ and $R_D$. The total resistance ($R_{TOT}$) can be summarized as

$$R_{TOT}(V_{GS}) \equiv \frac{V_{DS}}{I_{DS}} = R_S + R_D + L \times r_{ch} \quad (7)$$

with $r_{ch}$ as a $V_{GS}$-dependent channel resistance per unit length. Therefore, the sum of $R_S$ and $R_D$ can be experimentally extracted by the channel resistance method (CRM) through

$$R_S + R_D = V_{DS}/I_{DS}|_{extrapolated \ to \ V_{GS} \to \infty} \equiv R_{sum}. \quad (8)$$

Combining $R_{diff}(\equiv R_S - R_D)$ from the forward/reverse transconductance measurement and $R_{sum}(\equiv R_S + R_D)$ from the CRM result, we finally obtain $R_S$ and $R_D$ through

$$R_S = (R_{diff} + R_{sum})/2, \quad R_D = (R_{sum} - R_{diff})/2. \quad (9)$$

## III. Experimental Results and Discussion

For experimental verification of the dual-sweep combinational transconductance technique, we employed a-IGZO TFTs with a staggered bottom-gate structure. The thickness of the gate dielectric ($SiO_x$) $T_{GI} = 200$ nm, $L = 10\ \mu m$, $W = 30\ \mu m$, and the gate-to-S/D overlap length ($L_{ov}$) $= 6\ \mu m$. The passivation layer ($SiO_x$) was deposited on the top of TFTs.

For separate extraction of $R_S$ and $R_D$, transfer characteristics of TFTs are measured in the forward and reverse measurement configurations as shown in Fig. 2(a). As shown in the inset of Fig. 2(a), $V_T$ (=0.31 V) of forward and reverse configurations are the same. Through experimental output characteristics of Fig. 2(b), we primarily confirmed the gate voltage range to be in the saturation mode for the dual-sweep combinational transconductance technique. In the saturation region ($V_{Dsat} = V_{GS} - V_T < V_{DS}$), $g_{m,fwd}$ and $g_{m,rev}$ are obtained from the transfer curves for the forward and reverse configurations as the inset of Fig. 2(c). Therefore, $R_{diff} = R_S - R_D$ is experimentally extracted from Eq. (5) as shown in Fig. 2(c). Experimental results for the

TABLE I
PARASITIC SOURCE ($R_S$) AND DRAIN ($R_D$) RESISTANCES OF a-IGZO TFTs WITH VARIOUS $W$ AND $L$ COMBINATIONS

| $L$-dependent parasitic resistances in a-IGZO TFTs with $W$=30 $\mu$m | | | | |
|---|---|---|---|---|
| $W/L$ [$\mu$m/$\mu$m] | 30 /10 | 30 / 14 | 30 / 16 | 30 /20 |
| $R_S$ [k$\Omega$] | 17.38 | 23.57 | 26.35 | 30.16 |
| $R_{S,ext}$ [k$\Omega$] | 12.25 | 18.44 | 21.22 | 25.03 |
| $R_{SO}$ [k$\Omega$] | 5.13 | 5.13 | 5.13 | 5.13 |
| $R_D$ [k$\Omega$] | 15.44 | 19.15 | 20.43 | 24.79 |
| $R_{D,ext}$ [k$\Omega$] | 9.34 | 13.05 | 14.33 | 18.69 |
| $R_{DO}$ [k$\Omega$] | 6.10 | 6.10 | 6.10 | 6.10 |
| $W$-normalized $R_S$ [k$\Omega\cdot\mu$m] | 521.40 | 707.10 | 790.50 | 904.80 |
| $W$-normalized $R_D$ [k$\Omega\cdot\mu$m] | 463.20 | 574.50 | 612.90 | 743.70 |
| $W$-dependent parasitic resistances in a-IGZO TFTs with $L$=14 $\mu$m | | | | |
| $W/L$ [$\mu$m/$\mu$m] | 10 /14 | 14 / 14 | 30 / 14 | 36 /14 |
| $R_S$ [k$\Omega$] | 60.89 | 47.99 | 23.57 | 19.21 |
| $R_D$ [k$\Omega$] | 44.63 | 36.46 | 19.15 | 14.24 |
| $W$-normalized $R_S$ [k$\Omega\cdot\mu$m] | 608.90 | 671.86 | 707.10 | 691.56 |
| $W$-normalized $R_D$ [k$\Omega\cdot\mu$m] | 446.30 | 510.44 | 574.50 | 512.64 |

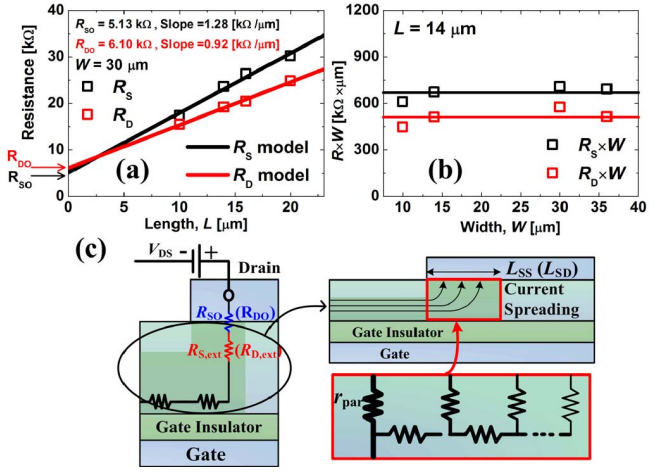


Fig. 3. (a) $L$-dependence of extracted $R_S$ and $R_D$ and (b) $W$-independence of normalized $R_S$ and $R_D$ in a-IGZO TFTs. (c) The current spreading phenomenon under the contact region.

$V_{GS}$-dependent $R_{TOT}$, as an inset of Fig. 2(d), are extracted from transfer characteristics of Fig. 2(d). Though Eqs. (7) and (8), $R_S + R_D$ is extracted under linear mode of operation. Extracted $R_S$ and $R_D$ [k$\Omega$] and normalized $R_S$ and $R_D$ ($R_S\cdot W$ and $R_D\cdot W$[k$\Omega\cdot\mu$m]) for a-IGZO TFTs with various $W$ and $L$ combinations are summarized in Table I.

We also modeled and characterized $L$- and $W$-dependences of $R_S$ and $R_D$ in TFTs. $L$-dependent $R_S$ ($R_D$) and $W$-independent $R_S \cdot W$ ($R_D \cdot W$) are also shown in Fig. 3(a) and (b). We note that $R_S$ and $R_D$ decrease with scaling down of the channel length in a-IGZO TFT as shown in Fig. 3(a). This is because the area of the vertical current path is extended under the contact region as the channel length gets shorter. As shown in Fig. 3(c), it is related to the current spreading. We note that the fringing field through the parasitic capacitance at the both edges of the gate-source and gate-drain overlap region strongly affects the channel conduction. Both the channel charge and the channel conductivity are modulated by the intrinsic part of the gate capacitance directly above the bottom gate and the parasitic part of the capacitance by the fringing field effect at the edges of the effective gate-source ($L_{SS}$) and gate-drain ($L_{SD}$) overlap regions. Therefore, the effective current path under the effective gate-source ($L_{SS}$) and gate-drain ($L_{SD}$) overlap region spreads laterally into both sides of the channel as the channel length gets shorter. This makes the relative effective channel length ($L_{eff}/L = 1-(L_{SS}+L_{SD})/L$)) shorter and smaller parasitic $R_S$ and $R_D$ in TFTs with decreasing the channel length.

Therefore, the $W$- and $L$-dependent $R_S$ and $R_D$ can be modeled as

$$R_S\,(R_D) = R_{SO}\,(R_{DO}) + R_{S,ext}\,(R_{D,ext}),\ R_{S,ext}\,(R_{D,ext}) = \frac{r_{par}}{L_{SS}\,(L_{SD})\,W} \tag{10}$$

with $R_{SO}$ ($R_{DO}$) [$\Omega$] as the $L$-independent parasitic source (drain) contact resistance, $R_{S,ext}$ ($R_{D,ext}$) [$\Omega$] as the extrinsic parasitic resistance, $r_{par}$ [$\Omega\cdot$cm$^2$] as the parasitic resistivity, and $L_{SS}$ ($L_{SD}$) as the current spreading length as schematically shown in Fig. 3(c). We expect that the relative contribution $L_{SS}/L$ ($L_{SD}/L$) increases with the scaling down of the channel length resulting a reduced parasitic $R_S$ and $R_D$ in TFTs with short channel lengths. As shown in Fig. 3(b), $W$-normalized parasitic resistances ($R_S\cdot W$ and $R_D\cdot W$) show constant over the gate width confirming consistency of the model and extracted result.

## IV. CONCLUSION

We proposed a dual-sweep combinational transconductance technique based on the degradation of the transconductance due to the parasitic resistance at the source terminal during the I-V characterization for separate extraction of parasitic $R_S$ and $R_D$ in insulated gate TFTs. By applying the proposed extraction technique to a-IGZO TFTs with $W/L = 30$ $\mu$m/10 $\mu$m, the parasitic resistances are obtained to be $R_S = 17.38$ [k$\Omega$] and $R_D = 15.44$ [k$\Omega$]. A model for the $W$- and $L$-dependence of the parasitic resistance in a-IGZO TFTs was provided and analyzed.

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