Investigation on mechanism for instability under drain current stress in amorphous Si–In–Zn–O thin-film transistors

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The mechanism for instability against positive bias stress (PBS) in amorphous Si–In–Zn–O (SIZO) thin-film transistors has been investigated by analyzing the subgap density of states (DOSs), which was extracted from multi-frequency method using direct capacitance–voltage measurements. It was found that DOSs including shallow tail states and deep trap states are constant in density as PBS time increases. It indicates that the bulk traps in the SIZO channel layer and the channel/dielectric interfacial traps are not created during the PBS duration. Therefore, the instability against PBS in SIZO thin-film transistors is attributed to the charge trapping by the acceptor-like DOSs.

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1. Introduction

Highly transparent amorphous oxide semiconductor (TAOS) based thin-film transistors (TFTs) have attracted great interest in the applications including future displays, optoelectronics and electronics [1,2]. Especially, the TAOSs, such as Ga–In–Zn–O (GIZO) [3], Hf–In–Zn–O (HIZO) [4], Zn–Sn–O [5], Si–In–Zn–O (SIZO) [6], and so on have been anticipated to resolve the innate drawbacks of current Si based TFTs including the poor carrier mobility of amorphous Si TFTs and the non-uniformity in electrical performances of low temperature processed poly-Si TFTs [7]. The TAOS based TFTs provide better uniformities and electrical properties compared with those of the poly-Si based ones, since crystallites that make the properties of TFTs inhomogeneous are not included in the TAOSs and a high electron mobility can be achieved even in amorphous state due to high symmetry of s-orbitals of heavy metal ions [8]. In order to improve the stability under positive/negative bias stress, illumination stress, and temperature stress, the fundamental mechanisms for the threshold voltage shift have been intensively investigated for GIZO–[8] and HIZO–TFTs [9]. Recently, it was reported that a high field effect mobility and good stability were achieved by a tiny amount of Si incorporated In–Zn–O (SIZO) TFTs fabricated at very low process temperature of 150 °C [10]. The post annealing process with low temperature will facilitate for SIZO semiconductor to be applied to flexible display. Considering 20% change in the luminance owing to improvement of stability in SIZO–TFTs. In earlier works, we reported that the instability under positive bias stress (PBS) of the SIZO–TFTs is attributed to the charge trapping in semiconductor bulk and at the semiconductor/dielectric interface by extracting the density of states in TFTs using the SIZO layer [10], remaining unproven for possibility of defect creation during the PBS in the SIZO–TFTs. Thus, it should be proved first that the defect creation model is not a dominant mechanism in the SIZO–TFTs.

In this paper, the mechanism for instability of 1 wt.% Si incorporated SIZO–TFT under PBS has been investigated by analyzing the subgap density of states (DOSs) extracted directly from multi-frequency method (MFM) using capacitance–voltage (C–V) characteristics [12]. The variation of subgap DOSs within energy range from conduction band edge (E_C) to 1.6 eV below the E_C was not observed during PBS tests. Therefore, it is no doubt that the defect creation in active channel layer bulk and at the channel/dielectric interface is not responsible for the positive V_U shift under the PBS in the SIZO–TFT.

2. Experimental details

Direct current sputtering method was used to deposit 150 nm thick Mo gate electrode on glass substrate at room temperature, and then 200 nm thick SiN_x as gate insulator was grown at 330 °C by plasma enhanced chemical vapor deposition. Amorphous 1 wt.% Si incorporated SIZO (In_2O_3:ZnO = 3:1) active layer with 30 nm in thickness was prepared by the radio frequency magnetron sputtering at room temperature. The SIZO active layer and source/drain (S/D) electrodes were well defined by the conventional photolithography and wet
process, in which the SIZO films were etched by 99% diluted hydrochloric acid and the S/D electrodes were patterned by lift-off process by acetone. Ti/Au (10 nm/60 nm) as source/drain electrodes were deposited by electron beam evaporation and thermal evaporation method, respectively. The well-defined channel length and width of the SIZO–TFTs were 200 μm and 100 μm, respectively. The SIZO–TFTs were annealed at 150 °C for 1 h in thermal furnace with N₂ ambience. All the transfer curves and stability tests were evaluated by means of a semiconductor parameter analyzer (HP 4145B) probe system in a dark and vacuum state of <2.67 Pa. The bias for the stress tests was kept at a gate voltage of 20 V and drain to source voltage of 10.1 V for 1500 s at room temperature. The C–V measurements to extract the DOSs in SIZO–TFTs were carried out by using precision LCR meter (Agilent 4284A).

3. Results and discussion

Fig. 1(a) shows the evolution of transfer curves obtained at drain to source voltage (VDS) of 0.1 V from amorphous SIZO–TFT under PBS with increasing stress time. The PBS was kept at gate to source voltage (VGS) of 20 V and VDS = 10.1 V during 1500 s. Transfer curves were shifted toward positive direction with increasing stress time. As a result, the threshold voltage (VTH) shift for the SIZO–TFT was about 5.7 V during 1500 s. The VTH values were extracted in IDS stress time were shown in Fig. 1(c) and (d). The SS and FE values were almost not changed with increasing stress duration. It has been reported that the positive shift in VTH during PBS is explained using a simple charge trapping or defect creation model [14–16]. In the case of SIZO–TFT, the SS values were not significantly changed during PBS duration. This result suggests that charge trapping in gate dielectric, and/or in oxide semiconductor bulk, and/or at the channel/dielectric interface is more dominant mechanism than the creation of defects in the SIZO–TFTs [3,14].

Fig. 2 illustrates the hysteresis window as a function of PBS stress time of SIZO–TFT. The transfer curves were also obtained at VDS = 0.1 V. The VTH was shifted to a further positive direction in the hysteresis loop as stress time increases. It is suggested that the positive VTH shift by the hysteresis is attributed to trapping of negatively charged carriers at the channel/dielectric interface or injection into the dielectric from SIZO channels [14]. The VTH shift by the hysteresis was decreased with increasing stress time, indicating that no defects were created at the channel/dielectric interface. If the defects are created by the PBS, the amount of VTH shift by the hysteresis should increase or be constant with increasing stress time, since the traps created at the interface by the PBS are immediately filled with free electrons. Therefore, it is believed that the reduction of VTH shift by the hysteresis with increasing PBS time is because the traps are not created at the interface. The inset in Fig. 2 shows the hysteresis window of transfer curves measured with the stress time.

Fig. 3 illustrates C–V curves of SIZO–TFT with different frequency (f) level as a function of PBS duration. The decrease in magnitude of the gate capacitance with increasing f within the frequency range between 5 kHz and 100 kHz was observed for all of C–V curves in Fig. 3. This observed result is due to the f dependence of capture–emission events through the interface and/or channel bulk trap as

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**Fig. 1.** (a) The evolution of transfer curves, and (b) the square root plots of IDS with PBS duration, (c) SS and FE, and (d) VTH and Ion-off ratio as a function of stress time.
well as parasitic source/drain resistance related the supplying speed of the charging current through source/drain electrodes [12]. At a given stress time, the sensitivity to the f of the obtained C–V curves is declined with increasing f, resulting in the decrease of the gate capacitance at a VGS. In other words, the carriers have a sufficient time to be captured at the localized traps and be emitted from the traps at low f. Thus, the gate capacitance measured at lower f is larger than that obtained at higher f. The SIZO–TFT clearly showed the dependency of the gate capacitance as a function of voltage on f.

Fig. 4 shows the evolutions of C–V curves for SIZO–TFT with increasing PBS duration at a fixed frequency of 5 kHz. The C–V curves were shifted toward positive direction, indicating the decrease

![Fig. 2. The hysteresis window by return sweep with increasing PBS time for SIZO–TFT. The inset shows the evolution of transfer curves.](image1)

![Fig. 4. The variation of C–V curves for SIZO–TFT with increasing PBS duration at a fixed frequency of 5 kHz.](image2)

![Fig. 3. The evolution of C–V curves of SIZO–TFT under PBS with different f. (a) 0 s, (b) 100, (c) 500 s and (d) 1500 s in stress time, respectively.](image3)
of free carriers in SIZO–TFT as stress time increases. The $V_{GS}$ starting to change from depletion mode to accumulation mode in $C-V$ curves, when $V_{GS}$ is swept positively, becomes larger with decreasing free carriers in TFTs, resulting in the positive shift in $C-V$ curve. Therefore, the observation from transfer characteristics is well matched with that from $C-V$ analysis.

Based on the gate capacitance as a function of $V_{GS}$ obtained from $C-V$ measurements, the DOSs with different PBS time were extracted from MFM method in order to investigate the subgap tail states and deep states in SIZO–TFTs. Fig. 5 shows the subgap DOSs in SIZO–TFTs with different PBS duration. The DOSs obtained from the MFM technique include trap states in channel bulk and/or at channel/dielectric interface [12]. Interestingly, the number of DOSs within the energy range from the $E_c$ to ~1.6 eV below the $E_c$ was not changed as stress time increases. This observation indicates that acceptor-like tail states and deep trap states in SIZO channel bulk and/or at the channel/dielectric interface were not created during PBS tests. Therefore, the charge trapping mechanism under PBS becomes clearly confirmed from the DOS analysis in SIZO–TFT.

4. Conclusions

In summary, it was found by directly extracting the DOSs in SIZO–TFTs during PBS tests that the $V_{TH}$ shift under the PBS tests is originated by charge trapping in SIZO channel bulk and/or at the channel/dielectric interface, not defect creation. Also, this fact was confirmed by the constant SS value and reduced hysteresis loop as PBS time increases. It is strongly suggested that electron trapping by acceptor-like DOSs within the band gap causes the instability under PBS in SIZO–TFT. To improve the stability of SIZO–TFT under the PBS, suppressing the acceptor-like tail states and deep trap states in SIZO–TFT is a crucial key factor.

References