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# Numerical study of read scheme in one-selector one-resistor crossbar array

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ABSTRACT

A comprehensive numerical circuit analysis of read schemes of a one selector–one resistance change memory (1S1R) crossbar array is carried out. Three schemes—the ground, $V/2$, and $V/3$ schemes—are compared with each other in terms of sensing margin and power consumption. Without the aid of a complex analytical approach or SPICE-based simulation, a simple numerical iteration method is developed to simulate entire current flows and node voltages within a crossbar array. Understanding such phenomena is essential in successfully evaluating the electrical specifications of selectors for suppressing intrinsic drawbacks of crossbar arrays, such as sneaky current paths and series line resistance problems. This method provides a quantitative tool for the accurate analysis of crossbar arrays and provides guidelines for developing an optimal read scheme, array configuration, and selector device specifications.



## 1. Introduction

Resistive switching devices fabricated from various oxides and chalcogenide materials—generally termed resistance-change memories (RRAMs)—have attracted considerable attention for their potential use in developing next generation non-volatile memories [1–3]. As a potential array configuration for RRAM that may enable low-cost product fabrication, the crossbar architecture has shown promise owing to its simple structure and high device density. In a crossbar array, RRAMs can be integrated at the junctions of orthogonal access lines to form simple lattices that may enable n-layer stacking [4] or the vertical fabrication of 3-D crossbar arrays [5].

However, the merits of crossbar array architectures can only be realized when selector devices are properly incorporated, as the presence of many sneaky current paths can adversely affect the ability to sense the state of selected memory cells. Owing to the increasing number of sneaky current paths, the role of the selector device becomes more important as the array density increases. In particular, device selectivity (defined as the ratio of the currents at full-read ($V_a$) and half-read voltage ($V_a/2$)) is crucial to determining the sensing margin of a selected cell during a crossbar array read operation. Accordingly, accurate estimates of required device selectivity for various array sizes are essential for the successful completion of crossbar array read operations.

Although several quantitative analyses of crossbar array architecture read schemes have been recently conducted [6–11], most of these have ignored series line resistance for simplicity. However, voltage drop in highly scaled devices and arrays often causes the series line resistance to become a serious or even dominant factor in array operation. Another problem with many of the previous studies is that they were conducted using too simplified of an analytical approach in which only portions of the sneak current path were considered [8], or, conversely, that they used overly analytical methods involving matrix algebra [11]. Moreover, although SPICE-based circuit simulation can produce accurate estimates [9,10], it requires high computational power for the simulation of high-density crossbar arrays.

In this study, a comprehensive numerical circuit analysis that incorporates series line resistance effects is carried out in order to optimize the read scheme of a one selector–one resistance change memory (1S1R) crossbar array. Without using a complex analytical approach or SPICE-based simulation, a simple numerical iteration method for simulating entire current flows and node voltages within a crossbar array is developed; this provides information on which array sizes are feasible with respect to the sensing margin and required selectivity of selector devices. In addition, three different read schemes—the ground, $V/2$, and $V/3$ schemes—are compared in terms of their respective sensing margins and power consumption. Ultimately, this study provides a means for creating guidelines in developing optimal read schemes, array configurations, and selector device specifications.

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## 2. Experimental details: calculation methodology

Fig. 1 shows a schematic diagram of the 1S1R crossbar array structure for which the calculations in this study were carried out. In this architecture, the resistance state of a selected cell is sensed by applying a read voltage $V_a$ to the selected word line (denoted as WL($M$)), while the current flowing through the selected cell is detected using a current-sensing-type sense amplifier connected to the end of the selected bit line (denoted by BL ($N$)). The end of the sense amplifier is assumed to be connected to the ground potential (denoted by GND in Fig. 1).

Ideally, the output sensing current is simply determined by the relationship $I_{sensing} = V_a/R_{selected\text{-}cell}$. However, owing to the presence of sneaky current paths through unselected cells, the output sensing current also contains noisy leakage currents. The problems associated with sneaky current paths are most severe when all of the unselected cells are in a low resistance state. Aside from sneaky current paths, voltage drop caused by series line resistance also affects the output sensing current; this voltage drop effect is most critical when the selected cell is located furthest from the read voltage source and ground potential, as is shown in Fig. 1 (in which the lower-right corner is the furthest from the read voltage and ground source). Because the total output sensing current is detected by the sense amplifier connected to the end of the selected bit line, it represents the sum of the ideal sensing current and unwanted noise components.

To suppress sneaky-path current flow, selector devices can be co-integrated with the RRAM at each cross point. As shown in Fig. 2a, three read bias schemes are proposed: the ground, $V/2$, and $V/3$ schemes. In the ground scheme, all unselected word lines and bit lines are grounded, and as a result, most of the leakage current results from fully selected cells in selected word line. In the $V/2$ scheme, all of the unselected word and bit lines are biased at one-half of the read voltage ($V_a/2$), and most of the leakage current originates from the half-selected cells in the selected word line and the selected bit line. Finally, in the $V/3$ scheme, all unselected word lines are biased at one-third of the read voltage ($V_a/3$), while all unselected bit lines are biased at two-thirds of the read voltage ($2V_a/3$). In the $V/3$ case, leakage current is generated from all of the one-third selected cells in all of the word lines and all of the bit lines, as shown in Fig. 2a.

To simulate the dependence of output sensing current on the selection of the read bias scheme, specifications of the selector device, array size, patterns of data stored in the memory array, and total current flows in the crossbar array should be calculated. Fortunately, the steady-state electrical characteristics of a crossbar array can be completely described by a set of unknown voltage variables, i.e., the voltages at every array junction. As shown in Fig. 2b, there are two unknown voltage variables at every junction: one on the WL plane ($V_{WL}(i, j)$), and the other on the BL plane ($V_{BL}(i, j)$), where $1 \leqslant i \leqslant M$ and $1 \leqslant j \leqslant N$. Consequently, all of the current flows in the crossbar array can be derived if the $2 \times M \times N$ unknown voltage variables (i.e., all values of $V_{WL}(i, j) + V_{BL}(i, j)$) can be calculated. Based on Kirchhoff's Law, which defines the current continuity at every junction point, $2 \times M \times N$ simultaneous equations are available to solve for the unknown voltage variables using a simple numerical iteration method, i.e., the Gauss–Seidel method. Details of this solution method and its simulation code are provided in the Supplementary information.

All the simulation parameters used in this study were selected from reported data on state-of-the-art RRAM and selector devices [13] and an assumed 30-nm technology node and are listed in Fig. 3a. The stored data pattern described by $R(i, j)$ in the $M \times N$ array represents either $R_{on}$, the low resistance state (LRS), or $R_{off}$, the high resistance state (HRS), the two meta-stable resistance states of the RRAM device at read voltage $V_a = 2$ V, as shown in Fig. 3b. The on–off ratio ($r = R_{off}/R_{on}$) of the RRAM device is fixed to 10 in the subsequent discussion. Three resistance states are defined for the selector devices used in the simulation: $R_0$, $R_{half}$ (or $R_{third}$), and $R_{full}$. The state $R_0$ is determined by the leakage current level at 0 V; in other words, the resistance of the selector device is $R_0$ when the selector is connected to the unselected cell so that its potential difference with the selector is 0 V. The state $R_{half}$ is defined by the current at one-half of the read voltage (i.e., in the $V/2$ scheme) at which the resistance of the selector device connected to the half-selected cell is $R_{half}$. Similarly, $R_{third}$ is determined by the current at one-thirds of the read voltage (in the $V/3$ scheme). The selectivity of the selector device ($k$) is variously

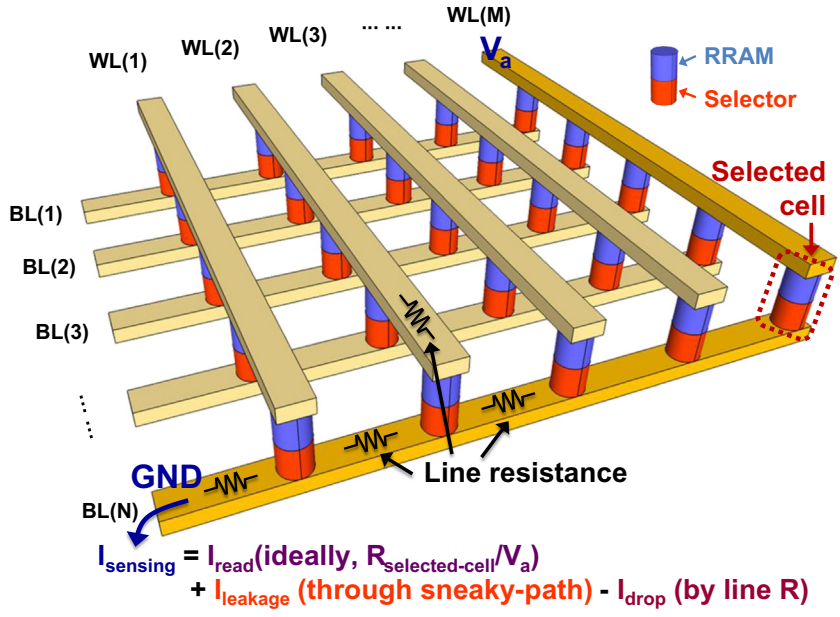


**Fig. 1.** Schematic diagram of crossbar array structure with WLs (vertical line) and BLs (horizontal lines). $R(M, N)$ at the lower-right corner is the selected cell. The output sensing current detected by the sense amplifier is the sum of the ideal sensing current and unwanted noise components.

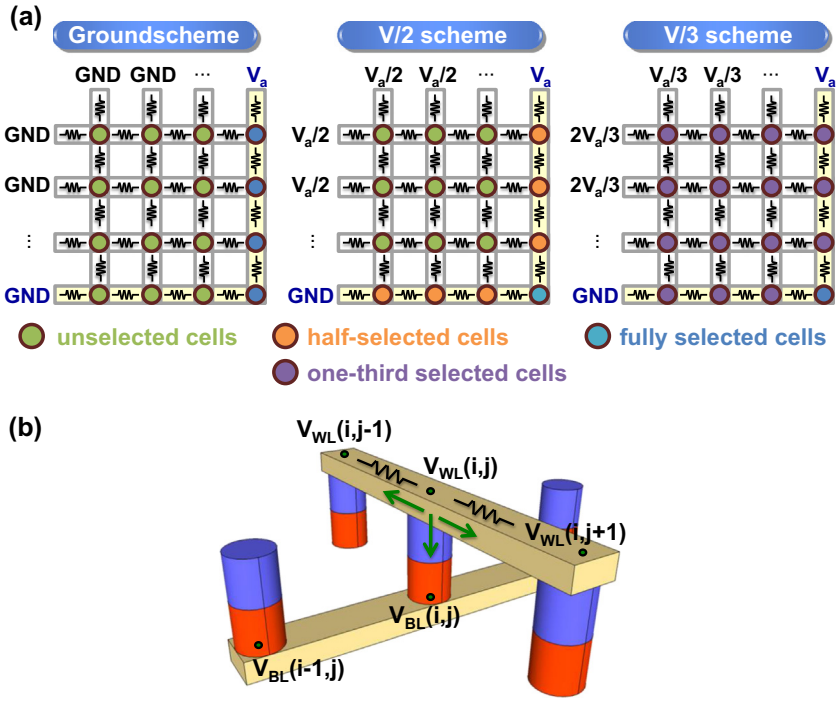


**Fig. 2.** (a) Three read bias schemes: ground scheme; *V*/2 scheme; and *V*/3 scheme. (b) Kirchhoff's law at every junction in the crossbar array.

| (a) | Parameters (assume 30×30 nm²) | Values |
|---|---|---|
| | Array size | M × N |
| RRAM | Resistance in LRS ($R_{on}$) | 2.5 × $10^4$ Ω [3] |
| RRAM | On-off ratio ($R_{off}/R_{on}$) | $r$ = 10 |
| RRAM | Resistance in HRS ($R_{off}$) | $R_{on}$ × $r$ |
| Selector | Resistance at V = 0 (unselected, $R_0$) | 4.4 × $10^{11}$ Ω [13] |
| Selector | Resistance at V = $V_a$ (fully selected, $R_{full}$) $J_{max}$ = 10 MA/cm² | 2.2 × $10^4$ Ω [13] |
| Selector | Selectivity | $k$ |
| Selector | Resistance at V = $V_a$/2 or $V_a$/3 ($R_{half}$ or $R_{third}$) | $R_{full}$ × $k$ |
| | Selected word line voltage ($V_a$) | 2.0 V |
| | Selected bit line voltage | 0 V |
| | Interconnect resistance ($R_L$) | 2.4 Ω [14] |

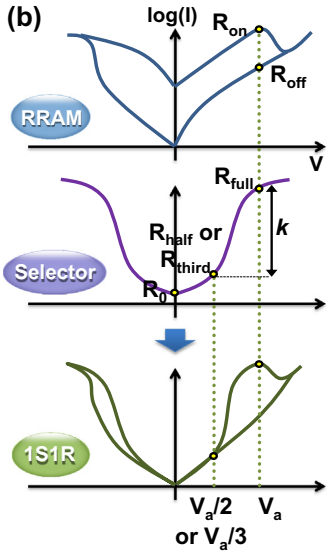


**Fig. 3.** (a) Parameters for simulation. (b) Schematics of *I*–*V* curve for 1S1R system.

defined as the ratio of the current at the full read voltage ($V_a$) to that at either half- or one-third read voltage ($V_a/2$ or $V_a/3$, respectively). Finally, $R_{full}$ is defined by the current level at $V_a$ at which the available maximum current density is 10 MA/cm$^2$. To enable an accurate simulation of the series line resistance between two adjacent junctions, a series line resistance effect based on the resistivity of a Cu line with an assumed line aspect ratio of 1 (2.4 Ω) is also included [14].

## 3. Calculation results

### 3.1. Optimal read bias scheme

Figs. 4a and b show bitmap images of the calculated leakage current in a 50 × 50 bits crossbar array with random data patterns, without and with a selector device ($k = 10^2$), respectively. While previous reports investigated only specific data patterns due to the difficulties of simulation with random data patterns from analytical approaches or SPICE-based simulations, the numerical method proposed in this study has no difficulty in simulating random data patterns [9–12]. It can be clearly seen in Fig. 4a that a large amount of leakage current through sneaky current paths is seen in the absence of a selector device. By contrast, Fig. 4b shows that leakage current can be effectively suppressed with the aid of a selector device. It is also apparent from Fig. 4b that in the ground scheme, most leakage current originates from the fully selected cells in the selected word line, while in the *V*/2 scheme, it mostly originates from the half-selected cells in the selected word line and the selected bit line. In the *V*/3 scheme, by contrast, leakage currents are generated by all of the one-third selected cells in all

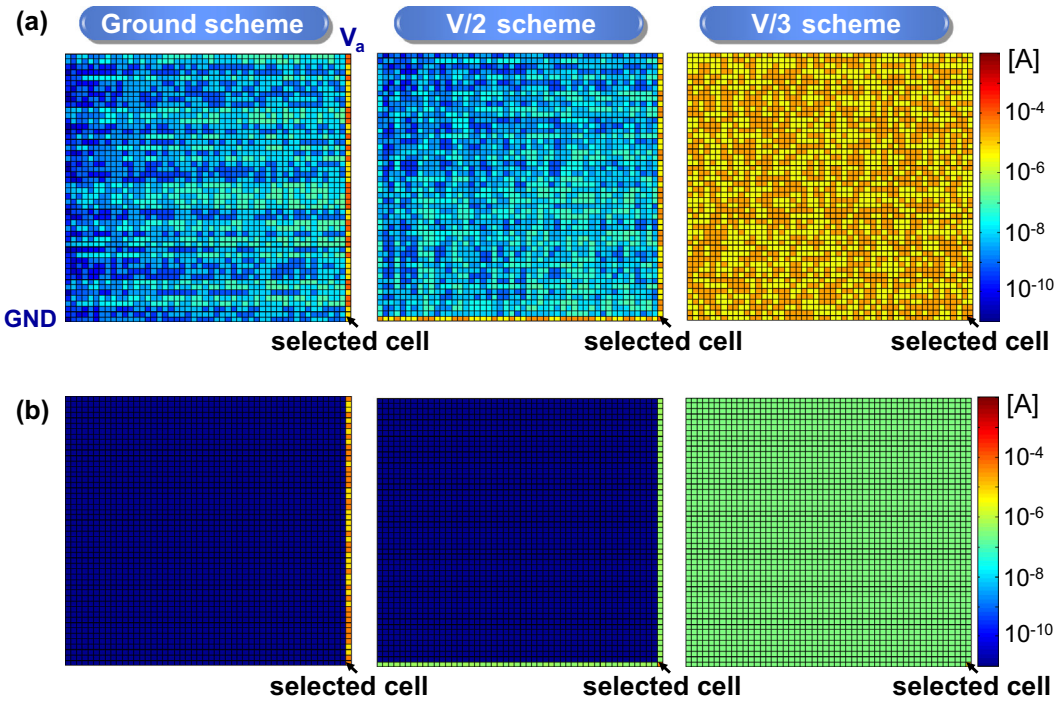


**Fig. 4.** Bitmap of leakage current in 50 × 50 bit array with random data patterns (a) without selector device and (b) with selector device of selectivity $k = 10^2$.

of the word lines and all of the bit lines. These respective characteristics lead to differences in terms of sensing margin and power consumption.

In order to compare the three read bias schemes on equal terms, the following discussion is based entirely on the worst-case scenario. As noted above, the location of the selected cell will strongly influence the read operation, causing the sensing margin and read voltage drop of the selected cell to differ depending by cell location. Thus, the worst-case scenario of cell selection during the read operation is that in which the cell is located at the furthest corner from the word- and bit-line sources, as shown in Fig. 5a; in this case, the voltage drop caused by series line resistance is largest. Furthermore, in the worst-case scenario, all of the unselected cells are in the LRS, and thus, the leakage current through sneaky paths is also maximized, which leads to a degradation of the sensing margin caused by increases in the noise current component.

Fig. 5b shows simulated sensing margins for $V/2$ schemes associated with differing array sizes and device selectivity. In this case, the sensing margin is defined by the ratio of the values of $I_{sensing}$ for the HRS and LRS of a selected cell normalized by the on–off ratio of the RRAM device. The sensing margin decreases as the array size increases and as the selectivity decreases because these changes lead to the inclusion of more noise components from sneaky current. A comparison of sensing margins among the different read bias schemes is shown in Fig. 6a. It can be seen that the ground scheme shows the highest sensing margin of the three and that the $V/2$ and $V/3$ schemes incur severe degradation as the array size is increased. The superior performance of the ground scheme arises from the fact that dominant leakage currents originate only from the selected word line and are drained to the unselected bit lines, as shown in Fig. 4b; consequently, relatively small noise components are added to the selected bit lines. On the other hand, because the leakage currents in the $V/2$ and $V/3$ schemes are generated from half- and one-third selected cells, respectively, on the selected bit line, the sensing margins are more degraded by noise currents injected into the selected bit line. It should be noted, however, that the sensing margins of the three schemes are nearly equal at sufficiently high device selectivity, e.g., $k = 10^4$. As shown in Fig. 6b, the difference in sensing margins among the three schemes is negligible when the selectivity of the selector device is high enough to suppress leakage current.

On the other hand, power consumption shows a tradeoff with respect to the sensing margin. Fig. 7a shows the calculated power consumptions through the selected word line. Here, the ground scheme shows the highest power consumption. The fact that the ground scheme consumes more power than the $V/2$ and $V/3$ schemes implies that a higher level of current needs to be supplied to the selected word line in the former case. However, supplemental high current levels may not be available in a scaled metal line owing to the electromigration effect, a limitation that should be taken into account when the ground scheme is used. Fig. 7b shows the calculated power consumption by all word lines; it is apparent from this that although its power consumption can be suppressed by increasing the selectivity of the selector device, the $V/2$ scheme always has a lower power consumption than the other schemes.

These calculation results provide guidelines for developing an appropriate read bias scheme. Because there is a trade-off between sensing margin and power consumption, an optimal read scheme needs to be based on the specifications of the selector devices. If the selectivity of the selector device is not high, e.g., $k = 10^2$, a ground scheme is recommended for improving the sensing margin. However, if a high-selectivity selector device is available, e.g., $k = 10^4$, the $V/2$ scheme is most appropriate in terms of both the sensing margin and the power consumption.

### 3.2. Specifications of selector devices

Recently, a tremendous amount of technological effort has been devoted to developing improved selector devices. It is generally believed that increasing the maximum on-current density ($J_{max}$) and selectivity ($k$) of a selector device will always lead to improved crossbar array operation. Fig. 8a shows a schematic of current–voltage ($I$–$V$) characteristics for two different selector devices with identical selectivity but different $J_{max}$. All else being equal, a

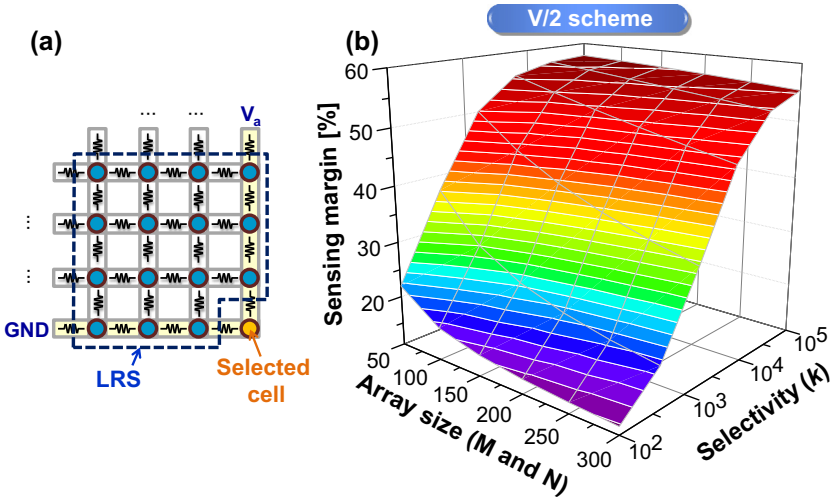


**Fig. 5.** (a) Schematics of worst-case scenario during read operation. (b) Calculated sensing margin with regard to differing array size and selectivity of selector device in *V*/2 scheme.

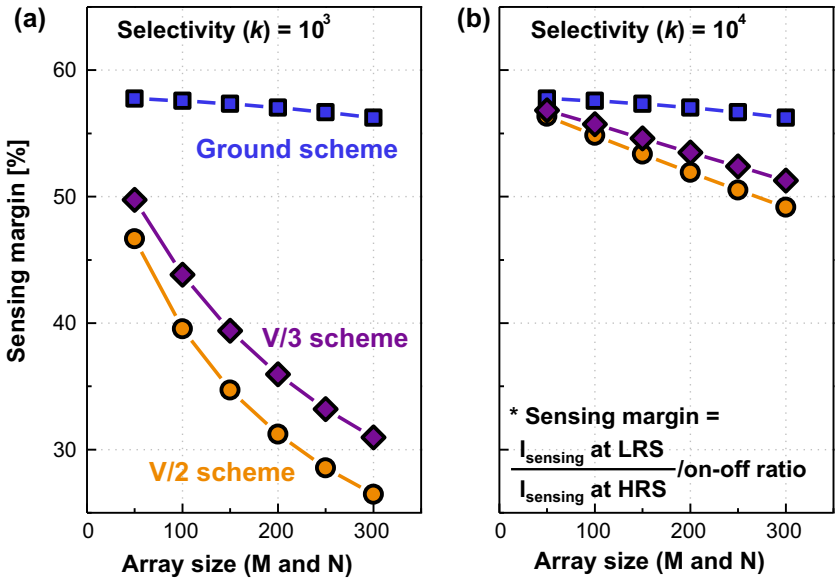


**Fig. 6.** Sensing margin comparison of three read bias schemes with respect to array size when (a) selectivity of selector device is $k = 10^3$ and (b) $k = 10^4$.

selector with a higher $J_{max}$ is usually considered to be most suitable for use in a crossbar array; however, the surprising calculational result is that a higher $J_{max}$ does not always guarantee an improved sensing margin. Fig. 8b shows the calculated sensing margins for different values of $J_{max}$ in the three read schemes discussed here. As can be seen, for a certain selectivity value ($k$), there exists an optimal value of $J_{max}$ in terms of the sensing margin, and increasing $J_{max}$ beyond this optimal point leads to a decrease in the sensing margin. The reason for this counter-intuitive dependence is that the leakage current from the half-selected cells also increases with $J_{max}$; in other words, at a constant value of $k$ an increase in $J_{max}$ leads to an increase in leakage current through the half-selected cells, and thus to an increase in $R_{half}$. This effect causes the noticeable result seen in Fig. 8b in which a selector with high values of $J_{max}$ and $k$ (450 MA/cm$^2$, $k = 10^4$, depicted by a blue star) does not offer any benefit in terms of sensing margin over a selector with low $J_{max}$ and $k$ (10 MA/cm$^2$, $k = 10^3$, depicted by a red star). From these results, it can be concluded that higher values of $J_{max}$ and $k$ cannot guarantee improved sensing margins, and instead, optimal points should be determined in order to obtain appropriate sensing margins without blindly improving the performance of the selector device.

### 3.3. Array configuration

In all previous studies, only square-shaped arrays have been discussed. However, as mentioned earlier, the voltage drop caused by series line resistance dictates that the location of the selected cell affects the sensing margin. This voltage drop effect is more critical at the selected word line than at the selected bit line because the read voltage is applied to the former; therefore, shortening the selected word line length should suppress the voltage drop effect. Fig. 9a shows three different array configurations ($M \times N$) with the same 10 kbit array density. The $50 \times 200$ configuration has the longest word line length, while the $200 \times 50$ configuration has the shortest word line length. As can be seen in Fig. 9b and c, a higher sensing margin can be achieved without increasing power consumption by shortening the word line length.

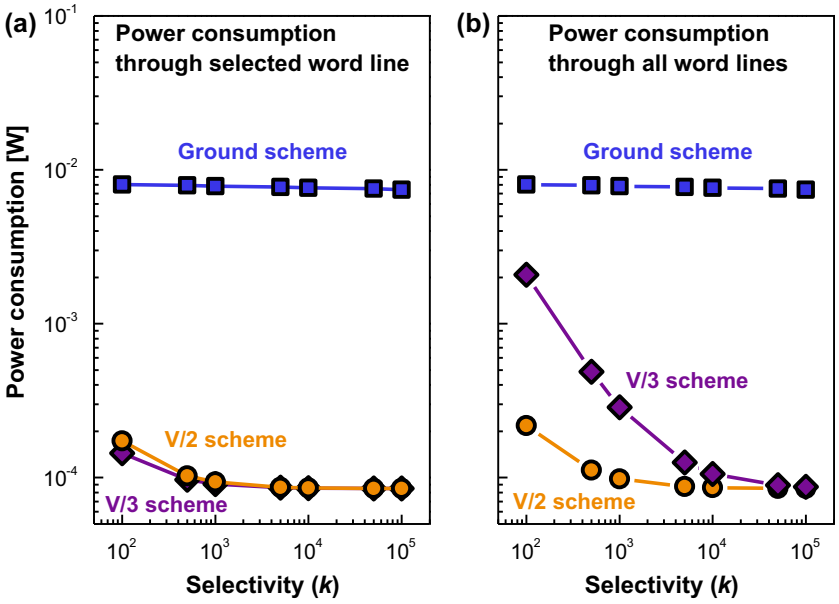


**Fig. 7.** Power consumption comparison among three read bias scheme as a function of selectivity of selector device for $10^2 \times 10^2$ (10 kbits) array. In the worst-case scenario, all of the cells are in the LRS. (a) Power consumption through selected word line only, and (b) power consumption through all word lines.

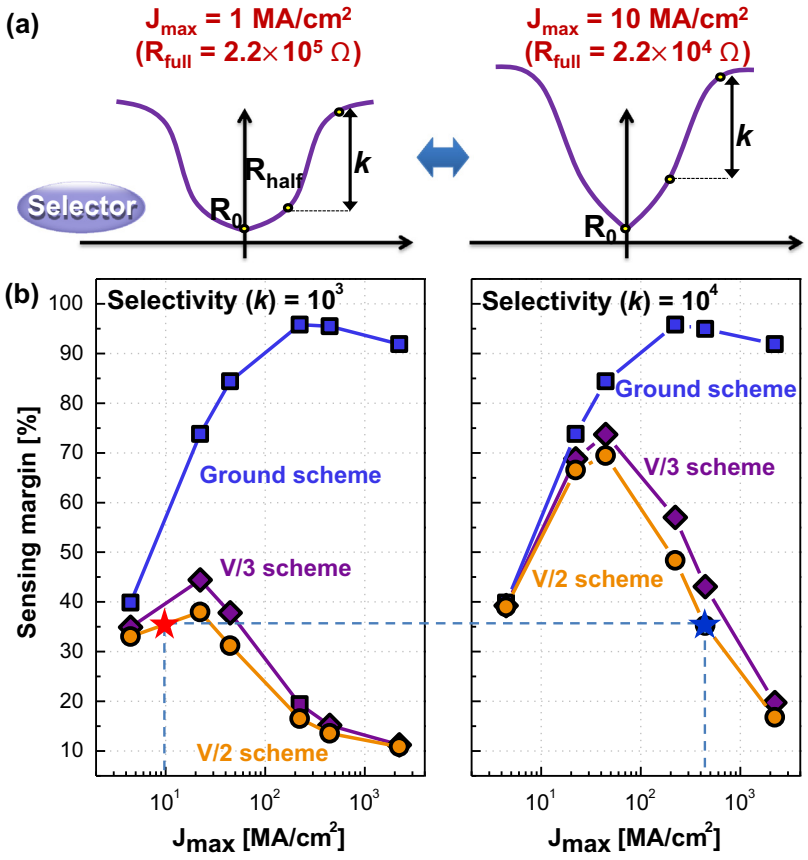


**Fig. 8.** (a) Schematic *I–V* curves for selector device with varying maximum on-current density ($J_{max}$) at a constant selectivity ($k$). (b) Calculated sensing margin with respect to $J_{max}$ for three read bias schemes. The array size is 10 kbits.

Although the peripheral circuitry attached to the word and bit lines, e.g., the sense amplifier, power supply unit, and decoders, should be taken into account in optimizing the array configuration, this simulation result still provides insights into possible sensing margin improvements that may be applicable in developing 3-D stacked crossbar array configurations.

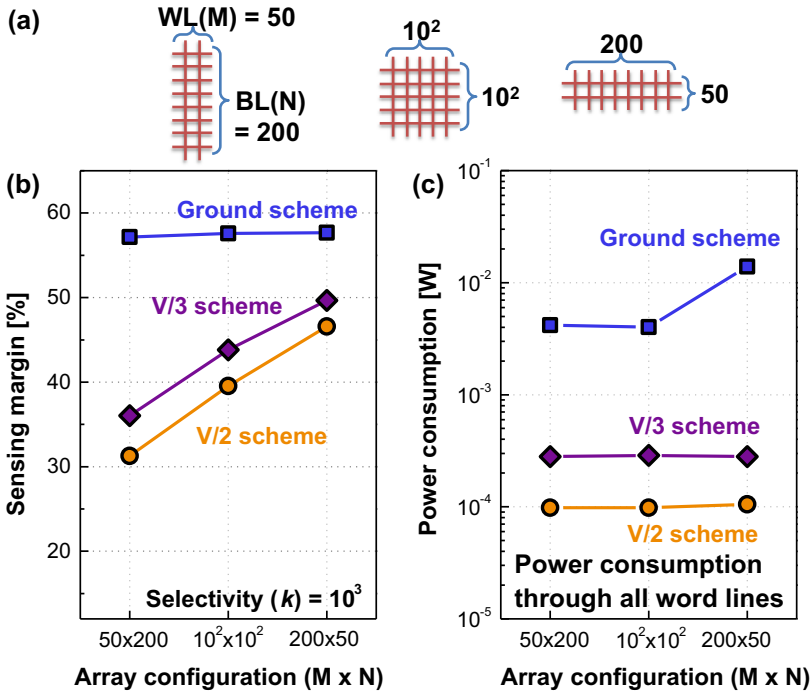


**Fig. 9.** (a) Schematics of differing array configurations for 10 kbit array. Calculated (a) sensing margins and (b) power consumptions.

## 4. Conclusions

In this study, an analysis of read schemes in a one selector–one resistance change memory (1S1R) crossbar array with respect to sensing margin and power consumption was conducted using a novel numerical circuit simulation method. It was found that as the optimal read bias scheme depended on the selectivity of the selector device, the specifications of such devices must be taken into account in optimization. In addition, higher selector device performance cannot guarantee improved sensing margins; instead, optimal points of maximum on-current density and selectivity should be determined instead of blindly improving the selector device. Simulation results for various array configurations provide insight into potential avenues of sensing margin improvement that may be applicable in developing 3-D stacked crossbar array configurations. The simulation method presented in this study provides guidelines for crossbar array design and read bias scheme optimization with respect to sensing margin and power consumption.

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## Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.sse.2015.08.001.

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