

Sub-bandgap photonic gated-diode method for extracting distributions of interface states in MOSFETs

S.S. Chi, H.T. Kim, M.S. Kim, T.E. Kim, H.T. Shin, H.S. Park, K.H. Kim, K.S. Kim, I.C. Nam, D.J. Kim, K.S. Min, D.W. Kang and D.M. Kim

A new sub-bandgap photonic gated-diode method is proposed to extract the energy-dependent and spatial distributions of traps at the SiO₂/Si interface in MOSFETs. For the photonic current–voltage (*I*–*V*) characterisation of MOSFETs, an optical source with a sub-bandgap photon energy less than the silicon bandgap ($E_{ph} = 0.95 \text{ eV} < E_g = 1.12 \text{ eV}$) is employed for the characterisation of interface states (D_{it}) distributed in the photo-responsive energy band ($E_C - 0.95 \leq E_{it} \leq E_C$) in MOS systems with a polysilicon gate.

Introduction: Gate dielectrics in deep sub-0.1 μm MOSFETs are subjected to a very high electric field during circuit operation, therefore ultra-thin gate dielectrics need to have very high dielectric strength and good interface properties [1]. The charge-pumping method is known to be a good tool for quantitative characterisation of the energy-dependent [2] and lateral distributions of interface states in MOS systems [3–6]. A photonic method with capacitance–voltage (*C*–*V*) characteristics is reported for the characterisation of interface states in MOS systems [7].

A novel sub-bandgap photonic gated-diode method (PGDM) for the extraction of interface traps in MOSFETs is reported. This nondestructive PGDM uses the sub-bandgap ($E_{ph} < E_g$) photonic *I*–*V* characteristics with the photon energy less than the silicon bandgap energy. Based on the PGDM combining the interface state-induced-current (I_{it}) in MOSFETs (in accumulation, depletion and inversion mode of the surface), the energy-dependent and spatial distributions of traps at the SiO₂/Si interface are extracted.

Energy-dependent profiling of interface states: In the experimental characterisation, a HP 4145B parameter analyser and ILX 7200 are used to monitor the optically-induced gated-diode current in fat MOSFETs ($W/L = 40 \mu\text{m}/40 \mu\text{m}$, $V_T \sim 0.6 \text{ V}$) under sub-bandgap optical excitation. N-MOSFETs are used as a test structure for this work. Physical mechanism involved in the PGDM is schematically shown in Fig. 1 inset.

We assume that only optically excited electrons from the traps at the SiO₂/Si heterojunction interface contribute to the surface generation current under sub-bandgap optical excitation. We measured gated diode currents [3] under dark and sub-bandgap optical excitation of MOSFETs and the interface-induced current I_{it} under optical illumination is shown in Fig. 1. The trap-induced current I_{it} can be analytically described as

$$I_{it} \equiv I_{Op} - I_{Dk} = A_g \sum_{\Delta E} J_{it} \quad (1)$$

where I_{Dk} and I_{Op} are the gated-diode current under dark and sub-bandgap optical excitation, respectively. Therefore, the trap-induced current density J_{it} , can be written as

$$J_{it} = qn_i s_o = qn_i \left(\frac{\sigma_s v_{th} N_{it}}{2} \right) \quad (2)$$

where n_i is the intrinsic carrier concentration in silicon, A_g is the gate area, s_o is the surface recombination velocity, σ_s is the effective capture cross-section, v_{th} is the thermal velocity, and N_{it} is the interface state density.

Modulating the surface potential with applied gate voltage, we obtain the trap-induced leakage current density from

$$I_{it} = A_g \Delta J_{it} = qn_i \left(\frac{\sigma_s v_{th} \Delta N_{it}}{2} \right) \quad (3)$$

Therefore, the energy-dependent interface state density D_{it} [$\text{cm}^{-2} \text{eV}^{-1}$] can be obtained from

$$D_{it} = \frac{\partial \Delta N_{it}}{\partial V_G} \frac{\partial V_G}{\partial \phi_S} = \frac{2}{A_g q n_i \sigma_s v_{th}} \frac{\partial \Delta I_{it}}{\partial V_G} \frac{\partial V_G}{\partial \phi_S} \quad (4)$$

and experimentally extracted D_{it} is shown in Fig. 2.

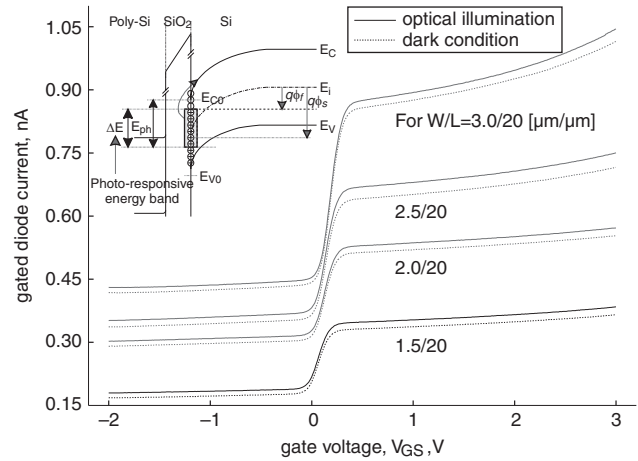


Fig. 1 *I*–*V* characteristics of the gated-diode in N-MOSFETs under sub-bandgap photonic excitation.

Inset: Schematic energy band diagram for a specific gate bias and generation of excess electrons from the interface states in N-MOS under sub-bandgap optical excitation with $E_{ph} < E_g$.

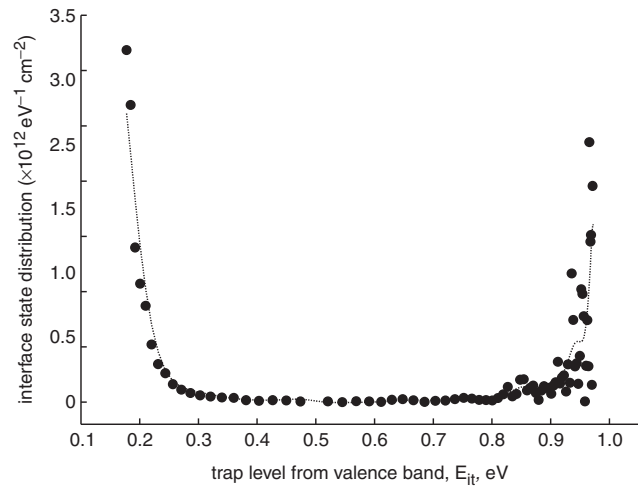


Fig. 2 Interface trap distribution (D_{it}) at Si/SiO₂ interface obtained from sub-bandgap photonic gated-diode *I*–*V* characteristics

Spatial profiling of interface states: A reverse voltage V_R is applied across the drain–substrate junction in MOSFETs and the current is measured against reverse voltage. With the gate voltage fixed at the flat band voltage (V_{FB}), the distribution of traps in the channel near the drain can be obtained from the optically-induced leakage currents as the schematic energy band diagram against reverse bias as shown in Fig. 1. All of the interface states cannot be filled with electrons without channel depletion by the reverse voltage. Increasing the reverse voltage, interface states in the depletion region are filled with electrons. In this condition, optical illumination is applied to the device under test to pump electrons to the conduction band and these electrons contribute to the surface generation current, which forms the interface state-induced-current, I_{it} as comparatively shown in Fig. 3. From the difference between the current under sub-bandgap photonic-illumination and the dark current, interface states N_{it} can be obtained from the interface-induced-current as

$$I_{it} \equiv I_{Op} - I_{Dk} = WL_{Dep} J_{it} = WL_{Dep} q n_i \left(\frac{\sigma_s v_{th} N_{it}}{2} \right) \quad (5)$$

We note that the difference in the reverse currents strongly depends on the depletion width of the drain junction. The relation between the trapped electrons in the interface states and a variation in the probed current can be described as

$$\Delta I_{it}(L_{Dep}) = qn_i W \int_0^{L_{Dep}} \Delta N_{it} dx \quad (6)$$

$$N_{it} \cdot (L_{Dep0} + \Delta L) - N_{it}(L_{Dep0}) = \frac{2}{Wqn_i\sigma_s v_{th}} \cdot f(L_{Dep}) \quad (7)$$

Therefore, spatial distributions of interface states in the channel near the drain can be obtained from

$$N_{it} = \frac{2}{Wqn_i\sigma_s v_{th}} \cdot \frac{\partial I_{it}}{\partial V_D} \cdot \frac{\partial V_D}{\partial L_{Dep}} \quad (8)$$

where

$$L_{Dep} = \sqrt{\frac{2\epsilon_s(V_{bi} + V_{Drain})}{qN_{Sub}}} \quad (9)$$

$$f(L_{Dep}) = I_{it}(L_{Dep0} + \Delta L) - I_{it}(L_{Dep0}) \quad (10)$$

Extracted spatial distribution of the traps at the SiO₂/Si interface is shown in Fig. 4

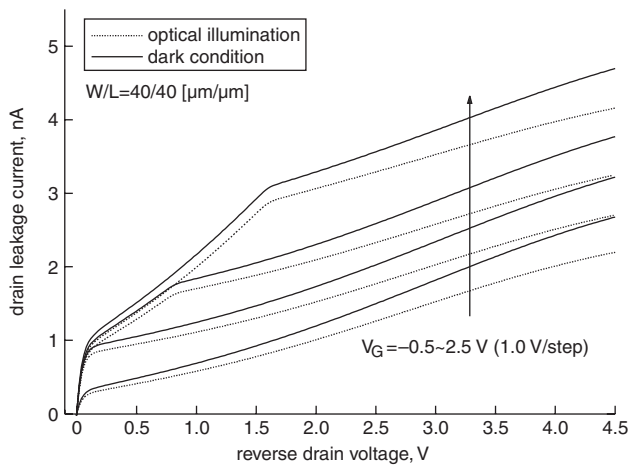


Fig. 3 Measured reverse gated-diode current against drain voltage under sub-bandgap photonic excitation

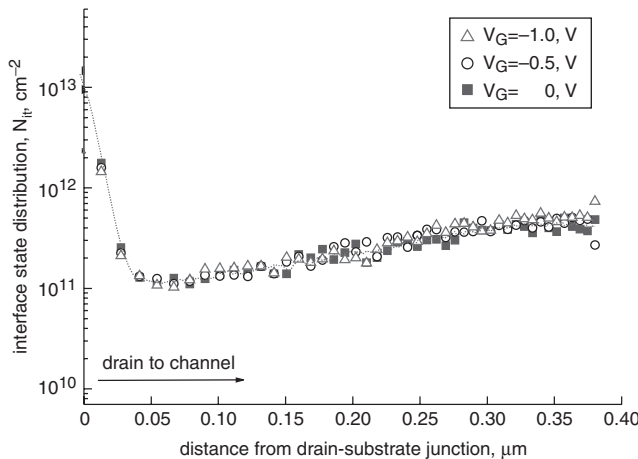


Fig. 4 Spatial distribution of interface trap density (N_{it}) obtained from sub-bandgap photonic gated-diode method

Conclusion: Based on the new PGDM method for MOSFETs under sub-bandgap photonic excitation, the trap density at the SiO₂/Si interface was characterised. A sub-bandgap optical source with a photon energy less than the silicon bandgap was employed for the photonic characterisation of interface states distributed in the photo-responsive energy band ($E_C - 0.95 \leq E_{it} \leq E_C$) in MOS systems. A U-shaped distribution of D_{it} has been obtained over the energy band ($E_C - 0.95 \leq E_{it} \leq E_C$) for N-MOSFETs. Spatial distribution of interface states near the drain has also been characterised using the proposed PGDM technique. We expect this new characterisation technique to be simple and accurate and to be of use for extracting the traps in MOSFETs under room temperature.

Acknowledgment: This work was supported by the Kookmin University Research Initiative Program.

© IEE 2003

10 September 2003

Electronics Letters Online No: 20031080

DOI: 10.1049/el:20031080

S.S. Chi (Hynix Semiconductor Inc., Kyunggi, Korea)

H.T. Kim, M.S. Kim, T.E. Kim, H.T. Shin, H.S. Park, K.H. Kim, K.S. Kim, I.C. Nam, D.J. Kim, K.S. Min, D.W. Kang and D.M. Kim (School of Electrical Engineering, Kookmin University, 861-1 Jungnung, Sungbuk, Seoul 136-702, Korea)

References

- BORSE, D.G., VAIDYA, S.J., and CHANDORKAR, A.N.: 'Study of SILC and interface trap generation due to high field stressing and its operating temperature dependence in 2.2 nm gate dielectrics', *IEEE Trans. Electron Devices*, 2002, **49**, pp. 699–701
- YU, J.-C., LAI, B.C., and LEE, J.Y.M.: 'Fabrication and characterization of metal-oxide-semiconductor field-effect transistors and gated diodes using Ta₂O₅ gate oxide', *IEEE Electron Device Lett.*, 2000, **21**, pp. 537–539
- MILITARU, L., MASSON, P., and GUEGAN, G.: 'Three level charge pumping on a single interface trap', *IEEE Electron Device Lett.*, 2002, **23**, pp. 94–96
- MELIK-MARTIROSIAN, A., and MA, T.P.: 'Lateral profiling of interface traps and oxide charge in MOSFET devices: charge pumping versus DCIV', *IEEE Trans. Electron Devices*, 2001, **48**, pp. 2303–2309
- CHU, Y.-L., LIN, S.-W., and WU, C.-Y.: 'A new charge-pumping technique for profiling the interface-states and oxide-trapped charges in MOSFETs', *IEEE Trans. Electron Devices*, 2000, **47**, pp. 348–353
- CHEN, C., and MA, T.P.: 'Direct lateral profiling of hot-carrier-induced oxide charge and interface traps in thin gate MOSFETs', *IEEE Trans. Electron Devices*, 1998, **45**, pp. 512–520
- KIM, D.M., KIM, H.C., and KIM, H.T.: 'Photonic high-frequency capacitance-voltage characterization of interface states in metal-oxide-semiconductor capacitors', *IEEE Trans. Electron Devices*, 2002, **49**, pp. 526–528