Modeling and Separate Extraction Technique for Gate Bias-Dependent Parasitic Resistances and Overlap Length in MOSFETs

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***Abstract*— We report a technique for separate extraction of extrinsic source/drain (S/D) resistances (R_{Se}/R_{De}) and gate bias (V_{GS})-dependent but channel length (L)-independent intrinsic source/drain (R_{Si}/R_{Di}) resistances for the overlap region in MOSFETs. For extraction of the overlap length (L_{ov}) in the heavily doped S/D regions, an analytical capacitance model for the depletion region is employed with the gate-to-source and gate-to-drain capacitance–voltage ($C_{G\text{-}S}$, $C_{G\text{-}D}$) characteristics. After verifying the extracted overlap length through a 2-D technology computer-aided design simulation, we successfully extract V_{GS}-dependent $R_{Si} = 0.9\sim3.7\ \Omega$ and $R_{Di} = 1.0\sim3.9\ \Omega$ in an n-channel MOSFET with $W = 140\ \mu$m and $L = 0.35\ \mu$m. In addition, V_{GS}- and L-independent extrinsic S/D resistances are separately extracted to be $R_{Se} = 5.1\ \Omega$ and $R_{De} = 5.0\ \Omega$, respectively.**

***Index Terms*— Drain resistance, extrinsic resistance, intrinsic, MOSFET, overlap length (L_{ov}), source resistance.**

I. Introduction

As MOSFETs are scaled down to establish improved electrical performance and integration density, the source (R_S) and drain (R_D) resistances become increasingly important in terms of long-term performance and reliability in integrated circuits. Therefore, accurate modeling and extraction of R_S and R_D considering gate bias (V_{GS}) dependence is necessary for prediction of the drive current degradation [1], [2]. R_S and R_D are generally regarded as symmetric and V_{GS}-independent parameters, but practical asymmetry and V_{GS}-dependence can be induced by asymmetric layout, process variation, and/or long-term degradation caused by hot carriers. Even with symmetrical device structure and fabrication through the same process, hot carriers during long-term operation cause asymmetry in R_S and R_D. The asymmetry observed in R_S and R_D can also be used as an indicative parameter of physical mechanisms on degradation by hot carrier stress or long-term operation. In particular, R_S is more influential on the electrical performance of the transconductance, the cutoff frequency over R_D.

Although there have been various methods for separate extraction of R_S and R_D [3]–[7], both asymmetry and V_{GS}-dependence have not been fully considered. There have been useful works for the extraction of V_{GS}-dependent R_S and R_D combining the additional resistance method [8], [9]. Even if these methods have considerable accuracy, additional external resistance and/or nonlinear fitting process with a body contact is required for the extraction of V_{GS}-dependent R_S and R_D.

We propose a technique for separate extraction of V_{GS}-dependent intrinsic source/drain (S/D) resistances (R_{Si}/R_{Di}) and V_{GS}-independent components (R_{Se}, R_{De}). As R_{Si} and R_{Di} are predominantly influenced by the vertical field through the overlapped S/D regions, we first obtained the overlap length (L_{ov}) from the analytical capacitance model of the depletion region and verified it through a 2-D Sentaurus TCAD simulation. To completely extract R_S separated from R_D, we combined two methods. First, the transfer length method (TLM) was used for extraction of $R_S + R_D$ including both V_{GS}-dependent (R_{Si}, R_{Di}) and -independent (R_{Se}, R_{De}) components. Second, the dual-sweep combinational transconductance technique [12] combined with the channel resistance method (CRM) [10] was utilized for V_{GS}-independent $R_S + R_D$ and V_{GS}-dependent $R_S - R_D$.

II. Extraction of Overlap Length With Analytical Capacitance Model in MOSFETs

Fig. 1 shows a cross-sectional structure associated with resistances and capacitances of an n-channel MOSFET for characterization through the equivalent circuit.

The V_{GS}-dependent overlap capacitance C_{ov} is defined as the capacitance between the gate and the S/D overlap region to be

$$C_{ov}(V_{GS}) = \varepsilon_{ox} W \cdot L_{ov}(V_{GS})/t_{ox} \quad (1)$$

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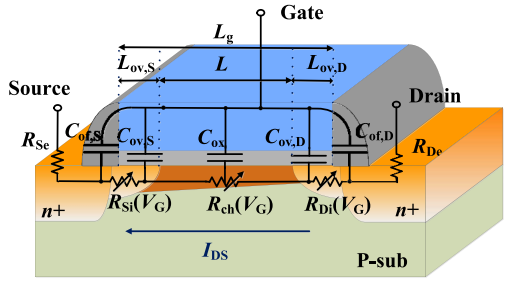

Fig. 1. Cross-sectional structure and associated equivalent circuit model with resistances and capacitances in n-channel MOSFETs.

with ε_{ox} as the permittivity and t_{ox} as the thickness of the insulating gate oxide with W as the gate width of the MOSFET under characterization.

In [13], even though V_{GS}-dependent L_{ov} was proposed as an empirical model, the analytical model is lacking in V_{GS}-dependent L_{ov} modeling. When the gate is biased at $V_i < V_{GS} < V_{FB,ov}$, as a bias condition for a depletion of the overlapped region ($V_i \equiv$ the gate voltage for the surface potential to be equal to the Fermi potential ($\varphi_{SD,ov} = \phi_f$), $V_{FB,ov} =$ the flat band voltage for the overlap region), charges in the overlapped region are dominated by the depleted acceptors in the p-type substrate and accumulated electrons in the highly doped (n^+) S/D region. Consequently, C_{ov} can be modeled as

$$\left.\frac{1}{C_{ov}(V_{GS})}\right|_{V_i<V_{GS}<V_{FB,ov}} = \frac{t_{ox}}{\varepsilon_{ox}(W\cdot L_{ov})} + \frac{1}{C_d(V_{GS})+C_n} \tag{2}$$

with $C_d(V_{GS})$ and C_n as capacitances for depleted acceptors and accumulated electrons, respectively.

Equation (2) can be modified by the well-known charge model [14] described as

$$\begin{aligned} C_{ov}(V_G)|_{V_i<V_G<V_{FB,ov}} &= \frac{C_{ox}(W\cdot L_{ov})}{1+\frac{k}{\left(\frac{1}{\sqrt{|\varphi_{SD,ov}|}}+\frac{1}{\sqrt{V_{th}}}e^{\frac{\varphi_{SD,ov}}{2V_{th}}}\right)}} \\ k &\equiv \sqrt{2C_{ox}^2/q\varepsilon_{si}N_{SD,ov}}, \\ C_{ox} &\equiv \varepsilon_{ox}/t_{ox} \end{aligned} \tag{3}$$

with $\varphi_{SD,ov}$ as the surface potential, $N_{SD,ov}$ as the doping concentration in the n^+ S/D overlap region, V_{th} as the thermal voltage, and C_{ox} ($\equiv \varepsilon_{ox}/t_{ox}$) as the oxide capacitance per unit area.

The gate-to-drain capacitance ($C_{GD} = C_{ov} + C_{of}$) in Fig. 1 for $V_i < V_{GD} < V_{FB,ov}$ is described as

$$C_{GD}|_{V_i<V_{GD}<V_{FB,ov}} = \frac{C_{ox}(W\cdot L_{ov,D})}{1+\frac{k}{\left(\frac{1}{\sqrt{-\varphi_{SD,ov}}}+\frac{1}{\sqrt{V_{th}}}e^{\frac{\varphi_{SD,ov}}{2V_{th}}}\right)}} + C_{of} \tag{4}$$

with C_{of} as the V_{GS}-independent capacitance associated with the fringing field between the sidewall of the gate and the S/D edge. We note that C_{of} becomes more significant and comparable with other capacitances in MOSFETs with scaling down.

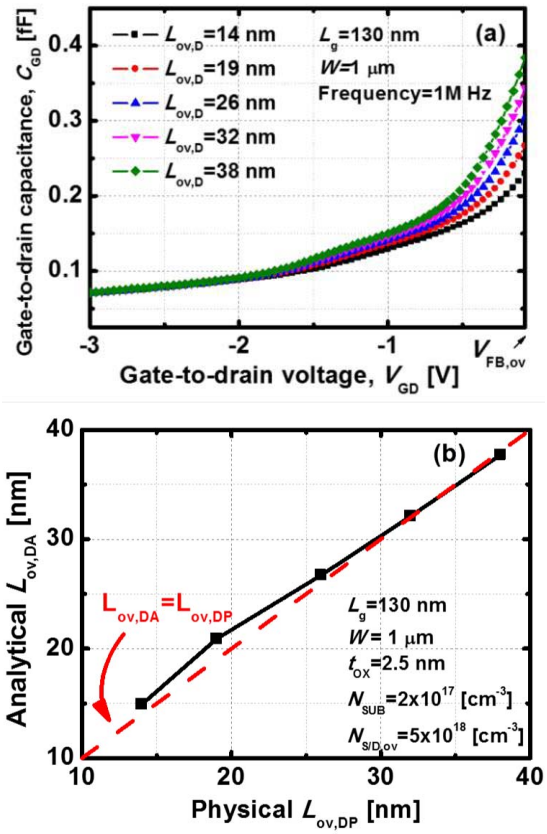

Fig. 2. (a) Simulated C_{GD}–V_{GD} characteristics for various $L_{ov,D}$ in an n-channel MOSFET with $W/L = 1/0.13$ [μm/μm] when $V_{GD} < V_{FB,ov}$. (b) Comparison of the physical (obtained from experimental data) $L_{ov,D}$ and $L_{ov,D}$ calculated by the analytical charge model for various $L_{ov,D}$.

As mentioned above, however, it is well known that C_{of} is independent of V_{GS}. Consequently, by eliminating C_{of} through (4) with the boundary condition at $V_{GD} = V_{FB,ov}$, the overlap length in the drain ($L_{ov,D}$) can be extracted through

$$\begin{aligned} L_{ov,D} &= \frac{C_{GD}|_{V_{GD}=V_{FB,ov}} - C_{GD}|_{V_i<V_{GD}<V_{FB,ov}}}{(1-1/\lambda(\varphi_{SD,ov}))\cdot C_{ox}\cdot W} \\ \lambda(\varphi_{SD,ov}) &\equiv 1+\frac{k}{\left(\frac{1}{\sqrt{-\varphi_{SD,ov}}}+\frac{1}{\sqrt{V_{th}}}e^{\frac{\varphi_{SD,ov}}{2V_{th}}}\right)}. \end{aligned} \tag{5}$$

Through the 2-D TCAD simulation, we confirmed that $L_{ov,D}$ decreases with decreasing V_{GD}. This is due to the additional capacitance component ($C_{SD,add}$) away from the S/D overlap region which is indirectly influenced by V_{GS}. We define the physical L_{ov} as the maximum value of experimentally obtained overlap length at $V_{GS} \cong V_{FB,ov}$ for minimizing the effect of $C_{SD,add}$. Fig. 2(a) shows the simulated C_{GD}–V_{GD} characteristics for various $L_{ov,D}$ in an n-channel MOSFET with $W/L = 1/0.13$ [μm/μm] and parameters summarized in Fig. 2(b). From the proposed analytical capacitance model, we simulated various cases of physical $L_{ov,D}$ and confirmed good agreement between the physical $L_{ov,D}$ (defined in the simulation) and analytical $L_{ov,D}$ (obtained from experimental data), as shown in Fig. 2(b).

After verifying the validity of the proposed model, we extracted L_{ov} from the experimental data.

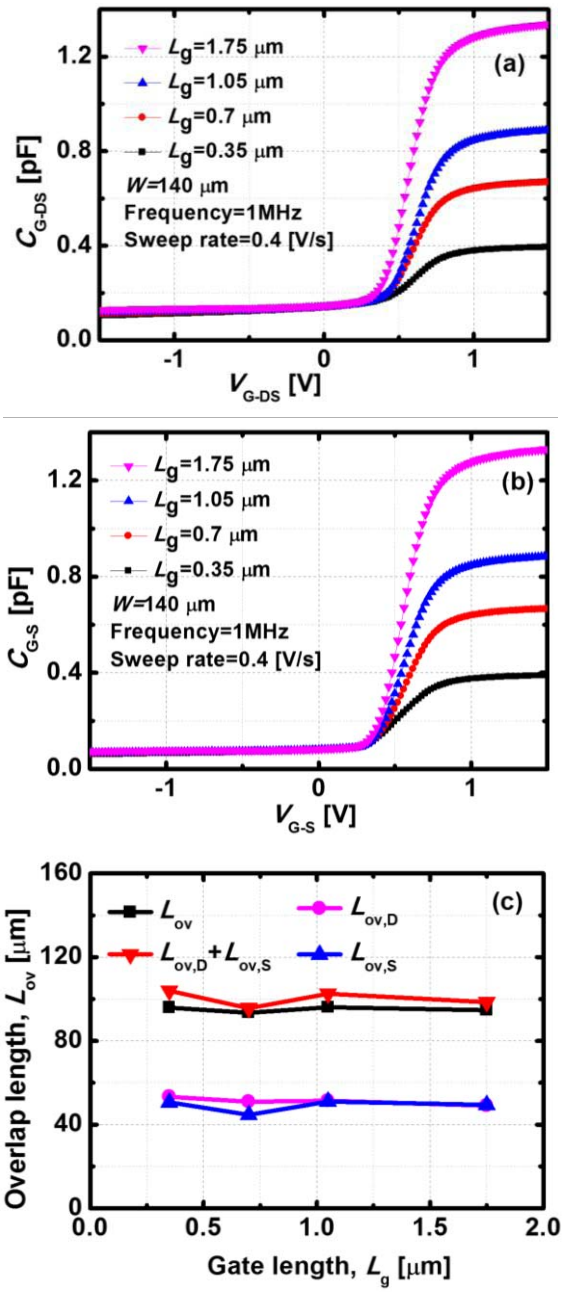

Fig. 3. Measured (a) $C_{G\text{-DS}}$–$V_{G\text{-DS}}$, (b) $C_{G\text{-}S}$–$V_{G\text{-}S}$ characteristics of an n-MOSFET with W/L = 140/0.35, 0.7, 1.05, 1.75 [μm/μm]. (c) Extracted L_{ov}, $L_{ov,D}$, and $L_{ov,S}$ with various gate lengths.

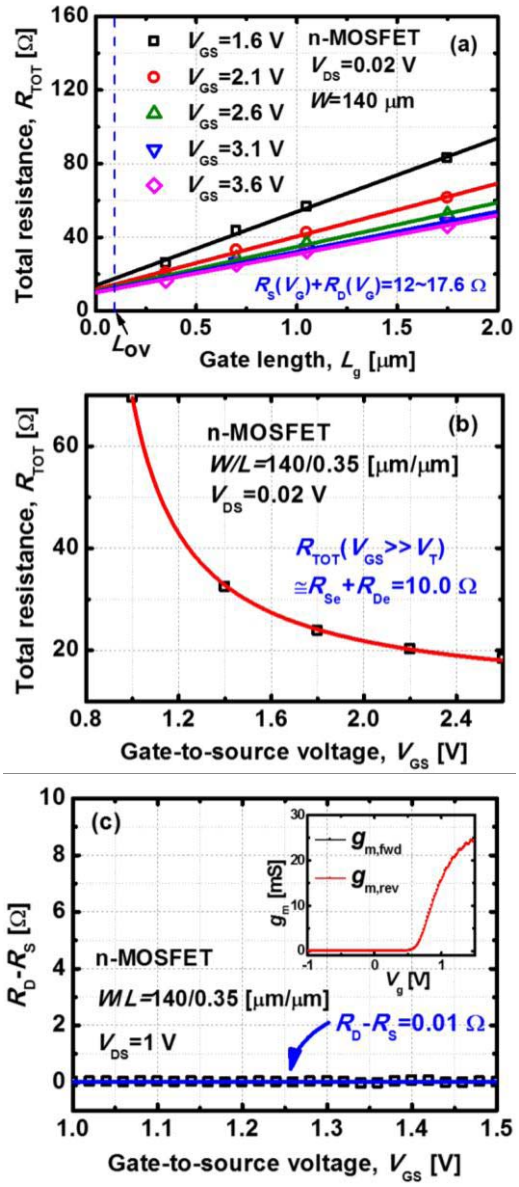

Fig. 4. (a) $R_{TOT} - L_g$ for the extraction of $R_S + R_D$ with $V_{GS} = 1.6 \sim 3.6$ V. (b) $R_{TOT} - V_G$ for the extraction of $R_{Se} + R_{De}$ in n-MOSFET with $W/L = 140/0.35$ [μm/μm]. (c) Extracted $R_D - R_S$ using the dual-sweep combinational transconductance technique. Inset shows g_m in forward and reverse modes.

Combining three different capacitance–voltage measurement configurations [$C_{G\text{-DS}}$–$V_{G\text{-DS}}$, $C_{G\text{-D}}$–$V_{G\text{-}D}$,$C_{G\text{-}S}$–$V_{G\text{-}S}$, as shown in Fig. 3(a) and (b)], overlap lengths (L_{ov}, $L_{ov,D}$, and $L_{ov,S}$) were extracted for various gate lengths (L_g), as shown in Fig. 3(c). It shows good consistency between L_{ov} and $L_{ov,D} + L_{ov,S}$.

III. Separate Extraction of Gate Bias-Dependent S/D Resistances

As shown in Fig. 1 for the MOSFET biased in the linear operation, the resistance model for the drain-to-source current (I_{DS}) path includes V_{GS}-dependent intrinsic source (R_{Si}) and drain resistances (R_{Di}), V_{GS}-independent extrinsic source (R_{Se}) and drain (R_{De}) resistances as follows:

$$R_{TOT}(V_{GS}) \equiv V_{DS}/I_{DS} = R_S(V_{GS}) + R_D(V_{GS}) + R_{ch}(V_{GS}, L_g) \quad (6)$$

$$R_S(V_{GS}) = R_{Si}(V_{GS}) + R_{Se},\ R_D(V_{GS}) = R_{Di}(V_{GS}) + R_{De}. \quad (7)$$

As the first step for separate extraction of each component, we employ the TLM technique for $R_{sum} \equiv R_S(V_{GS}) + R_D(V_{GS})$. The TLM has been generally used for extraction of $R_{SD} = R_S + R_D$ from the V_{GS}-dependent total resistance extrapolated to $V_{GS} - V_T \cong \infty$ under the assumption of V_{GS}-independent R_S and R_D. However, R_S and R_D are clearly

TABLE I
V_{GS}-DEPENDENT AND INDEPENDENT S/D RESISTANCES IN A MOSFET WITH $W/L = 140/0.35$ [μm/μm]

V_{GS} [V]	V_{GS}-dependent resistances		V_{GS}-independent resistances	
	R_{Si} [Ω]	R_{Di} [Ω]	R_{Se} [Ω]	R_{De} [Ω]
1.6	3.7	3.9	5.1	5.0
2.1	2.1	2.2		
2.6	1.4	1.5		
3.1	1.1	1.2		
3.6	0.9	1.0		

TABLE II
V_{GS}-DEPENDENT AND INDEPENDENT S/D RESISTANCES IN A MOSFET HAVING AN EXTERNAL DRAIN RESISTANCE $R_{D,ext} = 3.9$ [Ω] WITH $W/L = 140/0.35$ [μm/μm]

V_{GS} [V]	V_{GS}-dependent resistances		V_{GS}-independent resistances	
	R_{Si} [Ω]	R_{Di} [Ω]	R_{Se} [Ω]	R_{De} [Ω]
1.6	3.9	3.7	5.0	9.2
2.1	2.0	2.0		
2.6	1.3	1.4		
3.1	1.1	1.1		
3.6	0.7	0.7		

V_{GS}-dependent by the overlap region directly influenced by the vertical field. Therefore, we extract V_{GS}-dependent but the channel length (L)-independent ($R_S + R_D$) with L_{ov} obtained from the analytical capacitance model. It can be described as

$$R_{TOT}|_{L_g=L_{ov}} = R_{Si}(V_{GS}) + R_{Se} + R_{Di}(V_{GS}) + R_{De}. \quad (8)$$

Fig. 4(a) shows extracted $R_{TOT}(V_{GS}) = R_S(V_{GS}) + R_D(V_{GS})$ as a function of V_{GS}.

As the next step, we use the CRM for extraction of V_{GS}-independent $R_{Se} + R_{De}$. As V_{GS} increases more, V_{GS}-dependent resistance components get smaller. Therefore, $R_{Se} + R_{De}$ is obtained at $V_{GS} \gg V_T$ through

$$R_{TOT}|_{V_{GS} \gg V_T} = R_{Se} + R_{De}. \quad (9)$$

Fig. 4(b) shows the extrapolated R_{TOT} ($= R_{Se} + R_{De}$) in a MOSFET with $W/L = 140/0.35$ [μm/μm]. By subtracting (9) from (8), $R_{Si}(V_{GS}) + R_{Di}(V_{GS})$ is obtained. $R_{Si}(V_{GS}) + R_{Di}(V_{GS})$ can be separated by $L_{ov,D}$ and $L_{ov,S}$ extracted from the analytical capacitance model through

$$R_{Si}(V_{GS}) = \frac{L_{ov,S}}{L_{ov,S} + L_{ov,D}} \times (R_{Si}(V_{GS}) + R_{Di}(V_{GS})) \quad (10)$$

$$R_{Di}(V_{GS}) = \frac{L_{ov,D}}{L_{ov,S} + L_{ov,D}} \times (R_{Si}(V_{GS}) + R_{Di}(V_{GS})). \quad (11)$$

By the dual-sweep combinational transconductance technique as the next step, $R_{dif} \equiv R_D(V_{GS}) - R_S(V_{GS})$ can be experimentally obtained from the forward and reverse transconductances in the saturation region. As shown in Fig. 4(c), we extracted $R_{dif} \equiv R_D(V_{GS}) - R_S(V_{GS})$ from the forward and reverse transfer characteristics for the same drain current (I_{Do}) $\equiv I_{D,FWD}(V_{GS,FWD}) = I_{D,REV}(V_{GS,REV})$ of the MOSFET through

$$R_{dif} \equiv R_D(V_{GS}) - R_S(V_{GS}) = \frac{V_{GS,REV} - V_{GS,FWD}}{I_{Do}}. \quad (12)$$

We separated $R_D(V_{GS})$ from $R_S(V_{GS})$ combining $R_{sum} \equiv R_D(V_{GS}) + R_S(V_{GS})$, obtained from the TLM, with $R_{dif} \equiv R_D(V_{GS}) - R_S(V_{GS})$ from the dual-sweep combinational transconductance technique. Finally, using the separated S/D resistances with (10) and (11), R_{Se} and R_{De} are separated.

Table I shows separated resistances for various V_{GS} in the n-channel MOSFET with $W/L = 1/0.13$ [μm/μm]. As V_{GS} decreases, V_{GS}-dependent resistances increase significantly in contrast to V_{GS}-independent resistances. As a verification of the proposed method in asymmetric MOSFET structures, we intentionally loaded a resistance ($R_L = 3.9\ \Omega$) in drain contact to make the device asymmetric for the extrinsic drain resistance. As expected, the extracted results show good agreement with the increase in V_{GS}-independent R_D.

Expecting intentional asymmetric structure between R_S and R_D, due to a limited availability of asymmetric S/D MOSFETs, we added an intentional load resistance ($R_{D,ext} = 3.9\ \Omega$) to the drain contact. Consequently, the extracted results show good agreement with the increase in V_{GS}-independent R_{De}, as shown Table II.

IV. CONCLUSION

Considering the asymmetry and V_{GS}-dependence in the S/D resistances caused by layout, process variation, and long-term device degradation by hot carriers, we proposed a technique for separate extraction of V_{GS}-dependent but L-independent S/D resistances (R_{Si}, R_{Di}) related to the overlap region and V_{GS}-independent S/D resistances (R_{Se}, R_{De}) in MOSFETs. For extraction of V_{GS}-dependent R_{Si} and R_{Di}, the extraction technique based on the analytical capacitance model for the overlap length (L_{ov}) was also reported. Verifying the validity of the extraction technique for L_{ov} through a 2-D TCAD simulation, we successfully extracted V_{GS}-dependent R_{Si} and R_{Di} applying the extracted L_{ov} from the experimental results. We expect that the proposed technique for separate extraction of V_{GS}-dependent S/D resistances and the overlap length L_{ov} as well as V_{GS}-independent S/D resistance components is useful for accurate modeling, characterization, and robust design of CMOS-based integrated circuits and systems.

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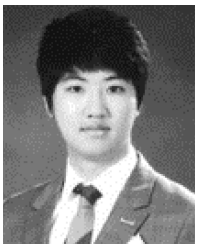

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