JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.15, NO.5, OCTOBER, 2015
http://dx.doi.org/10.5573/JSTS.2015.15.5.497
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

Frequency-dependent C-V Characteristic-based Extraction of Interface Trap Density in Normally-off Gate-recessed AlGaN/GaN Heterojunction Field-effect Transistors

Sungju Choi[1], Youngjin Kang[2], Jonghwa Kim[1], Jungmok Kim[1], Sung-Jin Choi[1], Dong Myong Kim[1], Ho-Young Cha[2], Hyungtak Kim[2], and Dae Hwan Kim[1,*]

Abstract—**It is essential to acquire an accurate and simple technique for extracting the interface trap density (D_{it}) in order to characterize the normally-off gate-recessed AlGaN/GaN hetero field-effect transistors (HFETs) because they can undergo interface trap generation induced by the etch damage in each interfacial layer provoking the degradation of device performance as well as serious instability. Here, the frequency-dependent capacitance-voltage (*C-V*) method (FDCM) is proposed as a simple and fast technique for extracting D_{it} and demonstrated in normally-off gate-recessed AlGaN/GaN HFETs. The FDCM is found to be not only simpler than the conductance method along with the same precision, but also much useful for a simple *C-V* model for AlGaN/GaN HFETs because it identifies frequency-independent and bias-dependent capacitance components.**

Index Terms—**normally-off, gate-recessed, AlGaN/GaN HFETs, interface trap density, frequency-dependent *C-V*.**

Manuscript received Apr. 17, 2015; accepted Sep. 16, 2015
[1] School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea
[2] School of Electronic and Electrical Engineering, Hongik University, Seoul 121-791, Korea
E-mail : drlife@kookmin.ac.kr

I. INTRODUCTION

GaN-based high electron mobility transistors (HEMTs) have been recognized as attractive candidates for high power and high frequency applications under high temperature due to its beneficial features, such as maximum frequency of oscillations, low specific on-resistance, and high breakdown voltage. However, in the case of Schottky-gate HEMTs, there has been remaining problems of large off-state leakage and collapse current which result from a high density of the surface and interface traps [1]. Then the AlGaN/GaN Heterojunction field-effect transistors (HFETs) with the gate-recessed metal-oxide-semiconductor structures were proposed as propitious devices for the normally-off GaN-based HEMT with advantages, such as a thin barrier layer, low gate leakage, and high breakdown voltage [2-4].

For such reasons, the density of interface traps (D_{it}) should be exactly characterized especially with the gate-recessed AlGaN/GaN HFETs because they undergo the trap generation induced by the etch damage in each interfacial layer, which would cause the degradation of device performance as well as serious instability [5-7]. A high D_{it} is well known to be affecting the degradation of response time, trap effect of current transient, frequency dispersion, mobility, subthreshold swing and low frequency noise [8]. Several methods such as deep-level transient spectroscopy (DLTS) [9], conductance method (CM) [6], and differential ideality factor technique (DIFT) [10], have been employed in extracting D_{it}.

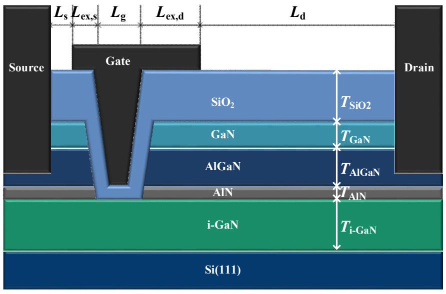


Fig. 1. A schematic view of normally-off gate-recessed AlGaN/GaN HFET. Geometrical parameters are the width W=100 [μm], L_s=2 [μm], $L_{ex,s}$=1 [μm], L_g=2 [μm], $L_{ex,d}$=3 [μm], L_d=12 [μm], T_{SiO2}= 30 nm, T_{GaN}=4 nm, T_{AlGaN}=20 nm, T_{AlN}= 2 nm, and $T_{i\text{-}GaN}$=1.7 [μm]

However, these methods have some drawbacks, such as requiring many parameters, which need to be experimentally extracted, and somewhat complicated measurement setup as well as such a narrow range of available energy levels.

In this work, we demonstrate the D_{it} extraction by using the frequency-dependence of capacitance-voltage (C-V) characteristics in the gate-recessed normally-off AlGaN/GaN HFETs. The proposed frequency-dependent C-V method (FDCM) enables a simple and fast extraction of D_{it} in comparison with the previous techniques. Also the C_{GaN} by free carrier and trap emission time(τ_{it}) can be extracted by FDCM. Therefore, the D_{it}-independent mobility is extracted, helping to understand the relation between D_{it} by gate-recessed process and mobility of device and the trap density of each interface between layers by using relation of τ_{it} - D_{it}. We believe that the FDCM is also very effective and adequate for an advanced C-V model for AlGaN/GaN HFETs because it identifies the frequency-independent and bias-dependent capacitance components while the extracted D_{it} is consistent with that extracted from a conventional CM.

II. Device Fabrication and Structure

The normally-off gate-recessed AlGaN/GaN HFETs used in this study were integrated with a Si substrate as shown in Fig. 1.

The epitaxial layer structure is fabricated with a 4-nm-thick undoped GaN capping layer, a 20-nm-thick undoped $Al_{0.23}Ga_{0.77}N$ barrier, a 1-nm-thick AlN spacer layer, and a 1.7-μm-thick i-GaN buffer layer on Si (111)

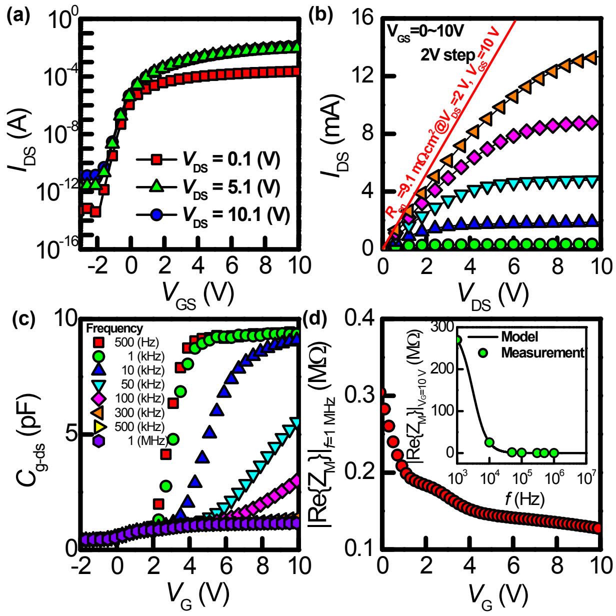


Fig. 2. (a) The measured transfer (I_{DS}-V_{GS}) characteristics in V_{DS}= 0.1 [V], 5.1 [V], and 10.1 [V], (b) the inset figure of the measured output (I_{DS}-V_{DS}) characteristics in V_{GS}=0~10 [V], (c) The measured $C_{G\text{-}DS}$-V_G characteristics with various small-signal frequencies, (d) The extracted R_S (V_G) with the inset figure of the real part of Z_M which is a function of a small signal frequency

substrate. After the mesa isolation using a low-damage plasma-etching, both the GaN capping layer and the AlGaN barrier in the gate region were fully recessed by using Cl_2/BCl_3-based inductively coupled plasma (ICP) reactive ion etching. Then, a 30-nm-thick SiO_2 dielectric layer was deposited as a gate insulator by ICP chemical vapor deposition process. For the source and drain contact formation, a Ti/Al/Ni/Au metal stack was evaporated and alloyed. The following patterning process defined gate regions and a Ni/Au metal stack was evaporated for gate contact. The gate-to-drain distance (L_{gd}=L_d+$L_{ex,d}$ in Fig. 1), recessed gate length (L_g), and gate-to-source distance (L_{gs}=L_s+$L_{ex,s}$) were 15 μm, 2 μm, and 3 μm, respectively.

Fig. 2(a) represents the transfer (I_{DS}-V_{GS}) characteristics with various values of V_{DS} which are measured at room temperature and dark ambient through an Agilent 4156C precision semiconductor parameter analyzer. The V_T~2 [V] is obtained by the linear extrapolation at V_{DS} = 0.1 [V]. Here, the subthreshold swing is 0.212 [V/dec] in the range of I_{DS}= 10^{-12}~10^{-9} [A] while the on-resistance(R_{ON}) is 9.1 [mΩ·cm^2] at V_{DS} =2 [V] and V_{GS}=10 [V]. Observed values of device parameters indicate that this device satisfies the requirements for high performance, fast switching speed, and normally-off switching that are critical for commercialization of AlGaN/GaN based power switching device.

Fig. 2(c) shows the frequency-dependent *C-V* curves which are characterized through C_M-R_M parallel mode of an Agilent 4294A precision impedance analyzer. Here, $C_{G\text{-}DS}$ and V_G signify the capacitance and the dc sweep voltage between the two terminals, i.e., the gate and the source tied with drain. The small-signal amplitude and the sweep rate of V_G are 0.1 V and 0.5 V/s.

III. RESULT AND DISCUSSION

Frequency dependency of the *C-V* curves is attributed to the capture-emission events via the interface and/or bulk traps. Also, the parasitic source/drain series resistance (R_S) affects the frequency dispersion of the *C-V* curves. The model and physical assumption are analogous to [11], meaning that the measured impedance (Z_M) in a parallel mode can be decomposed into the parallel mode capacitance (C_M) and the resistance (R_M) as a function of V_g under various frequencies as shown in Fig. 3(a). Fig. 3(b) also shows the equivalent four-element model including the effective capacitance of gate oxide (C_{EFF}) and series of resistance R_S. Then, Z_M and $Z_{M'}$ are individually obtained by

$$Z_M = \frac{R_M}{1+\left(\omega C_M R_M\right)^2} - \frac{j\omega C_M R_M^2}{1+\left(\omega C_M R_M\right)^2} \quad (1)$$

$$Z_{M'} = R_S + \frac{R_P}{1+(\omega C_p R_p)^2} - j\left(\frac{\omega C_p R_p^2}{1+\left(C_p R_p\right)^2} + \frac{1}{\omega C_{\mathrm{EFF}}}\right) \quad (2)$$

The $R_S(V_G)$ can be determined from the value of a real part of $Z_M(V_G)$ which is saturated with increasing frequency (the inset of Fig. 2(d)) by employing the assumption of $R_S(V_G) = \lim_{\omega\to\infty} \mathrm{Re}\left[Z_M(\omega, V_G)\right]$ [12]. In our case, the C_{EFF} and R_S were extracted from the maximum value of $C_{G\text{-}DS}(V_G)$ and the value of a real part of $Z_M(V_g)$ at the frequency f=1 MHz (Fig. 2(d)), which is based on the approximation of $\lim_{\omega\to\infty} \mathrm{Re}\left[Z_M(\omega, V_G)\right] \approx \mathrm{Re}\left[Z_M(\omega, V_G)\right]\Big|_{\omega=2\pi\ Mrad/s}$ of. The C_{EFF} and R_S then can be de-embedded from the four-element model in Fig. 3(b), which is given by Z_p. Thus, we can obtain the R_p and C_P as functions of experimentally acquired C_M and R_M by using Z_M=$Z_{M'}$. The following is the process to transform the four-element model ($Z_{M'}$) into the physics-based five-element model (Fig. 3(c)). Here, the channel impedance (Z_{CH}) is composed of R_{it}, C_{it}, and C_{GaN}. The R_{it} is the resistance describing the capture-emission process of electrons via the interface trap, and C_{it} and C_{GaN} are the interface trap capacitance and the capacitance of GaN bulk layer.

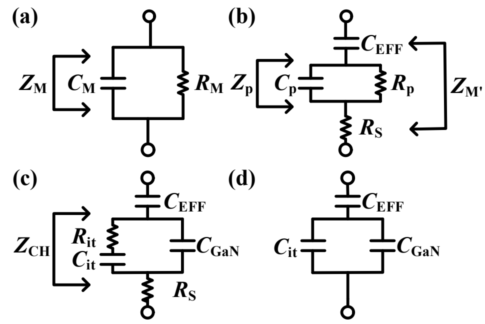


Fig. 3. (a) Equivalent circuit for the parallel mode impedance analyzer, (b) four-element model including the effective capacitance of gate oxide (C_{EFF}) and series resistance (R_s), (c) physics-based five-element model for frequency-dispersive *C-V* characteristics, (d) equivalent model for *f*-independent *C-V* characteristics

In Fig. 3(c), Z_{CH} can be derived by

$$Z_{\mathrm{CH}} = \frac{C_{it}^2 R_{it}}{\omega^2 C_{it}^2 C_{GaN}^2 R_{it}^2 + \left(C_{it}+C_{GaN}\right)^2} - j\frac{\omega^2 C_{it}^2 C_{GaN} R_{it}^2 + \left(C_{it}+C_{GaN}\right)}{\omega^3 C_{it}^2 C_{GaN}^2 R_{it} + \omega\left(C_{it}+C_{GaN}\right)^2} \quad (3)$$

Then, R_{it}^2 is described as follows by using Z_{CH}=Z_p

$$R_{it}^2 = \left\{\frac{\omega^2 C_p R_p^2 \left(C_{it}+C_{GaN}\right)\left(C_{it}+C_{GaN}-C_p\right)}{\omega^2 C_{it}^2 C_{GaN}\left[1+\omega^2 C_p R_p^2\left(C_p - C_{GaN}\right)\right]} - \frac{\left(C_{it}+C_{GaN}\right)}{\omega^2 C_{it}^2 C_{GaN}\left[1+\omega^2 C_p R_p^2\left(C_p - C_{GaN}\right)\right]}\right\} \quad (4)$$

Similarly to [11], it was assumed the value of R_{it} is independent of ω while it is a function of V_g. Thus, we can obtain the $C_{it}(V_G)$ and $C_{GaN}(V_G)$ by using the relation of $R_{it}(\omega_1)$= $R_{it}(\omega_2)$=$R_{it}(\omega_3)$. Here, the ω_1, ω_2, and ω_3 are three different frequencies of a small-signal in the $C_{g\text{-}d/s}$-V_g measurement. Moreover, we can obtain the *f*-independent C_G ($C_{G,\,f\text{-independent}}$) by using the equivalent circuit model in Fig. 3(d). The extracted C_{EFF}, $C_{GaN}(V_G)$,

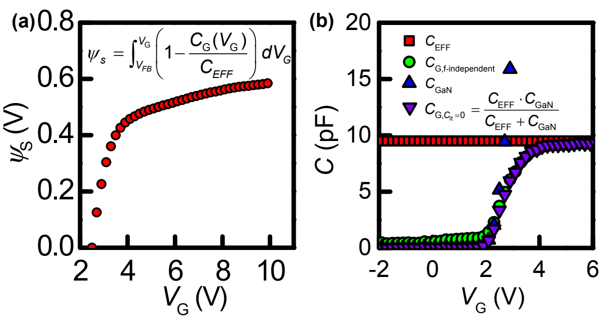


Fig. 4. (a) The relation between V_G and ψ_s which is calculated by using (6), (b) the extracted $C_{G,f\text{-independent}}(V_G)$, $C_{EFF}(V_G)$, $C_{GaN}(V_G)$, and $C_{G,Cit=0}(V_G)$

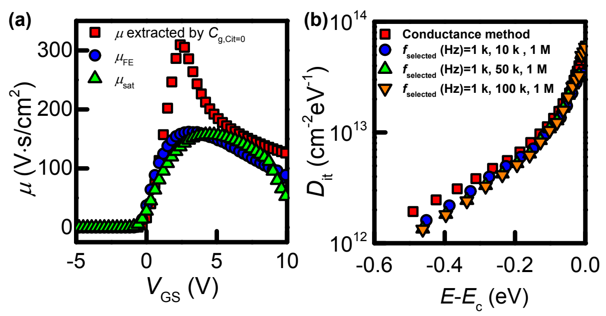


Fig. 5. (a) The comparison of the mobilities extracted by using f-independent C_G, μ_{FE} and μ_{sat}. The extracted $D_{it}(E)$ (b) in a semi-log scale. The $f_{selected}$ means the combination of three different frequencies which was chosen in the FDCM-based extraction of $D_{it}(E)$. The proposed FDCM was also compared with the conventional CM

and $C_{G,f\text{-independent}}(V_G)$ were shown in the Fig. 4(b)

Then, the D_{it} can be extracted as a by

$$D_{it}\left(V_G\right)=\frac{C_{it}\left(V_G\right)}{q^2 Area}=\frac{C_{it}\left(V_G\right)}{q^2 W\times L} \quad (5)$$

where the $D_{it}(V_G)$ can be transformed to $D_{it}(\psi_S)$ by using the relationship between V_G and the surface potential ψ_S. The nonlinear relation between V_G and ψ_S can be also obtained from the $C_{G,f\text{-independent}}(V_G)$ curve (Fig. 4(b)) as follows:

$$\psi_s=\int_{V_{FB}}^{V_G}\left(1-\frac{C_{G,f-independent}\left(V_G\right)}{C_{EFF}}\right)dV_G \quad (6)$$

where the V_{FB} is a flat band voltage. Fig. 4(a) shows the relation between V_g and ψ_S, which is calculated from (6).

Fig. 5(a) shows the D_{it}-independent mobility extracted by using the $C_{G,Cit=0}$ as by [13]

$$Q_{ind}\left(V_G\right)=\int_{-\infty}^{V_{GS}}\left(\frac{C_{G,C_{it}=0}}{WL}\right)dV=\int_{-\infty}^{V_{GS}}\left(\frac{\frac{C_{EFF}\cdot C_{GaN}}{C_{EFF}+C_{GaN}}}{WL}\right)dV \quad (7)$$

$$\mu\left(V_G\right)=\frac{L\cdot I_{DS}\left(V_G\right)}{W\cdot V_{DS}\cdot Q_{ind}\left(V_G\right)} \quad (8)$$

where V_{DS} is the small drain-to-source voltage which makes the channel charge density uniform across the length of the channel, $I_{DS}(V_{GS})$ is the drain-to-source current, and $C_{G,Cit=0}$ is gate capacitance by C_{it}=0 in Fig. 3(d). The proposed mobility can be used to estimate the value of the mobility which can be obtained based on the assumption that there are no D_{it}. Therefore, the Fig. 5(a) indicates that the D_{it} by gate-recessed process affect mobility.

Finally, the $D_{it}(E)$ can be extracted from $D_{it}(\psi_S)$ by using the relation of $E–E_C= –q\psi_S$. Here, the E, E_C, and q are the energy level in sub-bandgap, the conduction band minimum, and the magnitude of single electron charge, respectively. Extracted $D_{it}(E)$ was shown in Fig. 5(b). Here, the $f_{selected}$ means the combination of three different frequencies which was used in extracting $D_{it}(E)$; in detail, the relation of $R_{it}(\omega_1)= R_{it}(\omega_2)=R_{it}(\omega_3)$ as aforementioned. Our result suggests that the extracted $D_{it}(E)$ is nearly independent regardless of the combination of ω_1, ω_2, and ω_3. Therefore, it is verified that the proposed FDCM is a much simpler and faster method rather than the conventional CM because only three different frequencies are enough to extract $D_{it}(E)$. The FDCM-based $D_{it}(E)$ was also compared with the CM-based $D_{it}(E)$ as shown in Fig. 5(b). It is found that the FDCM-based $D_{it}(E)$ agrees well with the CM-based $D_{it}(E)$. Moreover, the extracted $D_{it}(E)$ and $\tau_{it}(V)$ demonstrates the range of 1×10^{12} ~ 6×10^{13} [$cm^{-2}eV^{-1}$] and 5×10^{-5} ~ 8×10^{-4} [s], which is consistent with the previous works [1, 6, 8, 14, 15]. In comparison with CM, the proposed FDCM gives abundant information on critical parameters, such as $C_{G,f\text{-independent}}(V)$, $R_{it}(V)$, $C_{GaN}(V)$, $C_{it}(V)$, $\tau_{it}(V)$, $D_{it}(V)$, and the D_{it}-independent mobility, which are efficiently viable for a simple C-V model of AlGaN/GaN HFETs.

IV. CONCLUSION

We have demonstrated the D_{it} extraction by using the frequency-dependence of *C-V* characteristics in the normally-off gate-recessed AlGaN/GaN HFETs. Our proposed FDCM is not only much efficient than the conventional CM maintaining the same precision, but also highly effective for a simple *C-V* model of the AlGaN/GaN HFETs because it identifies the frequency-independent/dependent and bias-dependent capacitance components. Also the extracted D_{it}-independent mobility can be widely used to understand the relation between D_{it} by gate-recessed process and mobility of device plus the trap density of each interface between layers by using relation of τ_{it} - D_{it}. A simple and efficient *C-V* model is substantially important especially in AlGaN/GaN HFETs where the interface/surface traps play a very important role in switching characteristics and reliability.

ACKNOWLEDGMENTS

This work was supported by National Research Foundation of Korea through the Ministry of Education, Science and Technology (Grant No. 2013R1A1A2013100) and the Ministry of Science, ICT and Future Planning (Grant No. 2013R1A1A2065339), in part by BK+ with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design under Grant 22A20130000042.

REFERENCES

[1] X.-H. Ma, *et al.*, "Quantitative characterization of interface traps in Al2O3/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by dynamic capacitance dispersion technique," *Appl. Phys. Lett.*, vol. 103, no. 3, p. 033510, 2013.

[2] F. Shahedipour-Sandvik, *et al.*, "Enhanced performance of an AlGaN/GaN high electron mobility transistor on Si by means of improved adatom diffusion length during MOCVD epitaxy," *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074002, Jul. 2013.

[3] S. M. Lee, *et al.*, "9.3: Control of Threshold Voltage in Back Channel Etch Type Amorphous Indium Gallium Zinc Oxide Thin Film Transistors," *SID Symp. Dig. Tech. Pap.*, vol. 42, no. 1, pp. 104–106, Jun. 2011.

[4] T. Palacios, *et al.*, "High-power AlGaN/GaN HEMTs for Ka-band applications," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 781–783, Nov. 2005.

[5] S. Dhar, V. R. Balakrishman, V. Kumar, and S. Ghosh, "Determination of energetic distribution of interface states between gate metal and semiconductor in sub-micron devices from current-voltage characteristics," *IEEE Trans. Electron Devices*, vol. 47, no. 2, pp. 282–287, 2000.

[6] X.-Y. Liao, *et al.*, "Interface states in Al_2O_3 /AlGaN/GaN metal-oxide-semiconductor structure by frequency dependent conductance technique," *Chinese Phys. B*, vol. 23, no. 5, p. 057301, May 2014.

[7] G. Meneghesso, *et al.*, "Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives," *IEEE Trans. Device Mater. Reliab.*, vol. 8, no. 2, pp. 332–343, Jun. 2008.

[8] J. Bae, *et al.*, "Characterization of traps and trap-related effects in recessed-gate normally-off AlGaN/GaN-based MOSHEMT," in *2012 International Electron Devices Meeting*, pp. 13.2.1–13.2.4, 2012.

[9] D. K. Schroder, *Semiconductor material and device characterization*, Wiley-Interscience, 2006.

[10] J. Bae, *et al.*, "Differential Ideality Factor Technique for Extraction of Subgap Density of States in Amorphous InGaZnO Thin-Film Transistors," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 399–401, Mar. 2012.

[11] S. Lee, *et al.*, "Extraction of Subgap Density of States in Amorphous InGaZnO Thin-Film Transistors by Using Multifrequency Capacitance–Voltage Characteristics," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 231-233, Mar. 2010

[12] E. H. Nicollian and J. R. Brews, *MOS(Metal Oxide Semiconductor) Physics and Technology*, Wiley, 2003.

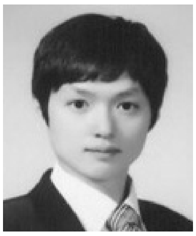
[13] In-Tak Cho, *et al.*, "Extraction of the channel mobility in InGaZnO TFTs Using Multifrequency Capacitance-Voltage Method," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 815-817, Jun. 2012.

[14] D. Gregušová, *et al.*, "Trap states in AlGaN/GaN metal-oxide-semiconductor structures with Al_2O_3

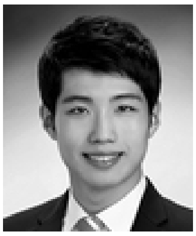
prepared by atomic layer deposition," *J. Appl. Phys.*, vol. 107, no. 10, p. 106104, 2010.

[15] R. M. Chu, *et al.*, "Admittance characterization and analysis of trap states in AlGaN/GaN heterostructures," *Phys. Status Solidi*, vol. 2403, no. 7, pp. 2400–2403, Dec. 2003.

Sungju Choi received the B.S. degree in the School of Electronic engineering from Kookmin University, Seoul, Korea, in 2014. He is currently pursuing the M.S. degree, and his current research interests include characterization and modeling for reliability of III-V compound semiconductor devices and oxide thin-film transistors.



Young Jin Kang received the B.S. and M.S. degrees in the Department of Electronic and Electrical Engineering from Hongik University, Seoul, Korea, in 2012 and 2014, respectively. He is currently with Fairchild Semiconductor, Bucheon, Korea. His research interests include the device characterization and TCAD simulation.



Jonghwa Kim received the B.S. degree in the School of Electronic Engineering from Kookmin University, Seoul, Korea, in 2014. He is currently pursuing the M.S. degree, and his research interests include characterization and modeling for reliability of III-V compound semiconductor devices and oxide thin-film transistors.

Jungmok Kim received the B.S. degree in the School of Electronic Engineering from Kookmin University, Seoul, Korea, in 2015, where he is currently pursuing the M.S. degree. His current research interests include characterization and modeling for reliabilities for III-V compound.

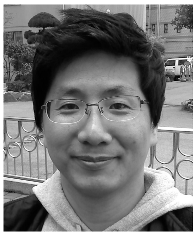
Sung-Jin Choi received the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2012. He is currently an Assistant Professor of the School of Electrical Engineering, Kookmin University, Seoul, Korea.

Dong Myong Kim (S'86–M'88) received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1986 and 1988, respectively, and the Ph.D. degree in electrical engineering from University of Minnesota, Twin Cities, MN, in 1993. From Feb. 1988 to August 1989, he was with Division of Electronic Engineering at Korea Institute of Science and Technology (KIST), Seoul, Korea where he worked on the characterization and modeling of microwave devices and integrated circuits. Since March 1993. He is a Professor of the School of Electrical Engineering, Kookmin University,Seoul, Korea. He also serves as a Special Lecturer for Semiconductor Physics and Devices at Samsung Electronics Co., Hwasung, Korea since April 2002. His current research interest includes design, fabrication, characterization, and modeling of nanostructure silicon devices, thin film transistors, bio-sensors, III-V compound semiconductor devices, volatile and nonvolatile memories, and CMOS RF circuits.

Ho-Young Cha received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1996 and 1999, respectively, and the Ph.D. degree in electrical and computer engineering from Cornell University, Ithaca, NY, in 2004. He was a Postdoctoral Research Associate with Cornell University until 2005 where he focused on design and fabrication of SiC and GaN electronic devices and GaN nanowires. He was with the General Electric Global Research Center, Niskayuna, NY, from 2005 to 2007, developing wide-bandgap semiconductor sensors and high power devices. Since

2007, he has been with Hongik University, Seoul, as an Associate Professor of the School of Electronic and Electrical Engineering. His research interests include wide bandgap semiconductor devices. He has authored over 70 publications in his research area.

Hyungtak Kim received the B.S. degree in Electrical Engineering from Seoul National University, Seoul, Korea and the M.S./Ph.D. degree in Electrical and Computer Engineering from Cornell University, Ithaca, New York, U.S.A., in 1996 and 2003, respectively. He is currently an associate professor of the school of electronic and electrical engineering at Hongik University, Seoul, Korea. His research interests include reliability physics of wide bandgap semiconductor devices and novel TFTs. During his graduate program, he performed comprehensive research on GaN-based hetero-structure field effect transistors for high frequency power application. Prior to joining with Hongik University, he spent 4 years developing CMOS devices and process integration for 60nm DRAM technology as a senior engineer in the semiconductor R&D center at Samsung Electronics, Co. Ltd.



Dae Hwan Kim (M’08-SM’12) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2002, respectively. From 2002 to 2005, he was with Samsung Electronics Company, Ltd., Kyung ki-Do, Korea where he contributed to design and development of 92-nm DDR DRAM and 80-nm DDR2 DRAM. In 2005, he joined in the School of Electrical Engineering at Kookmin University, Seoul where he is working as an Associate Professor. He has authored and coauthored more than 270 research publications and patents. His research interests are nanoscale CMOS devices and integrated circuits, metal oxide and organic thin-film transistors, biosensor devices, exploratory logic and memory devices, energy-efficient nano-ICs, and Si quantum devices. He has also worked on characterization, modeling, and circuit design for reliability of CMOS devices, thin-film transistors, display, biosensors, and neuromorphic systems. He is a senior member of IEEE, Society for Information Display, Materials Research Society, and Institute of Electronics Engineers of Korea.