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Comparative Analysis on Positive Bias Stress-Induced Instability under High V_{GS}/Low V_{DS} and Low V_{GS}/High V_{DS} in Amorphous InGaZnO Thin-Film Transistors

Hara Kang, Jun Tae Jang, Jonghwa Kim, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim*

Abstract—**Positive bias stress-induced instability in amorphous indium-gallium-zinc-oxide (a-IGZO) bottom-gate thin-film transistors (TFTs) was investigated under high V_{GS}/low V_{DS} and low V_{GS}/high V_{DS} stress conditions through incorporating a forward/reverse V_{GS} sweep and a low/high V_{DS} read-out conditions. Our results showed that the electron trapping into the gate insulator dominantly occurs when high V_{GS}/low V_{DS} stress is applied. On the other hand, when low V_{GS}/high V_{DS} stress is applied, it was found that holes are uniformly trapped into the etch stopper and electrons are locally trapped into the gate insulator simultaneously. During a recovery after the high V_{GS}/low V_{DS} stress, the trapped electrons were detrapped from the gate insulator. In the case of recovery after the low V_{GS}/high V_{DS} stress, it was observed that the electrons in the gate insulator diffuse to a direction toward the source electrode and the holes were detrapped to out of the etch stopper. Also, we found that the potential profile in the a-IGZO bottom-gate TFT becomes complicatedly modulated during the positive V_{GS}/V_{DS} stress and the recovery causing various threshold voltages and subthreshold swings under various read-out conditions, and this modulation needs to be fully considered in the design of oxide TFT-based active matrix organic light emitting diode display backplane.**

Index Terms—**a-IGZO TFT, driving condition of AMOLED, positive bias stress, charge trapping, electron-hole pair generation**

I. INTRODUCTION

Amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistor (TFT) is actively in use as a promising display device due to many attractive advantages as follows. The a-IGZO TFT has a high mobility along with the good large-area uniformity which is suitable for large-area, high frame-rate, and high resolution display backplane compared with amorphous Si TFT or organic TFT. Moreover, the a-IGZO TFT enables flexible display and transparent display due to its compatibility with a low temperature process and transparency in the visible light range while it still has a high on/off current ratio and good subthreshold swing (SS) [1, 2].

Despite the fact that the a-IGZO TFT enhance displaying industries with its various advantages, the stability under a bias stress still remains as a challenging issue, especially from the viewpoint of mass production. The positive bias stress (PBS)-induced instability is of special importance in terms of the active matrix organic light emitting diode (AMOLED) displays because applying both the positive gate-to-source voltage (V_{GS}) and positive drain-to-source voltage (V_{DS}) corresponds with the driving condition of AMOLED [3-5]. Although various V_{GS}/V_{DS} conditions including the high V_{DS} need to be investigated for optimizing the driving scheme of the AMOLED backplane driven by a-IGZO TFTs, most of the previous works have been focused on the cases of

Manuscript received Apr. 20, 2015; accepted Aug. 27, 2015
School of Electronic Engineering, Kookmin University, Seoul, Korea
E-mail : drlife@kookmin.ac.kr

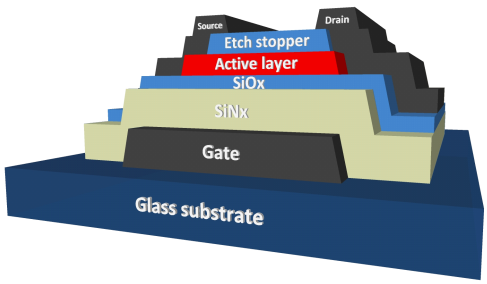

Fig. 1. The a-IGZO TFT with the inverted staggered bottom-gate top-ES structure

V_{GS} higher than or equal to V_{DS} [6-8].

In this paper, we investigated the PBS instability of the a-IGZO TFT with an inverted staggered bottom-gate top-etch stopper under two stress conditions, i.e., high V_{GS}/low V_{DS} and low V_{GS}/high V_{DS}, and then compared them each other combining the forward/reverse V_{GS} sweeps and the high/low V_{DS} read-out conditions. The main method used in this work was to reproduce the measured electrical characteristics via technology computer-aided-design (TCAD) device simulation. As a cosequence, it was verified that the electron trapping into the gate insulator (GI) was dominating in the high V_{GS}/low V_{DS} stress whereas the local electron trapping into GI near the drain and hole trapping into etch stopper (ES) layer were dominant in low V_{GS}/high V_{DS} stress.

Consequentially, we strongly believe that our results can contribute to enhancing and optimizing the driving scheme of a-IGZO TFTs-driven AMOLED from the viewpoint of PBS-induced instability.

II. Device Structure, Electrical Characteristics, and Measurement Setup

The a-IGZO TFTs with the inverted staggered bottom-gate top-ES structure were fabricated on a glass substrate as shown in Fig. 1. The detailed process is as follows. Molybdenum electrode was deposited on the glass substrate by using a radio frequency sputtering process and patterned by dry etching. Then, the GI made up of 400 nm/50 nm-thick SiNx/SiOx bilayer was deposited by plasma-enhanced chemical-vapor-deposition (PECVD). The 50-nm-thick a-IGZO thin-film was dc sputter-deposited with power of 3 kW at room temperature in gas mixture of Ar/O_2=35/63 at sccm in which its atomic ratio is In:Ga:Zn=2:2:1. The active layer was then patterned by wet etching with diluted HF. Subsequently, the 50-nm-thick SiO_x was formed as the ES layer by PECVD and dry etch patterning. Molybdenum was then dc sputter-deposited and patterned by dry etching as the source/drain electrodes. Subsequently, the 100-nm-thick SiO_x was the PECVD-deposited as a passivation layer. Lastly, the post annealing process was performed at 250°C for 1 hour.

The fabricated TFT has geometrical parameters, such as an equivalent oxide thickness of GI T_{OX}=258 nm, the active layer thickness T_{IGZO}=50 nm, the channel length L=50 μm, the gate-to-S/D overlap length L_{OV}=15 μm, and the channel width W=25 μm. The electrical properties of the a-IGZO TFT are the threshold voltage (V_T)=0.4 V, SS=387 mV/dec, field-effect mobility $\mu_{FE,lin}$=7.9 cm^2/Vs (linear region), and $\mu_{FE,sat}$=11.06 cm^2/Vs (saturation region).

The current-voltage transfer curves were measured at room temperature in dark ambient with the Agilent 4156C precision semiconductor parameter analyzer while the Atlas-2D was used for TCAD device simulation [13].

The PBS was measured under two stress conditions. The high V_{GS}/low V_{DS} stress was measured under 30 V/10 V whereas the low V_{GS}/high V_{DS} was measured under 10 V/30 V during the same stress time t_{STR}=5000 sec. In addition, the recovery measurement was conducted during the recovery time, which was set up as t_{REC}=2000 sec and all electrodes were tied to a ground during the t_{REC}.

Also, the transfer curve was measured with two kinds of V_{GS} sweep modes, i.e., forward and reverse V_{GS} sweeps, and with two kinds of V_{DS} conditions, i.e., low and high V_{DS} read-outs, respectively.

The forward V_{GS} sweep was to set the positions of source and drain electrodes during the read-out of transfer curve to the same as those of during the PBS. Contrastively, the reverse V_{GS} sweep signifies exchanging the positions of source and drain electrodes during the read-out in comparison with those of during the PBS.

On the other hand, the high V_{DS}/low V_{DS} read-out transfer curves were acquired under V_{DS}=10.1/0.1 V conditions, which individually corresponds to the saturation and linear regions.

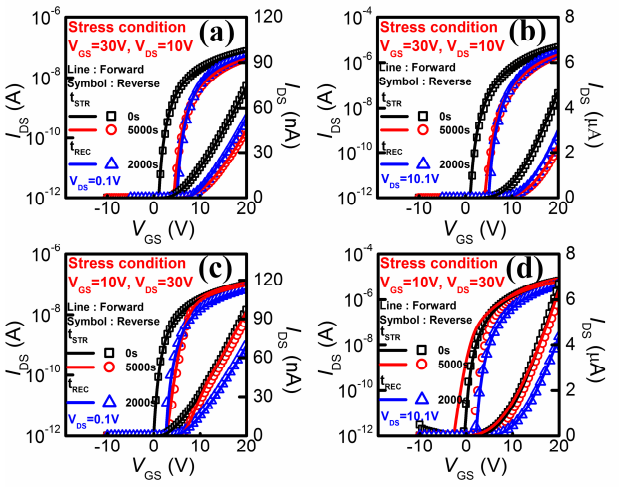

Fig. 2. The PBS and recovery time-evolutions of measured transfer characteristics (a) The V_{DS}=0.1 V (linear region) read-out under high V_{GS}/low V_{DS} PBS, (b) the V_{DS}=10.1 V (saturation region) read-out under high V_{GS}/low V_{DS} PBS, (c) the V_{DS}=0.1 V (linear region) read-out under low V_{GS}/high V_{DS} PBS, (d) the V_{DS}=10.1 V (saturation region) read-out under low V_{GS}/high V_{DS} PBS

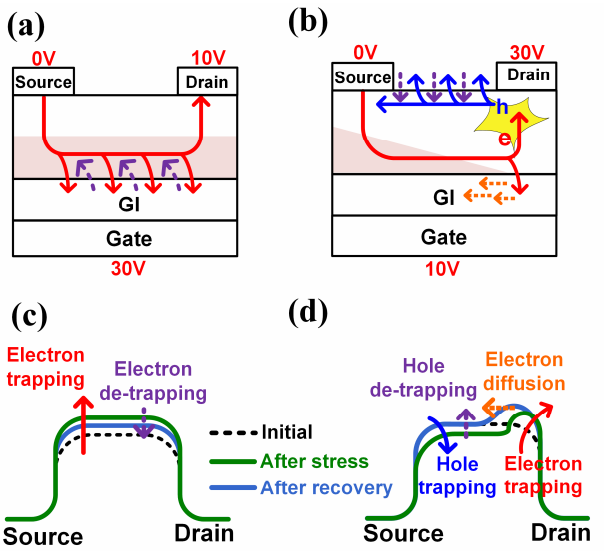

Fig. 3. Schematics illustrating the PBS instability during t_{STR} and t_{REC} under (a) high V_{GS}/low V_{DS}, (b) low V_{GS}/high V_{DS} PBS conditions. Schematics illustrating the lateral energy band diagrams and electron potential profiles during t_{STR} and t_{REC} under (a) high V_{GS}/low V_{DS}, (b) low V_{GS}/high V_{DS} PBS conditions

III. Result & Discussion

Fig. 2 shows the measured transfer curves. It is noteworthy that the t_{STR}/t_{REC}-evolutions of transfer curves were observed in complicated and different ways depending on all of the PBS (V_{GS}/V_{DS}=30 V/10 V and V_{GS}/V_{DS}=10 V/30 V), V_{GS} sweep (forward and reverse), and V_{DS} read-out (V_{DS}=10.1/0.1 V) conditions. These time-dependences of transfer curves need to be carefully investigated to understand the instability mechanisms in the operation of IGZO-driven AMOLED.

As shown in Fig. 2(a) and (b), the case of V_{GS}/V_{DS}=30 V/10 V stress condition, the positive V_T shift is observed during t_{STR} regardless of the V_{DS} read-out conditions. Moreover, there is no observed difference between the forward and reverse V_{GS} sweeps. Based upon such result, it can be inferred that the local V_T near source is identically increased to that of the drain during the t_{STR}. These phenomena have been frequently observed by other research groups and analyzed by uniformly electron trapping into the GI or the interface between GI and active layer [10, 11]. Similarly, in our case, electrons can be energetically enhanced by a high vertical electric field and be uniformly trapped into the GI as indicted by solid red arrows in Fig. 3(a), raising the electron potential profile during the t_{STR} (solid red arrow in Fig. 3(c)). Consequently, the positive V_T shift without SS degradation is observed in all cases of the read-out conditions. The transfer curve is also slightly shifted to a negative V_{GS} direction during the t_{REC} as shown in Fig. 2(a) and (b), which can be attributed to the electron detrapping from GI as illustrated by dashed purple arrows in Fig. 3(a) and (c).

However, in term of V_{GS}/V_{DS}=10 V/30 V stress condition, the measured transfer curves obviously have different t_{STR}/t_{REC}-dependences in each read-out condition as represented in Fig. 2(c) and (d). In the case of the V_{DS}=0.1 V read-out condition, the difference between the forward and reverse V_{GS} sweeps was negligible and both the SS degradation and the slightly positive V_T shift with hump phenomenon were clearly observed after t_{STR}=5000 sec as shown in Fig. 2(c). On the contrary, in case of the V_{DS}=10.1 V read-out condition, there is definite distinction between the forward and reverse V_{GS} sweeps. The positive V_T shift with SS degradation is shown in reverse sweep; however, the forward V_{GS} sweep has the result of negative V_T shift with SS degradation as shown in Fig. 2(d). That is to say, opposite direction of the V_T shift is caused only under the condition of V_{DS}=10.1 V read-out (Fig. 2(d)), and this phenomenon indicates the asymmetric V_T is formed in

each near the source and drain after the stress. Additionally, SS degradation is the clue to predict occurring of the asymmetric degradation [9]. We have come to understand abovementioned phenomena as follows. The local V_T near the source is lowered whereas the local V_T near the drain becomes higher during t_{STR} as a consequence of the local electron trapping into GI near the drain. In the low V_{GS}/high V_{DS} stress condition, the high local lateral electric field is formed near the drain because of high drain voltage. Therefore, electron, the mobile carrier, is rapidly accelerated by the high electric field and then can obtain the large kinetic energy, which is large enough to generate the electron-hole pair caused by the impact ionization [7, 12] or by the interaction between the valence band and subgap traps under mid-gap of a-IGZO. Accordingly, the electrons can be locally trapped into GI only near the drain (solid red arrow in Fig. 3(b)); hence, the local V_T as well as the electron potential near the drain becomes higher than the initial (solid red arrow in Fig. 3(d)). Generated holes can drift to the source under the influence of the lateral electric field so they can be quite uniformly trapped into ES (solid blue arrow in Fig. 3(b)), i.e., the V_T near the source becomes lower during the t_{STR} (solid blue arrow in Fig. 3(d)). Consequently, the lateral energy band of active layer is asymmetrically formed as indicated in Fig. 3(d) after the low V_{GS}/high V_{DS} stress. This phenomenon could be distinguished only in V_{DS}=10.1 V read-out and it can bring about the different characteristic in each read-out condition because each condition has different V_T depending not only on the forward and reverse V_{GS} sweeps but also how high V_{DS} is applied. When correlating between the before-mentioned analysis and measured data, the negative V_T shift is observed only under the forward high V_{DS} read-out because this condition can completely remove the locally high electron potential barrier near the drain due to applying high V_{DS}.

After t_{REC}=2000 s under V_{GS}/V_{DS}=10 V/30 V stress condition, we could see all read-out transfer curves move towards positive V_{GS} direction. Especially, in the case of measured transfer curve under the forward and V_{DS}=10.1V read-out condition, the negative V_T shift after the stress showed the complete recovery. More specifically, the transfer curve moved more towards the positive direction compared to the initial condition, that is to say, there is no difference between the forward and reverse V_{GS} sweeps. Therefore, it should be deduced that the recovery characteristic is caused by hole detrapping (dashed purple arrows in Fig. 3(b) and (d)). Furthermore, we consider the disappearance of the difference between the forward and reverse V_{GS} sweep transfer curves were consequent on the electric field-enhanced diffusion of trapped electrons in GI towards the source due not only to the electron concentration difference in GI, but also to the built-in electric field resulting from the asymmetric potential distribution as well (dashed orange arrows in Fig. 3(b) and (d)). However, the electron movement during the t_{REC} needs to be further investigated and proven.

IV. TCAD SIMULATION

In Fig. 3, we established the qualitative model on the t_{STR}/t_{REC}-dependence of transfer curves in all cases of PBS, V_{GS} sweep, and V_{DS} read-out conditions. In addition, we conducted the TCAD device simulation in order to validate our model quantitatively. For a precise and reasonable analysis, the subgap trap model of a-IGZO TFT [14] was employed as follows:

$$g_A(E) = g_{DA}(E) + g_{TA}(E)$$
$$= N_{DA} \times \exp\left(\frac{E - E_C}{kT_{DA}}\right) + N_{TA} \times \exp\left(\frac{E - E_C}{kT_{TA}}\right)$$
$$g_{TD}(E) = N_{TD} \times \exp\left(\frac{E_V - E}{kT_{TD}}\right).$$

g_A(E), which indicates the accepter-like states near the conduction band, is composed of exponential tail states (N_{DA}, kT_{TA}) and exponential deep states (N_{TA}, kT_{TA}). Also, g_D(E) indicating the donor-like states near the valence band is expressed by an exponential function (N_{TD}, kT_{TD}). The parameters utilized in the TCAD simulation are summarized in Table 1 [15]. The TCAD parameters used in simulation are reasonable because the simulated transfer curves accurately correspond to the measured initial transfer curves (black solid and black dashed lines in Figs. 4 and 5).

In order to verify our proposed model in V_{GS}/V_{DS}= 30 V/10 V stress condition, simulation was conducted by uniformly putting the electron fixed charge in GI. As a

Table 1. The parameters used in TCAD simulation

E_g [eV]	N_C [cm^{-3}]	N_V [cm^{-3}]	N_{SD} [cm^{-3}]	μ_n [cm^2/Vs]	
3.2	$1x10^{18}$	$2x10^{19}$	$1.2x10^{16}$	55	
N_{TA} [$cm^{-3}eV^{-1}$]	kT_{TA} [ev]	N_{DA} [$cm^{-3}eV^{-1}$]	kT_{DA} [ev]	N_{TD} [$cm^{-3}eV^{-1}$]	kT_{TD} [ev]
$9x10^{19}$	0.02	$1x10^{18}$	0.16	$1x10^{18}$	0.27

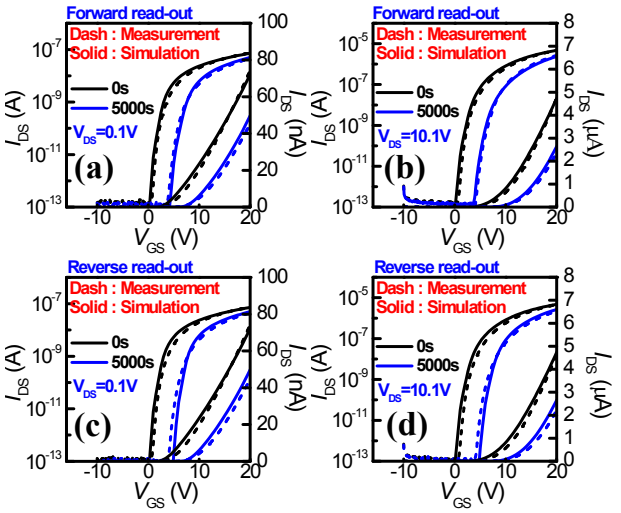

Fig. 4. Measured and simulated transfer curves under high V_{GS}/low V_{DS} PBS (a) The forward V_{DS}=0.1 V read-out, (b) the forward V_{DS}=10.1 V read-out, (c) the reverse V_{DS}=0.1 V read-out, (d) the reverse V_{DS}=10.1 V read-out

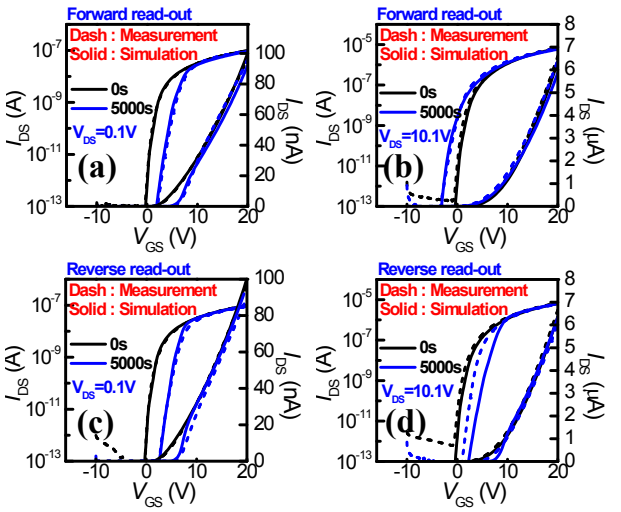

Fig. 5. Measured and simulated transfer curves under low V_{GS}/high V_{DS} PBS (a) The forward V_{DS}=0.1 V read-out, (b) the forward V_{DS}=10.1 V read-out, (c) the reverse V_{DS}=0.1 V read-out, (d) the reverse V_{DS}=10.1 V read-out

result, simulated transfer curves were well reproduced under all case of read-out conditions that is identical to measurement transfer curves such as solid blue lines and dashed blue lines in Fig. 4. Moreover, we were able to figure out that trapped electron charge density during the t_{STR}=5000 sec is $4x10^{11}$ cm^{-2} which is in the range of reasonable value.

In order to verify our model in V_{GS}/V_{DS}=10 V/30 V stress condition, the electrons were input from the drain edge to the source direction with a distance of 1 μm in the GI and hole were uniformly put into ES from the source edge to drain edge. Consequently, it should be emphasized that there is verified correlation between the measured data and simulated data. Also, we find out that $4.7x10^{11}$ cm^{-2} of electrons and $2x10^{11}$ cm^{-2} of holes were trapped respectively during the t_{STR}=5000 sec.

Through the TCAD simulation, measurement result is reproduced under the two stress conditions which are high V_{GS}/low V_{DS} and low V_{GS}/high V_{DS} with all measurement read-out conditions. Therefore, it is proved that our instability model is reasonable.

V. CONCLUSIONS

We have analyzed the PBS-induced instability under high V_{GS}/low V_{DS} and low V_{GS}/high V_{DS} conditions in the bottom gate a-IGZO TFTs with an emphasis on the forward/reverse and a low/high V_{DS} read-out conditions. In case of high V_{GS}/low V_{DS} stress condition, the electrons are uniformly trapped into gate insulator by the vertical electric field. On the other hands, in case of low V_{GS}/high V_{DS}, it was dominated by the local trapping of electron/hole into GI/ES and the local potential barriers were complicatedly modulated by the variations of not only the position of the source/drain but also the value of V_{DS} under an individual read-out condition. The proposed instability model was meticulously verified by TCAD simulation under all the stress conditions and read-outs.

During the t_{REC}, it was observed and analyzed that electron detrapping occurs after high V_{GS}/low V_{DS} stress whereas electron diffusion and hole detrapping primarily occurs after low V_{GS}/high V_{DS} stress; however, further studies should be required.

Consequentially, we believe that our results would provide the informative implications of optimizing the driving scheme for the display pixel in the amorphous oxide TFT-driven AMOLED backplanes.

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REFERENCES

[1] K. Nomura, *et al.*, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, Vol.432, p. 488, Nov., 2004.

[2] E. M. C. Fortunato, *et al*., "High mobility indium free amorphous oxide thin film transistors" *Appl. Phys. Lett.*, Vol.92, No.22, p. 590, Jun., 2008.

[3] J.-S. Park, "Oxide TFTs for AMOLED TVs," *Information Display*, Vol.29, No.2, p. 16, 2013.

[4] J. F. Wager, "Flat-Panel-Display Backplanes: LPTS or IGZO for AMLCDs or AMOLED Displays?," *Information Display*, Vol.30, No.2, p. 26, 2014.

[5] W.-J. Nam, *et al.* "55-inch OLED TV using InGaZnO TFTs with WRGB pixel Dising," *SID Symposium Digest.*, Vol.44, No.1, p. 243, Jun. 2013.

[6] S. M. Lee, *et al.*, "Device instability under high gate and drain biases in InGaZnO thin film transistors," *IEEE Trans. Device Mater, Reliab.*, Vol.14, No.1, p. 471, Mar., 2014.

[7] C.-Y. Jeong, *et al.*, "A study on the degradation mechanism of InGaZnO thin-film transistors under simultaneous gate and drain bias stresses based on the electronic trap characterization," *Semicond. Sci. and Technol*., Vol.29, No.4, p. 045023, Mar., 2014.

[8] S. Urakawa, *et al.*, "Thermal analysis of amorphous oxide thin-film transistor degraded by combination of joule heating and hot carrier effect," *Appl. Phys. Lett.*, Vol.102, No.5, p. 053506, Feb., 2013.

[9] T.-Y. Hsieh, *et al.*, "Investigating the Drain-Bias-Induced Degradation Behavior Under Ligh Illumination for InGaZnO Thin-Film Transistors," *IEEE Electron Device Lett.*, Vol.33, No.7, p. 1000-1002, Jul., 2012.

[10] J.-M. Lee, *et al*., "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," *Appl. Phys. Lett.*, Vol.93, No.9, p. 093504, Sep., 2008.

[11] C. P. T. Nguyen, *et al.*, "Bias–stress-induced threshold voltage shift dependence of negative charge trapping in the amorphous indium tin zinc oxide thin-film transistors," *Semicond. Sci. Technol.* Vol.28, No.10, p. 105014, Aug., 2013.

[12] S. H. Choi and M. K. Han, "Effect of channel widths on negative shift of threshold voltage, including stress-induced hump phenomenon in InGaZnO thin-film transistors under high-gate and drain bias stress," *Appl. Phys. Lett.*, Vol.100, No.4, p. 043503, Jan., 2012.

[13] Atlas User's Manual, Silvaco, Santa Clara, CA, 2014.

[14] Y. Kim, *et al.*, "Amorphous InGaZnO Thin-Film Transistor-Part 1: Complete Extraction of Density of States Over the Full subband-Gap Energy Range," *IEEE Trans. Electron Devices*, Vol.56, No.10, p. 2689, Oct. 2012.

[15] E. K.-H. Yu, *et at.*, "Density of states of amorphous In-Ga-Zn-O from electrical and optical characterization," *Appl. Phys. Lett.*, Vol.116, No.15, p. 154505, Oct. 2014.

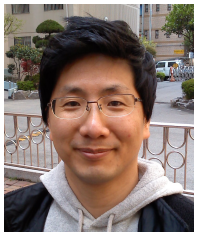
Hara Kang received the B.S. degree in the School of Electronic engineering from Kookmin University, Seoul, Korea, in 2015. She is currently pursuing the M.S. degree, and her current research interests include amorphous oxide thin-film transistor and nonvolatile memory devices.

Jun Tae Jang received in the B.S. degree from the School of Electronic Engineering, Kookmin University, Seoul, Korea, in 2014, where he is currently pursuing the M.S. degree in electrical engineering. His current research interests include amorphous oxide thin-film transistor and nonvolatile memory devices.

Jonghwa Kim received the B.S. degree in the School of Electronic Engineering from Kookmin University, Seoul, Korea, in 2014. He is currently pursuing the M.S. degree, and his research interests include characterization and modeling for reliability of III-V compound semiconductor devices.

Sung-Jin Choi received the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2012. He is currently an Assistant Professor of the School of Electrical Engineering, Kookmin University, Seoul, Korea.

Dong Myong Kim received the B.S. (*magna cum laude*) and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1986 and 1988, respectively, and the Ph.D. degree in electrical engineering from University of Minnesota, Twin Cities, MN, in 1993. From Feb. 1988 to August 1989, he was with Division of Electronic Engineering at Korea Institute of Science and Technology (KIST), Seoul, Korea, where he worked on the characterization and modeling of microwave devices and integrated circuits. Since March 1993, he has been with the School of Electrical Engineering, Kookmin University, Seoul, Korea. He is also serving as a Special Lecturer for Semiconductor Physics and Devices at Samsung Electronics Co., Hwasung, Korea since April 2002. His current research interest includes design, fabrication, characterization, and modeling of nanostructure silicon devices, thin film transistors, bio-sensors, III-V compound semiconductor devices, volatile and nonvolatile memories, and CMOS RF circuits.



Dae Hwan Kim received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2002, respectively. From 2002 to 2005, he was with Samsung Electronics Company, Ltd., Kyung ki-Do, Korea, where he contributed to the design and development of 92-nm DDR DRAM and 80-nm DDR2 DRAM. In 2005, he joined the School of Electrical Engineering, Kookmin University, Seoul, where he is currently an Associate Professor. He has authored or coauthored more than 270 research publications and patents. His current research interests are nanoscale CMOS devices and integrated circuits, metal oxide and organic thin-film transistors, biosensor devices, neuromorphic devices and circuits, exploratory logic and memory devices, energy-efficient nano-ICs, and Si quantum devices. He is a senior member of IEEE, and also a member of Society for Information Display, the Electrochemical Society, Materials Research Society, the Korean Information Display Society, and the Institute of Electronics and Information Engineers of Korea.