## Experimental Decomposition of the Positive Gate-bias Temperature Stressinduced Instability and Its Modeling in InGaZnO Thin-film Transistors

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The positive gate-bias temperature stress (PBTS)-induced instability in top gate self-aligned coplanar InGaZnO thin-film transistors (TFTs)<sup>1,2</sup> is experimentally decomposed into contributions of distinct mechanisms by combining the stress-time-divided measurements and the extraction of subgap density-of-states (DOS) from the optical response of C-V characteristics. It is found that a total threshold voltage shift ( $\Delta V_{T,tot}$ ) under PBTS is decomposed into three mechanisms: 1) increase of DOS due to excess oxygen in the active region ( $\Delta V_{T,DOS}$ ), 2) shallow ( $\Delta V_{T,shallow}$ ) and 3) deep charge trapping in the gate insulator components ( $\Delta V_{T,deep}$ ). The procedure of decomposition is illustrated in Fig. 1(a)~(c) and experimentally decomposed  $\Delta V_{T,DOS}$ ,  $\Delta V_{T,shallow}$ , and  $\Delta V_{T,deep}$  are plotted as a function of the stress time ( $t_{str}$ ), as denoted by the symbols in Fig. 1(d). Fig. 1(e) shows the contribution percentage of each component to the PBTS  $\Delta V_{T,tot}$  after  $t_{str}=10^4$  s at varying temperatures of 27, 60, 100 °C. The lines in Fig. 1(d) show that all of  $\Delta V_{T,DOS}$ ,  $\Delta V_{T,shallow}$ , and  $\Delta V_{T,deep}$  are well fitted with the stretched-exponential (SE) functions with individual parameters and the  $\Delta V_{T,tot}$ (t) is well described by the superposition of multiple SE functions. The effective activation energy is found to be 0.75, 0.40, 0.90 eV for the  $\Delta V_{T,DOS}$ ,  $\Delta V_{T,shallow}$ , and  $\Delta V_{T,deep}$ , respectively.

Our results can be easily applied universally to any device with any stress conditions, along with guidelines for joint optimization of the dielectrics, the active layer, and the interfaces towards ultimate PBTS stability.



Fig. 1. Schematics illustrating (a) the procedure of decomposition of PBTS ΔV<sub>T,tot</sub>, (b) the stress-timedivided measurement, and (c) finally decomposed ΔV<sub>T</sub> as the function of t<sub>str</sub>. (d) Experimentally decomposed ΔV<sub>T</sub>(t<sub>str</sub>) (symbols) and model fitted with the SE function (lines). (e) Contribution percentage of each ΔV<sub>T</sub> components at several temperatures.

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## References

1. J. U. Bae et al., *SID'13 Technical Digest*, vol. 44, p. 89 (2013). 2. S. Oh et al., *IEEE Electron Device Lett.*, 35, 1037 (2014).