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Synaptic devices based on two-dimensional layered single-crystal chromium thiophosphate (CrPS₄)

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Abstract

Two-dimensional (2D) van der Waals (vdW) materials have recently attracted considerable attention due to their excellent electrical and mechanical properties. TmPS_x (where Tm = a transition metal), which is a new class of 2D vdW materials, is expected to show various physical phenomena depending on the Tm used. In this paper, the unprecedented synaptic behavior of a vertical Ag/CrPS₄/Au capacitor structure, where CrPS₄ is a single-crystalline 2D vdW layer, is reported. Multi-stable resistive states were obtained using an external voltage of less than 0.3 V. Both short-term plasticity and long-term potentiation were observed by controlling the interval of the external voltage pulse. Simple mechanical exfoliation was used to develop a synaptic device based on a very thin CrPS₄ layer with a thickness of ~17 nm. Therefore, it was demonstrated that vertical Ag/CrPS₄/Au capacitors could be promising inorganic synaptic devices compatible with next-generation, flexible neuromorphic technologies.

Introduction

Conductive-bridge random access memory (CBRAM), which exploits electrochemically active ion migration, has been proposed as a potential candidate for future non-volatile memory applications^{1–3}. In metal oxide and chalcogenide electrolyte materials that display both ionic and electronic conductivity, ion migration is associated with reduction and oxidation processes. These processes result in large electrical conductance changes, characteristic of ion-controlled memristors, with the application of an external bias^{3–5}. The development of reliable memristor devices capable of storing multiple states of information has led to new applications, including neuromorphic computing^{6–8}.

A synapse can be regarded as a two-terminal device, the synaptic weight of which can be dynamically modified using consecutive spikes, which is similar to an ion-controlled memristor^{9–11}. Learning, forgetting, and memorization events in the human brain can be described using the modulation of the synaptic weights between pre-neurons and post-neurons. This phenomenon is known as synaptic plasticity. An ion-controlled memristor can mimic short-term plasticity (STP) and long-term potentiation (LTP) via the electrically induced oxidation and reduction of ions. STP is achieved through the temporal enhancement of a synaptic connection, while repeated stimulation causes a permanent change in the connection, leading to LTP^{12–16}. In the human brain, 10¹⁵ synapses consume only ~10 W per synaptic event with a duration of ~100 ms, and hence, a low energy consumption and an extremely small size are required for a synaptic memristor device to be applied in a neuromorphic system^{9,10}.

Two-dimensional (2D) layered van der Waals (vdW) materials, such as MoS₂ and WS₂, are considered to be

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promising electrolytes for use in extremely thin CBRAM devices because they can be exfoliated to atomic layers. Recently, Bailey et al. reported ion migration-based synaptic memristor devices containing 2D layered vdW materials¹⁷. Their surface oxide layers with a sub-nanometer thickness exhibited an excellent synaptic plasticity and learning capacity in response to ~ 100 -mV-level stimuli comparable to neuron spikes, which is thought to result from the formation of electrically induced conductive bridges consisting of oxygen vacancies¹⁷. However, the 2D layered vdW materials in the $\text{MoO}_x/\text{MoS}_2$ and WO_x/WS_2 heterostructure devices acted as only supporting materials and not as active layers. CBRAM devices utilizing ion migration along the thickness directions in 2D layered vdW materials have not yet been demonstrated.

In this paper, CBRAM devices that use cation migration along the thickness direction of a new class of 2D layered vdW materials, which show synaptic plasticity and learning function without the formation of oxygen-deficient surface oxides, is proposed. An electrochemically active metal, such as Ag or Cu, was used for the operation of the synaptic memristor based on electrically controlled cation migration^{18–20}. A 2D layered chromium thiophosphate (CrPS_4) single crystal was used as an electrolyte material for cation migration, similar to Ag_2S , Cu_2S , and GeS_2 ^{18,20–22}. Moreover, low-dimensional devices emulating biological synapses for neuromorphic systems were achieved through control of the thickness using a mechanical exfoliation method.

Materials and methods

Crystal synthesis

Single-crystalline CrPS_4 was grown from high-purity Cr, P, and S powders using a chemical vapor transport method. The powders were mixed and sealed in a quartz ampoule under vacuum, which was then placed into a horizontal 2-zone furnace, where the target temperatures were set to 690°C (hot zone) and 650°C (cold zone) for 9 days. The stoichiometries of all the as-grown single crystals were analyzed using a scanning electron microscope (SEM) (COXEM COXI EM30) with an energy-dispersive X-ray spectrometer (Bruker Quantax 100).

Device fabrication

The $\text{Ag}/\text{CrPS}_4/\text{Au}$, $\text{Cu}/\text{CrPS}_4/\text{Au}$, $\text{Au}/\text{CrPS}_4/\text{Au}$, and $\text{Pt}/\text{CrPS}_4/\text{Au}$ cross-point devices with a $3 \times 3 \mu\text{m}^2$ contact area were fabricated on SiO_2 substrates with pad electrodes that were pre-patterned using a photolithography method. Mechanically exfoliated CrPS_4 samples on poly (methyl methacrylate) (PMMA) with different thicknesses were transferred to Au bottom electrodes with a $3 \mu\text{m}$ width on SiO_2 substrates. Ag, Cu, and Au top electrodes, each with a 120 nm thickness and a $3 \mu\text{m}$ width, were

deposited on the CrPS_4 sample using e-beam evaporation. The Pt top electrode was deposited on the CrPS_4 sample through direct-current (DC) sputtering in an Ar atmosphere. All the electrodes were patterned using e-beam lithography and a lift-off process.

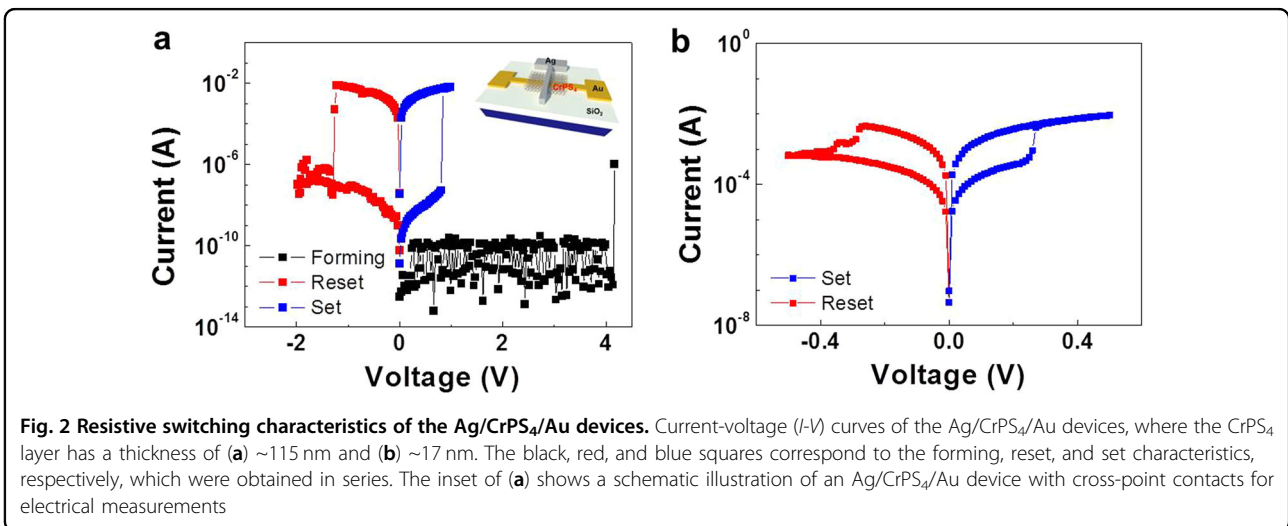
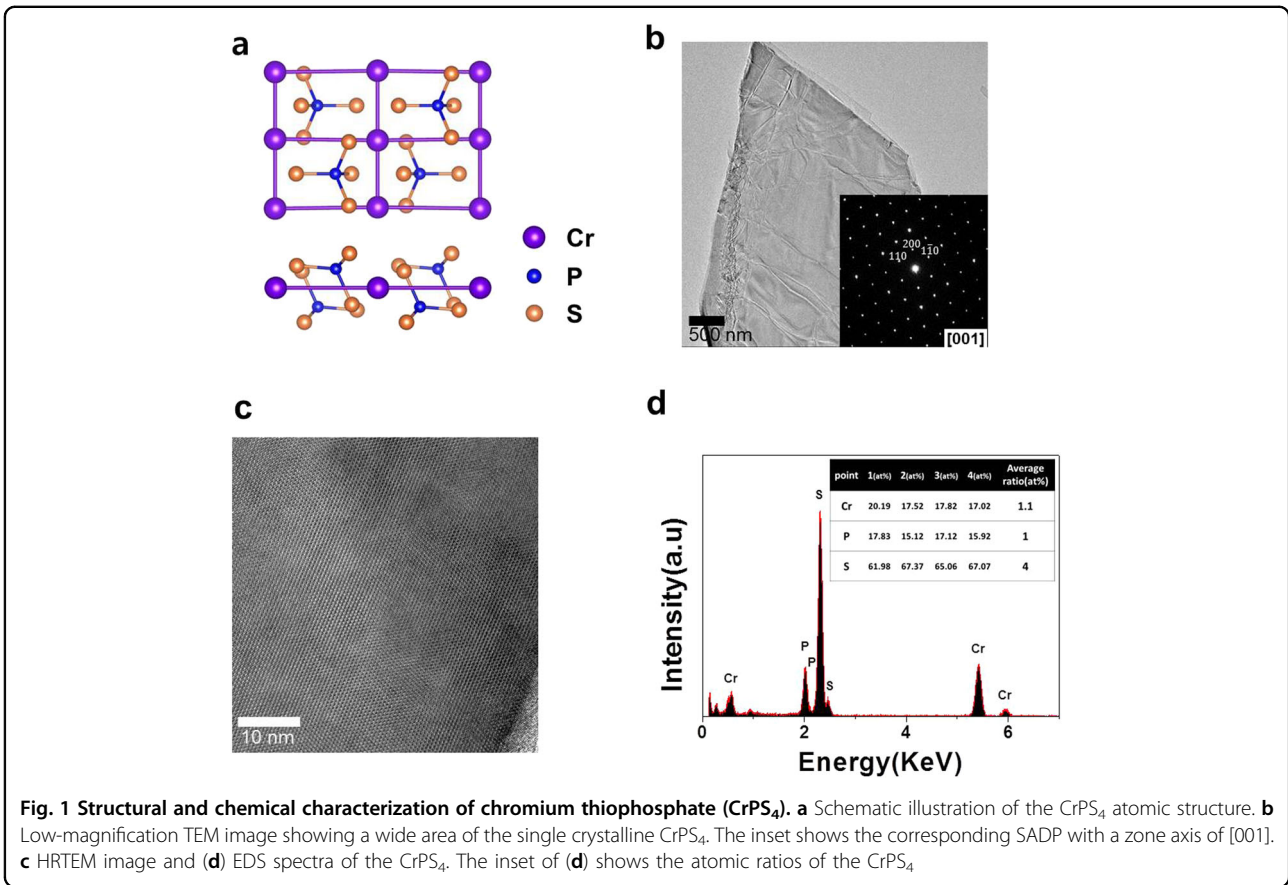
Characterization

The electrical properties of the memristor devices were investigated using the I - V sweep mode at room temperature using a semiconductor parameter analyzer (Agilent 4156B). The synaptic measurements by pulse stimulation were performed at room temperature using a semiconductor characterization system (Keithley 4200-SCS). The CrPS_4 thickness was measured using an atomic force microscopy (AFM) topography measurement (Park system XE-100). Transmission electron microscopy (TEM) and energy dispersive spectroscopy (EDS) analyses were performed using a Talos TEM (FEI Talos F200X) equipped with four silicon drift detectors (SDDs) (Bruker). In situ I - V /TEM images were obtained using a 200-kV field emission TEM (Tecnai F20). SEM images were obtained using a field-emission SEM (TESCAN MIRA-II) at an accelerating voltage of 15 kV. Quantitative modeling of the frequency-dependent binary resistive switching was performed using HSPICE simulation based on Verilog-A code.

Results and discussion

As shown in Fig. 1a, the CrPS_4 lattice has puckered hexagonally close-packed sulfur layers, which are stacked in parallel with Cr and P in octahedral and tetrahedral interstices, respectively²³. There is a large vdW gap between the sulfur layers along the c axis in these bulk crystals²⁴. 2D layered CrPS_4 single crystals were synthesized using a chemical vapor transport (CVT) method, as described in the methods section. The crystallinity and chemical composition of the CrPS_4 crystals were confirmed through TEM and EDS analyses, respectively. A single-crystalline CrPS_4 flake with a $15 \mu\text{m}$ diameter and a 300 nm thickness was mechanically exfoliated, as shown in the TEM image in Fig. 1b. The contrast observed in the image implies that the surface of the flake is not sufficiently flat. The selected-area electron diffraction pattern (SADP) provided in the inset of Fig. 1b shows that the CrPS_4 crystal has a monoclinic structure and is highly crystalline. The high-resolution TEM image shown in Fig. 1c also indicates that CrPS_4 is highly crystalline. Figure 1d shows the EDS results obtained at four different points in the CrPS_4 sample. From the EDS results, the average atomic ratio of Cr:P:S was determined to be 1.1:1:4, which is consistent with the stoichiometric ratio within experimental error.

A CBRAM device using the mechanically exfoliated CrPS_4 is schematically illustrated in the inset of Fig. 2a.



The device is positioned at the cross-point between an electrochemically active Ag or Cu top electrode and an inactive Au bottom electrode on a SiO₂/Si substrate, leading to a metal/insulator/metal (MIM) capacitor structure. The single-crystalline 2D layered CrPS₄ acts as an electrolyte with a controlled thickness. This electrolyte

was fabricated using a mechanical exfoliation method and aligned on the patterned Au bottom electrode using a transfer method^{25,26}. Both the top and bottom electrodes were fabricated using electron-beam (e-beam) lithography and e-beam evaporation (see the methods section for detailed information).

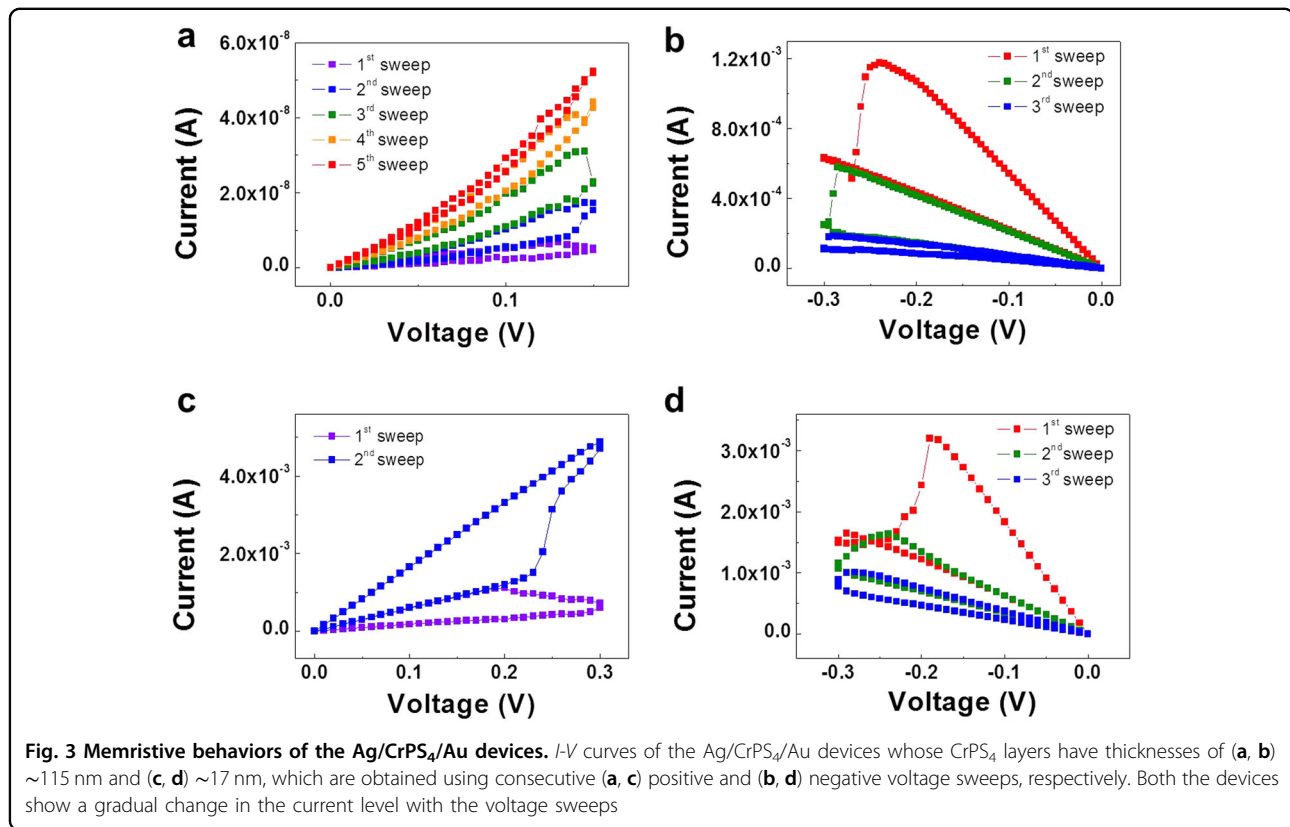
The current-voltage (I - V) curves in Fig. 2a, b show the bias-polarity-dependent bipolar resistive switching (RS) behaviors of the Ag/CrPS₄/Au structures with exfoliated CrPS₄ layers having 115 and 17 nm thicknesses, respectively (Supporting Information, Fig. S1). In Fig. 2a, the initial current is very noisy because it is close to the detection limit of the electrical measurement system used. Above a forming voltage (V_{forming}) of approximately +4 V with a compliance current of 0.1 μ A, the current drastically increases, and the device reaches a low resistance state (LRS). After the forming process, the bipolar RS behavior between this LRS and the high resistance state (HRS) occurs at V_{reset} (LRS \rightarrow HRS) and V_{set} (HRS \rightarrow LRS), which have values of -1.2 V and $+0.8$ V, respectively. As shown in Fig. 2b, the device with the thin CrPS₄ (17 nm) layer displays higher initial and HRS current levels along with lower switching voltages of V_{reset} (-0.27 V) and V_{set} ($+0.27$ V) than the Ag/CrPS₄ (115 nm)/Au device. In addition, the thinner device shows reproducible RS behavior without the forming process, in contrast to the thicker device. These results can be ascribed to the thinner CrPS₄ electrolyte layer. If we consider conducting filament formation and rupture based on metal ion migration as a mechanism for the bipolar-type switching, a higher voltage is required for both the migration of Ag ions in a thicker CrPS₄ layer and the formation of a longer conducting filament^{27,28}. In a thinner device, a low voltage is sufficient to form a short conducting filament connecting the top and bottom electrodes, leading to forming-free resistive switching. It can be argued that our thicker device shows more abrupt resistive switching because of its larger on/off resistance ratio and lower HRS current compared to the thinner device²⁹.

The log-log scale I - V curves for the LRSs of both devices clearly exhibited linear Ohmic behavior with gradients close to 1, indicating the formation of conductive bridges in the CrPS₄ layer (Supporting Information, Figs. S2a and S2b). Furthermore, the temperature dependences of the resistances were investigated to identify the conduction mechanism of each resistance state. The LRS resistance increased with increasing temperature, corresponding to metallic behavior, while the HRS resistance decreased as the temperature increased, which is a characteristic feature of insulators (Supporting Information, Fig. S3a)³⁰. In addition, the temperature dependence of the HRS resistance was effectively fitted by an Arrhenius plot, suggesting the occurrence of thermally activated conduction behavior in the HRS with an activation energy of 0.24 eV (Supporting Information, Fig. S3a). The amplitudes of the set and reset voltages decreased as the temperature increased from 200 K to 400 K due to the easy migration of the thermally activated Ag ions, leading to the formation and rupture of the Ag conductive bridges, even under a low electric field^{3,6} (Supporting Information, Fig. S3b).

Given the above experimental observations, the bipolar RS behavior observed in our Ag/CrPS₄/Au devices can be explained as follows. When a positive voltage is applied to the Ag top electrode, the electrochemically active Ag ions can migrate towards the Au bottom electrode, leading to the growth of an Ag conductive bridge from the Au cathode that reaches the Ag top electrode at V_{forming} . Bipolar RS behaviors are caused by the formation and rupture of this conductive bridge at switching voltages with opposite polarities. In most CBRAM devices, the formation/rupture of the conductive bridge inside the solid electrolyte layer is attributed to the diffusion of metal (Ag or Cu) ions and their oxidation/reduction reactions³¹.

To confirm the above RS mechanism based on the electrochemically induced formation/rupture of a cation conductive bridge, the top electrode materials were replaced with electrochemically active Cu and electrochemically inactive Au or Pt. The Cu/CrPS₄/Au device showed RS behavior similar to that displayed by the Ag/CrPS₄/Au devices (Supporting Information, Fig. S4a). However, the Au/CrPS₄/Au and Pt/CrPS₄/Au devices exhibited typical I - V curves of MIM structures without either a forming process or RS behavior (Supporting Information, Figs. S4b and S4c). Moreover, a change in the surface between the pristine state, LRS, and HRS of the planar Ag/CrPS₄/Au configuration induced by Ag ion migration was directly observed using scanning electron microscopy (SEM) (Supporting Information, Fig. S5). In the LRS, which was obtained after the application of a positive forming voltage to the Ag electrode, a conducting path grew from the edge region of the Ag electrode and reached the Au electrode. In the HRS, it was found that the conducting filament was disconnected from the Au electrode. From the in situ I - V /TEM images of the vertical Ag/CrPS₄/Au device (Supporting Information, Fig. S6), it seemed that the number of conducting filaments formed at the Au electrode increased with increasing applied voltage. A further comprehensive TEM study is needed to provide more analytical details and to confirm this hypothesis.

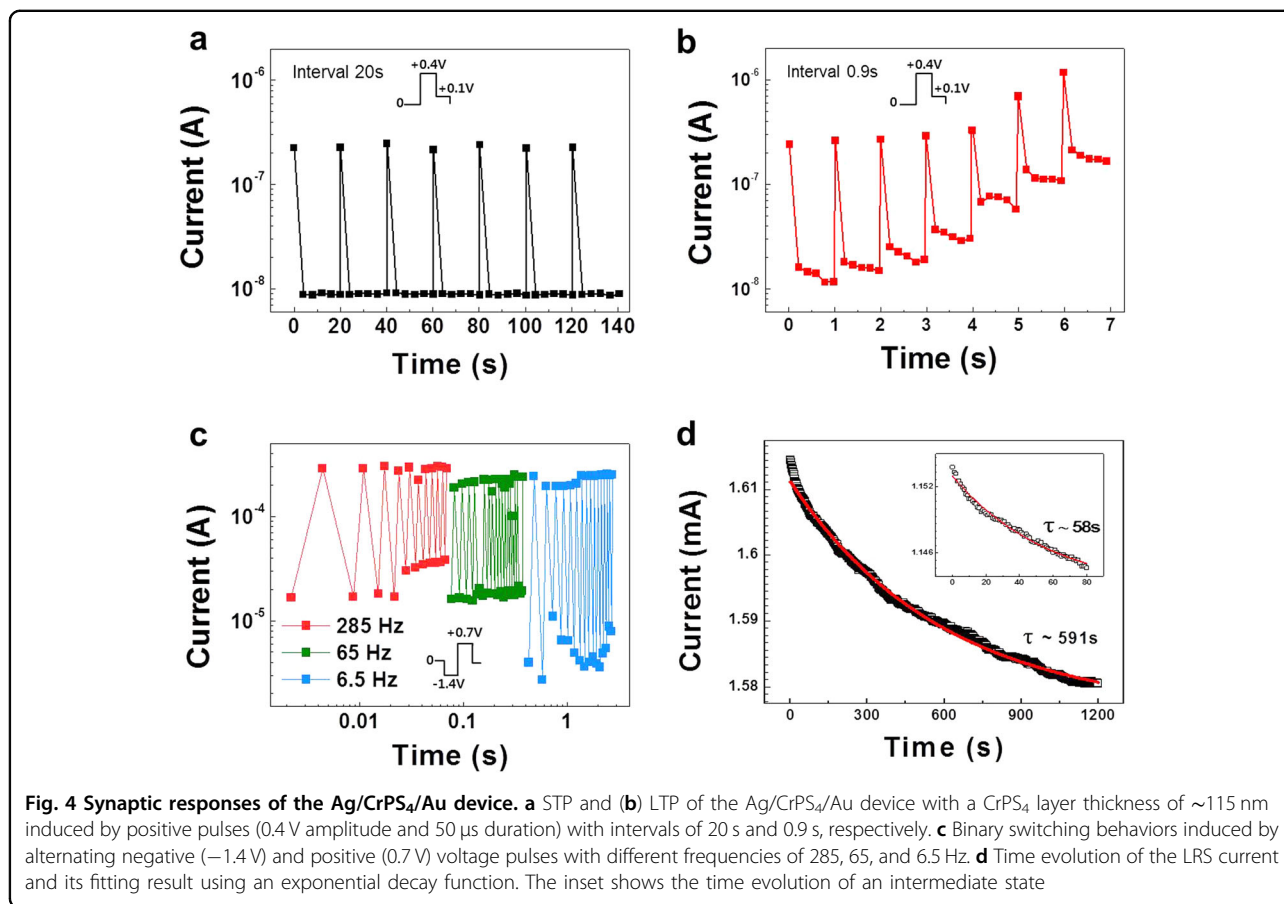
Memristive behavior was also obtained by controlling Ag ion movement through consecutive voltage sweeps in the Ag/CrPS₄/Au devices. Figure 3a, b show the potentiation and depression, respectively, of the Ag/CrPS₄ (115 nm)/Au device. When consecutive positive (0 to 0.15 V) and negative (0 to -0.3 V) voltage sweeps are applied to the device in the HRS and the LRS, its current level gradually increases and decreases, respectively. Figure 3c, d show similar memristive behaviors for the Ag/CrPS₄ (17 nm)/Au device. It is noteworthy that such memristive behavior is induced by voltages lower than 0.3 V in both the thin (17 nm) and thick (115 nm) Ag/CrPS₄/Au devices. In previous reports, the memristive operating voltages



of an Ag₂S-based atomic switch and an AgInSbTe-based CBRAM were -0.27 V/ 0.23 V and -0.45 V/ 0.4 V, respectively^{12,32}. These results imply that our vertical Ag/CrPS₄/Au device has multiple resistance states that can be achieved through consecutive voltage sweeps, which are usually observed in memristor devices^{12–15}. The length and width of the conducting filament formed between the top and bottom electrodes are state variables in a memristor device, which depend on the applied voltage profile^{33–35}. Therefore, the multiple resistance states of our devices may be caused by the gradual migration of Ag ions and the resultant changes in the length and width of the conducting filament. Such multiple resistance states can be reproducibly observed by performing repetitive measurements under the same conditions. In order to stabilize the multiple resistance states, the corresponding conducting filaments should be complete and connect the top and bottom electrodes.

Typically, the cation movement causing multiple resistance states in a CBRAM-based memristor device can also be controlled through the variation of an electrical input pulse, leading to synaptic plasticity^{12,13}. The plasticity mechanisms are commonly categorized as short- and long-term plasticity (STP and LTP, respectively). Synaptic plasticity is useful for implementing a model of human memory in adaptive and neuromorphic systems through synaptic weight modification^{12–16}. Figure 4 shows the

synaptic plasticity of the Ag/CrPS₄ (115 nm)/Au memristor device, which includes both STP and LTP behaviors. To observe the synaptic plasticity, electrical input pulses with different intervals were applied. STP, which corresponds to volatile memorization, was induced by electrical pulses, each with an amplitude of 0.4 V, a duration of 50 μ s, and a repetition interval of 20 s (Fig. 4a). The current change after the application of each input pulse was monitored using six reading pulses, each with an amplitude of 0.1 V and a duration of 50 μ s. The interval between the input pulse and the first reading pulse was 0 s, as shown in the inset of Fig. 4a. The current rapidly returns to its initial value, indicating that a long repetition interval time brings about the facile decay of the conductive bridge resulting from spontaneous Ag ion diffusion. During the LTP programming, the input pulse repetition interval was decreased to 0.9 s, while the pulse amplitude and duration were fixed at 0.4 V and 50 μ s, respectively. As shown in Fig. 4b, a transition to a gradually higher current level is obtained with frequently repeated stimulation of input pulses. The current does not decay back to its original state, which means that the short repetition interval time is insufficient for the Ag ions to diffuse to their initial state^{12,13,16,19}. As a result, the current is increased by the frequent application of input pulses to the Ag/CrPS₄ (115 nm)/Au memristor device. The memristive behaviors and synaptic responses shown



in Figs. 3 and 4 are representative ones among the data observed for ~30 devices, which showed reproducible resistive switching. This behavior is similar to that of a biological synapse, the synaptic weight of which is increased by repeated stimulation^{10,12–16}.

Figure 4c shows the frequency-dependent binary switching of the Ag/CrPS₄ (115 nm)/Au device. The amplitudes of the negative and positive input pulses were fixed at −1.4 and 0.7 V, respectively. These alternating input pulses cause binary resistive switching of the Ag/CrPS₄ (115 nm)/Au device, which depends on the frequency of the input pulses with a modulated duration time. The resistance on/off ratio increases as the frequency decreases, and the pulse duration time increases when input pulses with 285, 65, and 6.5 Hz are applied. The observed frequency-dependent binary resistive switching shown in Fig. 4c can be quantitatively modeled using HSPICE simulation based on Verilog-A code (Supporting Information, Fig. S7 and Table S1). It was found that the frequency-dependent binary resistive switching was induced by frequency-dependent changes in the length and width of the conducting filament during resistive switching: the conducting filament increasingly ruptured due to the decreasing frequency of the input

pulses. Therefore, this frequency-dependent binary switching can be ascribed to the rate-limiting Ag ion migration and has applications in advanced computer logic and non-volatile memory¹⁷.

Figure 4d shows the time evolution of the current in the LRS of the Ag/CrPS₄ (115 nm)/Au device, which was obtained at a reading voltage of 0.1 V just after the positive voltage sweep (0 to 0.9 V) at room temperature under ambient conditions, along with its fitting result using the exponential decay function¹⁷:

$$I = I_0 + A \exp(-t/\tau) \quad (1)$$

where I and I_0 represent the current values at time t and in the stable state, respectively; A is a prefactor; and τ is the decay time constant. From the fitting parameters, we can estimate the τ value of the current in the LRS to be 591 s. As shown in the inset, the current decay curve of an intermediate state with a current level lower than that of the LRS, obtained after applying a positive voltage sweep (0 to 0.5 V), can also be fitted with the same exponential function, and its τ value is estimated to be 58 s. The shorter decay time obtained for the intermediate state can be attributed to the Ag conducting path being thinner

than that in the LRS^{19,36}. The high applied voltage required to achieve the LRS state induces the formation of a stable and complete conducting filament, thus leading to a decrease in the resistance level of the device. The small applied voltage required to achieve the intermediate state induces the formation of an unstable and incomplete conducting filament, which decays faster than that of the LRS state³⁷. According to a previous report, voltage pulses with a higher repetition rate induced rehearsal before the complete decay of the memorization level, leading to long-term memorization^{16,38}. Therefore, it is expected that long-term memorization can be achieved by applying voltage pulses with a higher repetition rate.

Conclusion

In summary, an Ag/CrPS₄/Au synaptic device based on a single-crystalline 2D layered CrPS₄ electrolyte has been reported. Several essential synaptic functions were demonstrated in this device, including synaptic plasticity and STP to LTP transition. These synaptic functions were dependent on the intervals and durations of the stimulating electrical pulses. Moreover, synaptic plasticity was also observed in the Ag/CrPS₄/Au device with a 17-nm-thick CrPS₄ layer, indicating that high-density neuromorphic devices could be implemented using a very thin CrPS₄ layer. The unprecedented synaptic functions observed in the thickness direction of the single-crystalline 2D layered CrPS₄ offer potential for application in low-dimensional neuromorphic devices with a low density of structural defects.

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Conflict of interest

The authors declare that they have no conflict of interest.

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