Empirical Model of Relationship between the Operation Frequency and the Size of Crossbar Array in the IGZO ReRAM-based Reconfigurable Logic

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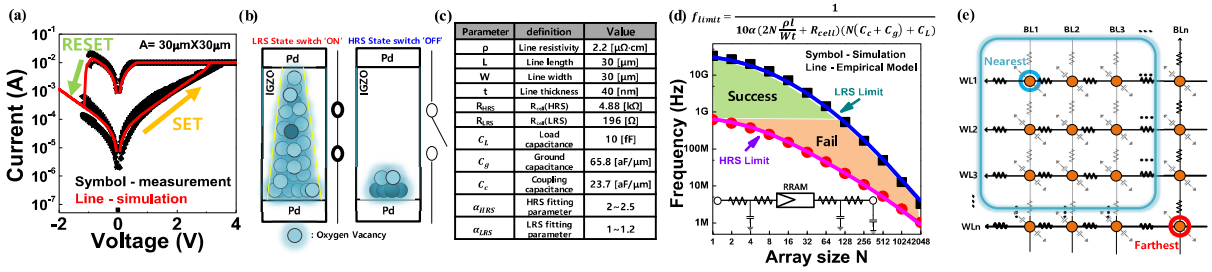
To overcome the von Neumann bottleneck which is caused by a single data path between the CPU and main memory and to maximize the energy-efficiency, the reconfigurable logic (RL) architecture implemented by the memory crossbar array which can acts as the routing switch matrix has recently attracted much attention [1]. Undoubtedly, the performance and advantage of RL over the von Neumann architecture should be quantitatively assessed for more fair comparison and systematic RL design. However, the real characteristic of memory device has not been fully considered in the system-level evaluation of RL architecture. Indeed, the behavioral model for device characteristic has been often used in the system-level evaluation rather than the SPICE model. Motivated by this background, in this paper, the measured characteristic of the fabricated InGaZnO (IGZO) Resistive Random Access Memory (ReRAM) device is incorporated into SPICE simulation via Verilog-A compact model. Furthermore, as an example of the system-level performance metrics, the relationship between the RL operation frequency and the size of crossbar array based on IGZO ReRAM is empirically modeled.

The Pd/IGZO/Pd ReRAM device exhibits abrupt switching behavior after the forming process (symbol in Fig. 1(a)), the conducting filament (CF) of which is modulated by the oxygen ion/vacancy-based redox reaction as illustrated in Fig. 1(b). The I-V characteristic of IGZO ReRAM device is modeled like [2] and incorporated into SPICE simulation via Verilog-A, the simulated result of which agrees very well with the measured one (line in Fig. 1(a)). Then, the crossbar array is implemented with parameters (Fig. 1(c)) as shown in Fig. 1(e). The SPICE simulation result for the relationship between the RL operation frequency (f_{op}) and the size of crossbar array (N) is shown as denoted by symbols in Fig. 1(d). Consistently, to estimate the f_{op}-N relationship, we calculate an Elmore delay considering interconnect resistance and capacitance of the crossbar array and establish an empirical model as shown in the equation in Fig. 1(d). Proposed empirical model also shows good agreement with the SPICE simulation (lines in Fig. 1(d)), where the pass/fail of RL operation is evaluated in the cell farthest from the input driver. Proposed model is potentially useful for the real device characteristic-aware design and the system-level evaluation of RL architecture.



Parameter	definition	Value
ρ	Line resistivity	2.2 [μΩ·cm]
L	Line length	30 [μm]
W	Line width	30 [μm]
t	Line thickness	40 [nm]
R_{HRS}	R_{cell}(HRS)	4.88 [kΩ]
R_{LRS}	R_{cell}(LRS)	196 [Ω]
C_L	Load capacitance	10 [fF]
C_g	Ground capacitance	65.8 [aF/μm]
C_c	Coupling capacitance	23.7 [aF/μm]
α_{HRS}	HRS fitting parameter	2~2.5
α_{LRS}	LRS fitting parameter	1~1.2

Fig 1. (a) Measured I-V characteristic of IGZO ReRAM. (b) Illustrations of LRS and HRS. (c) Table summarizing the model parameters. (d) SPICE simulation and empirical model of the operation frequency versus the size of crossbar array. (e) Circuit schematic of the IGZO ReRAM-based crossbar array.

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