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Fabrication and characterization of Pt/Al_2O_3/Y_2O_3/$In_{0.53}Ga_{0.47}As$ MOSFETs with low interface trap density

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In this work, we fabricated the $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors (MOSFETs) with a MOS interface of $Y_2O_3/In_{0.53}Ga_{0.47}As$ and recessed gate structure. We investigated the interfacial properties of the gate stack and the junction characteristics of the fabricated MOSFETs. Low subthreshold slope ($SS = 110$ mV/dec), high on/off current ratio ($I_{on}/I_{off} = 10^6$), and high effective mobility of 1600 cm^2/V·s were achieved in the MOSFETs at a sheet charge density $(N_s) = 1.2 \times 10^{12}$ cm^{-2}. From the temperature dependence of *I–V* characteristics, the interface trap density was extracted to be $D_{it} = 2.2 \times 10^{11}$ $cm^{-2}\cdot eV^{-1}$ with a negligible trap-assisted leakage current. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4974893]

InGaAs is the most prospective channel alternative for n-channel field effect transistors in future logic devices due to its high electron mobility and injection velocity.[1,2] Recent advance in metal-oxide-semiconductor (MOS) interface control in high-*k*/InGaAs systems allows a low *SS* and high effective mobility, which are important to reduce V_{DD} in VLSI circuits.[3–5] In particular, the trivalent oxide has a better interfacial quality than the HfO_2/InGaAs interface.[6,7] Finally, we chose the Y_2O_3 gate dielectric because the *k*-value of Y_2O_3 (14–17.8) is higher than that of Al_2O_3 (9–10), which is typically used as an interfacial layer. Suzuki *et al.*[8] reported a low equivalent oxide thickness (EOT) gate stack using the Al_2O_3 layer as an interfacial layer between InGaAs and HfO_2 (higher-*k* material than Al_2O_3). Recent studies on InGaAs MOSFETs have used Al_2O_3/ a higher-*k* gate dielectric for the gate stack with a thin EOT.[9–11] For an ultimate EOT scaling, on the other hand, the *k*-value of the interfacial layer should also be scaled. Therefore, developing a higher-*k* interfacial layer than the dielectric constant of Al_2O_3 is quite important. However, the gate stack of Al_2O_3 has been studied widely than other high-*k* dielectrics. Although Chang *et al.*[12] reported InGaAs MOSFETs with Y_2O_3, the extracted interface trap density (D_{it}) in InGaAs MOSFETs was quite high, resulting in high *SS* at a given EOT. We also reported InGaAs MOSFETs with low *SS* utilizing Y_2O_3 as a gate dielectric.[13] However, the device structure was a bottom gate InGaAs-on-insulator, which remained for a feasibility study.

In this work, therefore, we investigated the interfacial properties of $Y_2O_3/In_{0.53}Ga_{0.47}As$ by using $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) capacitors. We also investigated the electrical performance and junction characteristics of top-gate $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors (MOSFETs) with Y_2O_3 as a gate dielectric and recessed gate structure.

To investigate the MOS interface between the gate insulator (Y_2O_3) and $In_{0.53}Ga_{0.47}As$ channel, we fabricated the MOS capacitors. The channel layers are 500-nm-thick n-$In_{0.53}Ga_{0.47}As$ (doping concentration, N_D of approximately 1×10^{16} cm^{-3}), which was grown on a highly doped n-InP (001) wafer with $N_D \sim 10^{18}$ cm^{-3} by the metal organic chemical vapor deposition (MOCVD). After at *ex-situ* surface treatment of the III–V wafers with NH_4OH and $(NH_4)_xS$ solutions, a 10-nm-thick-Y_2O_3 layers were deposited on III–V layers by the electron beam (EB) evaporator.

Then, 5-nm-thick- Al_2O_3 layers were deposited on Y_2O_3 layers by the atomic layer deposition (ALD). Finally, the gate was formed by the Pt (30 nm)/Au (70 nm) deposition.

To verify the effect of the post metallization annealing (PMA), MOS capacitors were annealed at several temperatures by the annealing chamber. Figure 1 shows a schematic image of the MOS capacitor and the multi-frequency *C-V* characteristics of the MOS capacitors annealed in N_2 ambient at an annealing temperature of 250, 300, 350, and 400 °C. As-deposited device showed poor *C-V* characteristics with a severe frequency dispersion. Annealed devices at 250 and 300 °C showed a significant improvement of *C-V* characteristics compared with the as-deposited device in the frequency dispersion and steep capacitance change by gate voltage sweeping from the accumulation to the depletion states. The MOS capacitor annealed at 350 °C showed the steepest capacitance change and the smallest frequency dispersion. However, with annealed device at 400 °C, *C-V* characteristics were slightly degraded at the bias range from the depletion to the inversion states.

To quantitatively evaluate the *C-V* characteristics and interfacial quality, we extracted D_{it}(E) by the conductance

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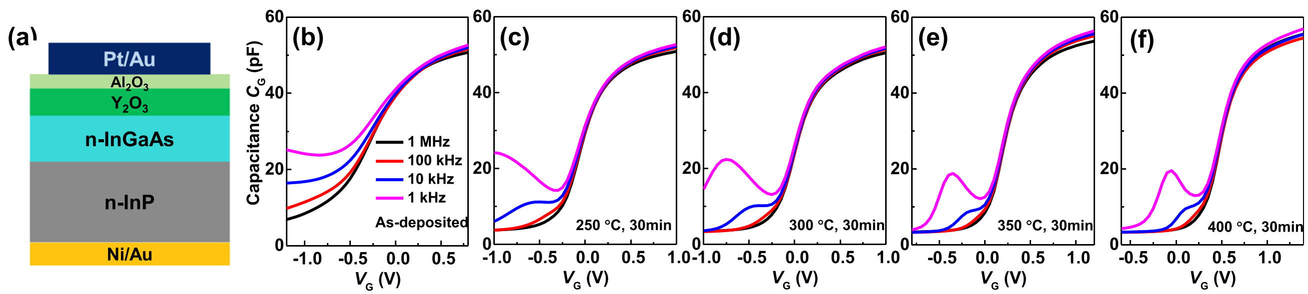

FIG. 1. *C-V* characteristics of Pt/Al_2O_3/Y_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors at several frequencies (a) schematic image of MOS capacitors (b) as-deposited (c) after RTA at 250 °C (d) 300 °C (e) 350 °C (f) 400 °C for 30 min at N_2 ambient.

method. We obtained the parallel conductance per unit area (G_p) from the measured equivalent circuit. We note that G_p/ω value is modeled as

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (1)$$

with G_m as the measured conductance per unit area, C_{ox} as the oxide capacitance per unit area, $\omega = 2\pi f$ as the angular frequency, and C_m as the measured capacitance per unit area. Fig. 2(a) shows the fitted G_p/ω versus the frequency curve extracted by Eq. (1). We also considered the surface potential fluctuation (SPF) due to the non-uniformity of the oxide charge and the interface traps.[14] Finally, we obtained the experimental D_{it}(E) ranging from 10^{11} to $10^{12}\,cm^{-2}\cdot eV^{-1}$ considering the SPF. Annealed sample at 400 °C has generally a higher D_{it}(E) than that at 350 °C. Possible origin of this degradation is the Ga up-diffusion, which occurred with annealing at a high temperature of 400 °C.[15] The MOS capacitor annealed at 350 °C had the lowest D_{it}(E) among devices shown in Fig. 2(b). We found that the best annealing temperature to achieve a low D_{it} is observed to be $T = 350\,°C$ and $D_{it} \sim 2.2 \times 10^{11}\,cm^{-2}\cdot eV^{-1}$. This is quite low among any high-*k*/$In_{0.53}Ga_{0.47}As$ interface and is comparable with that of reported high-*k*/$In_{0.53}Ga_{0.47}As$ interface such as Y_2O_3/$In_{0.53}Ga_{0.47}As \sim 8 \times 10^{11}\,cm^{-2}\cdot eV^{-1}$ and Al_2O_3/$In_{0.53}Ga_{0.47}As \sim 1 \times 10^{12}\,cm^{-2}\cdot eV^{-1}$.[12,16–18] Also, the interfacial quality of Y_2O_3/$In_{0.53}Ga_{0.47}As$ showed lower D_{it} values than that of Al_2O_3/$In_{0.53}Ga_{0.47}As$ as shown in Fig. 2(b).

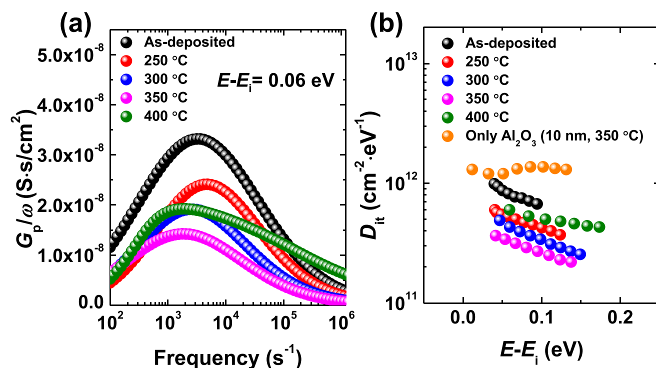

FIG. 2. (a) The comparison of parallel conductance (G_p/ω) versus frequency between as-deposited, RTA at 250, 300, 350, and 400 °C at E-E_i = 0.06 eV (b) Energy distribution of D_{it}(E), evaluated by the conductance method for Pt/Al_2O_3/Y_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with an annealing temperature.

Fig. 3(a) shows a schematic image of the device structure and fabrication process. To fabricate the recessed gate $In_{0.53}Ga_{0.47}As$ MOSFETs, epitaxial layers were grown on semi-insulating (S. I) InP (001) wafer by the MOCVD process. The 50-nm-thick InP buffer layer ($N_A \sim 1 \times 10^{17}\,cm^{-3}$) was grown on S. I. InP (001) wafer. The device layers were composed of 20-nm-thick $In_{0.53}Ga_{0.47}As$ channel (unintentionally doped), 5-nm-thick InP etch stop (unintentionally doped), 50-nm-thick n^+ $In_{0.53}Ga_{0.47}As$ contact layer ($N_D \sim 1 \times 10^{19}\,cm^{-3}$) from the bottom side. In the first, device isolation was carried out by the mesa etching process. Then, n^+ $In_{0.53}Ga_{0.47}As$ and InP were recessed in gate regions by citric acid and HCl solutions, respectively. Subsequently, it was cleaned by acetone, NH_4OH, and $(NH_4)_xS$ solutions to remove the native oxide and to passivate the surface by sulfur(S) atoms. As a gate dielectric, 10-nm-thick Y_2O_3 and 5-nm-thick Al_2O_3 was deposited by EB evaporator and ALD, respectively. Here, Al_2O_3 was deposited for the step-coverage around the mesa to prevent the leakage current over the edge. The gate metal (Pt/Au) was formed by the EB evaporation, followed by the rapid thermal annealing (RTA) at 350 °C for 1 min. in N_2 ambient. Finally, Ni was deposited for the S/D contacts. Cross-sectional

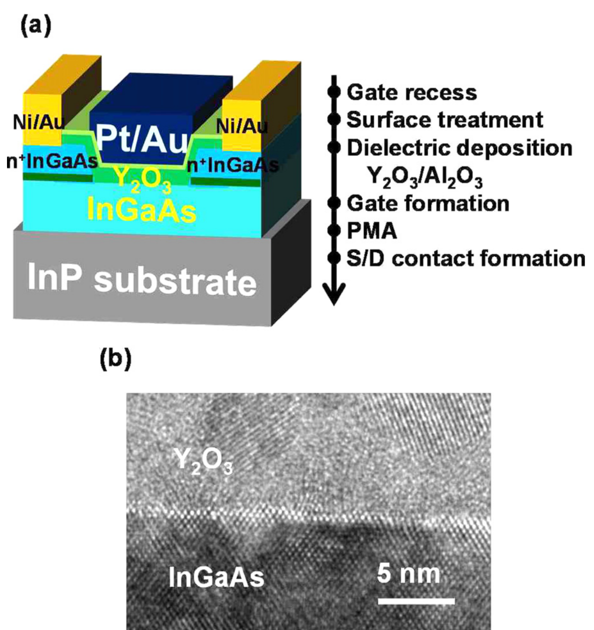

FIG. 3. (a) Schematic image of the final device structure and fabrication process of InGaAs MOSFETs (b) Cross-sectional TEM image of Y_2O_3/InGaAs interface.

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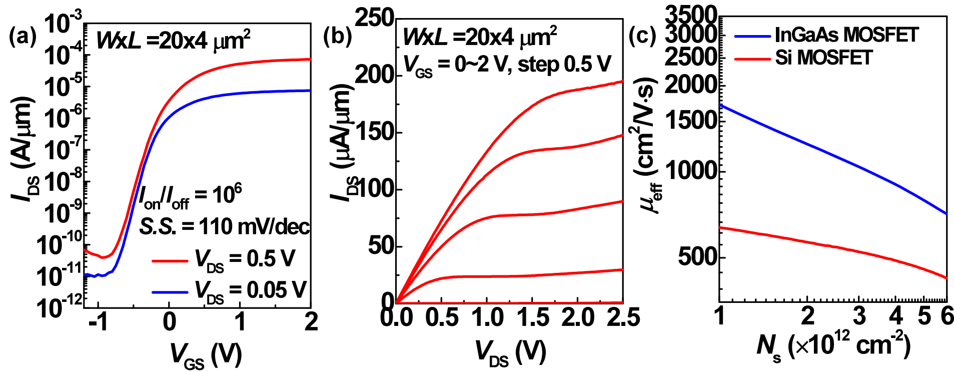

FIG. 4. (a) Transfer and (b) output characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs with L_G of 4 μm. Good transfer and output characteristics were observed with $SS = 110$ mV/dec and on/off ratio of 10^6. (c) Effective mobility (μ_{eff}) characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs. μ_{eff} is about two times higher than that of Si MOSFETs.

transmission electron microscope (TEM) image of the fabricated $Y_2O_3/In_{0.53}Ga_{0.47}As$ stack in Fig. 3(b) shows an abrupt interface between Y_2O_3 and $In_{0.53}Ga_{0.47}As$.

Electrical characterization was carried out for the fabricated $In_{0.53}Ga_{0.47}As$ MOSFETs. Figs. 4(a) and 4(b) show the typical drain current (I_{DS})–V_{GS} (gate voltage) and I_{DS}–V_{DS} (drain voltage) characteristics of the $In_{0.53}Ga_{0.47}As$ MOSFETs with a gate length (L_G) of 4 μm. Good I_{DS}–V_{GS} curves were obtained with steep subthreshold slope ($SS = 110$ mV/dec) considering a thick equivalent oxide thickness (EOT) ($\sim$4.6 nm) of the device and a high on/off ratio (10^6). We obtained the gate current at least 4-orders lower than the drain current. Also, a clear current saturation was observed in the output characteristics.

To further characterize the electrical properties of the gate stack and the junction formation in the fabricated MOSFETs, we evaluated the effective mobility (μ_{eff}) and temperature dependence of *I-V* characteristics. We obtained $\mu_{eff} \sim 1600$ cm^2/V·s at the sheet charge density $(N_s) = 1.2 \times 10^{12}$ cm^{-2} due to the good interfacial quality between Y_2O_3 and $In_{0.53}Ga_{0.47}As$. μ_{eff} values were obtained to be roughly two times higher than that of Si MOSFET all over the range of N_s as shown in Fig. 4(c). Our μ_{eff} value is comparable to that reported of the other group.[19] Fig. 5(a) shows the temperature dependence of transfer curves of the $In_{0.53}Ga_{0.47}As$ MOSFET with $L_G = 4$ μm at $V_{DS} = 0.05$ V. To investigate the leakage current mechanism at the off-state, we evaluated the temperature-dependence of the off-state current (I_{off}). Inset of Fig. 5(a) shows I_{off} at several bias points as a function of $1/kT$

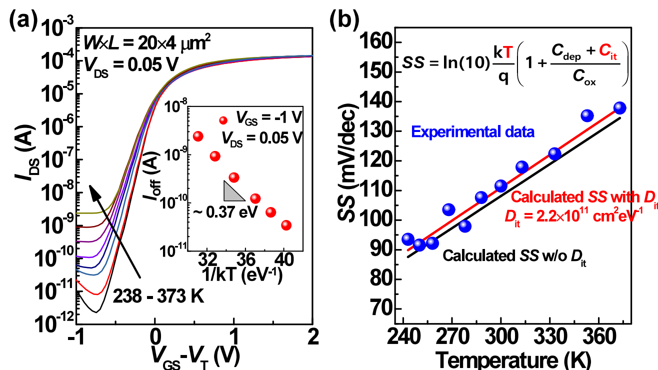

FIG. 5. (a) Temperature dependence of the transfer characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs. Inset shows I_{off} at gate bias $= -1$ V as a function of temperature for fabricated devices. (b) temperature-dependence of *SS*. Calculated *SS* lines with and without D_{it}.

with *k*T as the average thermal energy. It was found that $\ln(I_{off})$ and $1/kT$ shows a linear relationship. From the slope of the plot in inset of Fig. 5(a), the activation energy (E_a) was extracted to be $E_a \sim 0.37$ eV which is close to a half of bandgap of $In_{0.53}Ga_{0.47}As$. I_{off} behaviors in our device that can be explained by the generation current (I_{gen}) in PN junction, which can be expressed by

$$I_{gen} = A_j \int_0^{W_d} q g_{th} dx \cong A_j \frac{q n_i}{2\tau_o} W_d \quad \text{with } g_{th} = \frac{n_i}{2\tau_o}, \tag{2}$$

where A_j, n_i, τ_o, and W_d as the effective junction area, the intrinsic carrier concentration, the excess carrier lifetime in the depletion region, and the depletion width, respectively. Since I_{gen} is proportional to n_i, an activation energy (E_a) of I_{off} in PN junction dominated by I_{gen} is extracted to be $E_g/2$. This result indicates that the generation current is dominant in the S/D junction in the device at the off-state and the trap-assisted tunneling current is quite minor in the S/D junction. *SS* was monotonically decreased with decreasing the temperature as shown in Fig. 5(b). From the relationship between *SS* and temperature, D_{it} was extracted to be 2.2×10^{11} cm^{-2}·eV^{-1}, which is quite low among the reported D_{it} values of high-*k*/InGaAs interfaces. *SS* is expected to be further improved by scaling the EOT and reducing D_{it}. Here, we assumed that the channel layer is fully depleted. (C_{dep} is 6.11×10^{-7} F/cm^2, $\varepsilon_{InGaAs} = 13.8\varepsilon_o$)

Finally, in this work, we obtained $SS = 110$ mV/dec and D_{it} of approximately 2.2×10^{11} cm^{-2}·eV^{-1}. We found that D_{it} in the MOSFETs with the MOS interface of $Y_2O_3/In_{0.53}Ga_{0.47}As$. By scaling down of the EOT and channel thickness, it is expected to achieve $SS \sim 60$ mV/dec with the $Al_2O_3/Y_2O_3/In_{0.53}Ga_{0.47}As$ gate stack.[19] We believe that our work with thick EOT is also quite meaningful as a feasibility study. Also, further improvements of the electrical properties in $In_{0.53}Ga_{0.47}As$ MOSFETs are expected through further process optimization such as EOT and gate length scaling as well as a thin body structure as a future work.

In this study, we fabricated $In_{0.53}Ga_{0.47}As$ MOSFETs with a MOS interface of $Y_2O_3/In_{0.53}Ga_{0.47}As$ and a recessed gate structure. We investigated the electrical properties of fabricated $In_{0.53}Ga_{0.47}As$ MOSFETs and achieved low *SS* (=110 mV/dec) and high on/off ratio (=10^6). The effective channel carrier mobility μ_{eff} was also as high as 1600 cm^2/V·s at $N_s = 1.2 \times 10^{12}$ cm^{-2}, which is much higher than the conventional Si MOSFETs. From the temperature dependence of

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I–V characteristics, we obtained $D_{it} = 2.2 \times 10^{11}\,cm^{-2} \cdot eV^{-1}$ and a negligible trap-assisted leakage current in the S/D junction. These results strongly suggest that Y_2O_3 is a promising dielectric interlayer for extremely low EOT gate stack in $In_{0.53}Ga_{0.47}As$ MOSFETs.

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