Fully subthreshold current-based characterization of interface traps and surface potential in III–V-on-insulator MOSFETs

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\textbf{Abstract}

We report characterization of the interface trap distribution \(D_i(E)\) over the bandgap in III–V metal-oxide–semiconductor field-effect transistors (MOSFETs) on insulator. Based only on the experimental subthreshold current data and differential coupling factor, we simultaneously obtained \(D_i(E)\) and a nonlinear mapping of the gate bias \(V_{GS}\) to the trap level \(E_t\) via the effective surface potential \(\psi_{surf}\). The proposed technique allows direct extraction of the interface traps at the In\textsubscript{0.53}Ga\textsubscript{0.47}As-on insulator (−OI) MOSFETs only from the experimental subthreshold current data. Applying the technique to the In\textsubscript{0.53}Ga\textsubscript{0.47}As channel III–V−OI MOSFETs with the gate width/length \(W/L = 100/50, 100/25, \) and 100/10 \(\mu\text{m}/\mu\text{m}\), we obtained \(D_i(E) \approx 10^{11}−10^{12} \text{eV}^{-1} \text{cm}^{-2}\) over the bandgap without the dimension dependence.

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1. Introduction

III–V compound semiconductors are one of the most preferred candidates for replacing silicon-based electronics because of their high electron mobility [1]. To apply these materials to extremely scaled technology node in complementary metal oxide semiconductor (CMOS) circuits, it is necessary to suppress the short channel effects (SCEs) [2]. These motivated many studies on III–V FETs with a thin body structure, such as Fin and Gate-all-around [3,4]. III–V–on insulator (III–V−OI) structure with an ultra-thin body (UTB) has also been studied by many groups [5,6], and scaled devices with gate length \(L < 20\) nm were recently reported [7]. On the other hand, one of the key parameters to determine the device performance is the interface traps between the insulator and the UTB in SOI devices [8,9]. These affect electrical characteristics as well as device reliability. Therefore, accurate characterization of the interface trap distribution \(D_i(E)\) over the bandgap \((E_V < E_t < E_C)\) is crucial in the device characteristics, which is detrimental in the device performance including the leakage current and long term reliability. There are useful techniques such as the Terman method [9] and the high-low frequency technique [10–12]. However, there are limits in conventional techniques to extract the energy distribution of interface states over the bandgap. In the case of scaled devices, the capacitance–voltage based measurement is influenced by increased portion of parasitic resistances and capacitances [13,14]. Such characteristics cause inaccurate data extraction and geometrical dependence on the extracted data. Therefore, it is important to investigate and develop an analytical method, which is based upon the \(I−V\) characteristics of devices with small feature size.

In this study, we propose a fully subthreshold current-based technique for the extraction of both \(D_i(E)\) and the effective surface potential \(\psi_{surf}\) in the nonlinear mapping of the gate bias \(V_{GS}\) to the trap energy level \(E_t\) in InGaAs-OI MOSFETs. Both the energy state mapping and interface state distribution \(D_i(E)\) were achieved from the differential body coupling factor [15] and simultaneous nonlinear mapping of the gate bias to the trap level through the effective surface potential [16] though the subthreshold current model [17], respectively.

2. Device structure and electrical properties

A cross-sectional view of the In\textsubscript{0.53}Ga\textsubscript{0.47}As channel III–V−OI MOSFET is shown in Fig. 1(a). The In\textsubscript{0.53}Ga\textsubscript{0.47}As/InP(sacrificial
layer)/In0.53Ga0.47As was epitaxially grown on InP substrate. After cleaning the III–V wafers with NH4OH and (NH4)2S solutions at ex-situ, a 20-nm-thick-Al2O3 layer was deposited on III–V and Si wafers at 200 °C by the ALD. The Al2O3/In0.53Ga0.47As (10 nm, \( N_A = 1 \times 10^{16} \) cm\(^{-3} \))/InP(50 nm, undoped)/In0.53Ga0.47As (100 nm, undoped)/InP substrate and Al2O3/Si substrate were directly bonded to each other. Finally, In0.53Ga0.47As-OI substrate was formed by the selective etching of the In0.53Ga0.47As and InP wafer.

Next, bottom-gate MOSFETs were fabricated on In0.53Ga0.47As-OI wafer using Si substrate (\( N_D = 6 \times 10^{16} \) cm\(^{-3} \)) as a gate electrode. Mesa was defined by wet etching, followed by SiO2 (30 nm) deposition as a field-oxide. Then, source/drain was formed by Ni (30 nm)/Au(70 nm) deposition and a subsequent rapid thermal annealing process at 250 °C for 40 s.

The experimental transfer characteristics with the on/off ratio of 10\(^8\) and the subthreshold swing \( = 300 \) mV/dec with a weak hysteresis of 90 mV and similar subthreshold swing are shown in Fig. 1(b) with the gate width/length \( W/L = 100 \mu m/50 \mu m \). Also, the extracted threshold voltage \( V_T \) turned out to be -0.8 V by the transconductance extrapolation method [18].

3. Extraction of the effective surface potential from the subthreshold current

The subthreshold current model is employed for the non-linear mapping of the gate voltage to the effective surface potential \( \psi_{S,eff} \) [16], as the potential drop across the active channel region, and finally map to the trap energy level \( E_T \). The subthreshold current \( I_{D,sub}(V_{GS}) \) in MOSFETs is modeled to be

\[
I_{D,sub}(V_{GS}) = I_{Do} \exp \left( \frac{V_{GS} - V_T}{m(V_{GS})V_{TH}} \right)
\] (1)

\[
I_{Do} = \mu_C \left( \frac{W}{L} \right) V_{GS} \left( m(V_{GS}) - 1 \right)
\] (2)

\[
m(V_{GS}) = 1 + \frac{C_s(V_{GS})}{C_{ox}} = 1 + \frac{|Q_s(V_{GS})|}{\psi_{S,eff}(V_{GS})C_{ox}}
\] (3)

\[
C_s(V_{GS}) = C_{S,dep} + C_{S,inv} + C_{S,eff}(V_{GS}) + C_{S,dox}(V_{GS})
\] (4)

\[
C_{S,dep}(V_{GS}) = \frac{dQ_{dep}(V_{GS})}{dV_{GS}} = \frac{e}{X_d}
\] (5)

\[
C_{S,inv}(V_{GS}) = \frac{dQ_{inv}(V_{GS})}{dV_{GS}}\quad Q_{inv}(V_{GS}) = -q \int n(x, V_{GS}) dx,
\] (6)

\[
n(x, V_{GS}) = n_{sub} \exp \left( \frac{\psi(x, V_{GS})}{V_{TH}} \right)
\] (7)

\[
\psi(x, V_{GS}) = \psi_s(V_{GS}) \left( 1 - \frac{x^2}{X_d^2} \right)
\] (8)

\[
C_{S,eff}(V_{GS}) = \frac{dQ_{eff}(V_{GS})}{dV_{GS}} = \frac{e}{X_d}
\] (9)

\[
Q_{eff}(V_{GS}) = -q \int_{V_T}^{V_{GS}} D_{eff}(x, V_{GS}) dx + q \int_{V_{TH}}^{V_{GS}} D_{ox}(x, V_{GS}) dx
\] (10)

\[
C_{S,dox}(V_{GS}) = \frac{dQ_{dox}(V_{GS})}{dV_{GS}}
\] (11)

\[
Q_{dox}(V_{GS}) = qX_{dox}(E_d) = q \int_{V_{GS}}^{V_{GS1}} g_d(E) dE - \int_{V_{GS}}^{V_{GS2}} g_s(E) dE
\] (12)

We note that \( C_{ox}, C_{S,dep}, C_{S,inv}, C_{S,eff}, C_{S,dox}, I_{Do}, V_{TH}, X_d, Q_{inv}, Q_{dox}, m(V_{GS}), g(E) \) as the oxide capacitance per unit area, the depletion capacitance of substrate, the gate bias-dependent substrate inversion capacitance, the capacitance by interface trap charge, the capacitance by bulk trap charge, the threshold current, the thermal voltage, the depletion width, the mobile charge, the interface charge, the at VGS-dependent body coupling factor and sub-gap density of states, respectively. If \( \Delta V_{GS} \) as the voltage step in the experimental data is sufficiently small, \( m(V_{GS}) \) and \( m(V_{GS}) + \Delta V_{GS} \) can be assumed to be almost the same for the effective surface potential. Therefore, \( \psi_{S,eff} \) can be derived through

\[
V_{GS} = V_{FB} + \psi_s + \psi_{ox} + \psi_{S,eff} \equiv \psi_{ox} + \psi_{S,eff}(\psi_s \ll \psi_{ox} + \psi_{S,eff})
\] (13)

\[
\psi_{S,eff}(V_{GS}) = \frac{E_{FB}(V_{GS}) - E_0}{q} = \frac{V_{GS} - V_{FB}}{m(V_{GS})V_{TH}}
\] (14)

with \( \psi_s \) as the potential drop across the gate, \( \psi_{ox} \) as the potential drop across the gate oxide, and \( V_{FB} \) as the flat-band voltage. We note that \( E_{FB} = E_{FB}(V_{GS} = V_{FB}) \) is defined as the Fermi energy at the flat band state as shown in Fig. 2. As a function of \( \psi_{S,eff} \), therefore, the subthreshold current \( I_{D,sub} \) can be re-described as

\[
I_{D,sub}(V_{GS}) = I_{Do} \exp \left( \frac{\psi_{S,eff}(V_{GS}) + V_{FB} - V_T}{m(V_{GS})V_{TH}} \right)
\] (15)

and therefore, \( \psi_{S,eff} \) can be described as

\[
\psi_{S,eff}(V_{GS}) = V_{TH} \left( \frac{\ln I_{D,sub}(V_{GS})}{I_{Do}} - \frac{V_{FB} - V_T}{m(V_{GS})V_{TH}} \right).
\] (16)

By differentiating Eq. (14) with respect to \( V_{GS} \), we obtain

\[
\frac{\partial \psi_{S,eff}(V_{GS})}{\partial V_{GS}} = V_{TH} \frac{\partial \ln I_{D,sub}(V_{GS})}{\partial V_{GS}} - \frac{(V_{FB} - V_T)|m(V_{GS})|}{m^2(V_{GS})} \frac{\partial m(V_{GS})}{\partial V_{GS}}.
\] (17)

**Fig. 1.** (a) Device structure. (b) Double sweep \( I_{DS}–V_{GS} \) characteristics and the flat band voltage is extracted to be \( V_{FB} \sim -2.6 \) V by the transconductance extrapolation method.
Therefore, \( \psi_{\text{S,eff}}(V_{\text{GS}}) \) for a nonlinear mapping of the gate bias to the trap energy level can be experimentally obtained from the \( I_{\text{DS}}-V_{\text{GS}} \) curve through

\[
\psi_{\text{S,eff}}(V_{\text{GS}}) = \int_{V_{\text{th}}}^{V_{\text{GS}}} \left( \frac{\partial \psi_{\text{S,eff}}(V_{\text{GS}})}{\partial V_{\text{GS}}} \right) dV_{\text{GS}} = \int_{V_{\text{th}}}^{V_{\text{GS}}} \left[ \frac{\partial \ln(I_{\text{D,sub}}(V_{\text{GS}}))}{\partial V_{\text{GS}}} \left( \frac{V_{\text{T}} - V_{\text{t1}}}{m(V_{\text{GS}})} \right) \right] dV_{\text{GS}}.
\]

(18)

In the previous study [16], the second term in Eqs. (17) and (18) was neglected due to the negligible value in InGaAs-OFETs. Finally, experimentally obtained effective surface potential \( \psi_{\text{S,eff}}(V_{\text{GS}}) \) is shown in Fig. 3 as a function of \( V_{\text{GS}} \) with \( V_{\text{FB}} < V_{\text{GS}} < V_{\text{T}} \). Therefore, \( \psi_{\text{S,eff}} \) increases in the low bias region and becomes saturated near the \( V_{\text{T}} \), which is normal behavior in the MOSFETs. As a result, we successfully obtained the non-linear mapping of \( V_{\text{GS}} \) to \( \psi_{\text{S,eff}} \) for the mapping to the trap level \( E_t \) only with the experimental subthreshold \( I-V \) characteristics.

4. Extraction of the interface traps from the subthreshold differential body coupling factor

With the equivalent circuit shown in Fig. 4, we expect that the depletion capacitance \( (C_{\text{S,dep}}) \) of the gate region is much larger than the oxide capacitance \( (C_{\text{ox}}) \) for the gate insulator (GI: \( C_{\text{G,I}} \gg C_{\text{ox}} \)). The interface state capacitance \( (C_{\text{G,I}}) \) at the gate-GI junction is in parallel with \( C_{\text{G,I}} \). Therefore, the voltage drop across them \( (C_{\text{G,I}} + C_{\text{G,I}}) \) is negligible. We also note that the substrate capacitance \( (C_{\text{S,sub}}) \) caused by the bulk traps (sub-gap density-of-states: DOS) in the InGaAs channel layer is negligible because the InGaAs/GaAs channel layer is an epitaxial-grown high quality layer.

With a simplified equivalent circuit in Fig. 4, \( m(V_{\text{GS}}) \) with \( C_{\text{S,eff}}(V_{\text{GS}}) \) can be expressed by

\[
m(V_{\text{GS}}) = 1 + \frac{C_{\text{S,dep}} + C_{\text{S,sub}}(V_{\text{GS}}) + C_{\text{S,eff}}(V_{\text{GS}})}{C_{\text{ox}}}
\]

(19)

with \( C_{\text{S,dep}}, C_{\text{S,inv}}(V_{\text{GS}}), C_{\text{S,sub}}(V_{\text{GS}}), \) and \( C_{\text{S,sub}}(V_{\text{GS}}) \) as the depletion, inversion, interface, and bulk DOS capacitances, respectively. We note that \( C_{\text{S,dep}} \) is assumed to be constant in fully depleted MOSFETs with a thin active layer and \( C_{\text{S,sub}}(V_{\text{GS}}) \) is negligible in the subthreshold region. \( C_{\text{S,sub}}(V_{\text{GS}}) \) is also negligible due to epitaxially grown high quality InGaAs channel. Therefore, \( C_{\text{S,eff}}(V_{\text{GS}}) \) is the only term governing the body coupling factor dependence on \( V_{\text{GS}} \). By differentiating Eq. (19) with respect to \( V_{\text{GS}} \), the relationship between \( m(V_{\text{GS}}) \) and \( C_{\text{S,eff}}(V_{\text{GS}}) \) can be modified as

\[
\frac{\partial m(V_{\text{GS}})}{\partial V_{\text{GS}}} \cong \frac{1}{C_{\text{ox}}} \frac{\partial \psi_{\text{S,eff}}(V_{\text{GS}})}{\partial V_{\text{GS}}} \frac{C_{\text{S,eff}}(V_{\text{GS}})}{\partial V_{\text{GS}}}
\]

(20)

Therefore, \( m(V_{\text{GS}}) \) is experimentally obtained through the Eq. (21) and expressed by

\[
m(V_{\text{GS}}) = \frac{\Delta V_{\text{GS}}}{V_{\text{th}}} \frac{C_{\text{ox}}}{\ln \left( \frac{I_{\text{D,sub}}(V_{\text{GS}} + \Delta V_{\text{GS}})}{I_{\text{D,sub}}(V_{\text{GS}})} \right)}.
\]

(22)

We finally obtain the distribution of \( D(E) \) from the experimental \( I-V \) data in the subthreshold region through

\[
\frac{\partial C_{\text{S,eff}}(V_{\text{GS}})}{\partial \psi_{\text{S,eff}}} = C_{\text{ox}} \frac{\partial m(V_{\text{GS}})}{\partial V_{\text{GS}}} \left| \frac{\partial \psi_{\text{S,eff}}(V_{\text{GS}})}{\partial V_{\text{GS}}} \right|
\]

(23)

\[
D(E) = \frac{\Delta C_{\text{S,eff}}(V_{\text{GS}})}{q^2} = \frac{C_{\text{ox}}}{q^2} \left| \frac{\partial m(V_{\text{GS}})}{\partial V_{\text{GS}}} \right| \left| \frac{\partial \psi_{\text{S,eff}}(V_{\text{GS}})}{\partial V_{\text{GS}}} \right| \Delta V_{\text{GS}}
\]

(24)

with \( \Delta \psi_{\text{S,eff}} = \psi_{\text{S,eff}}(V_{\text{GS}} + \Delta V_{\text{GS}}) - \psi_{\text{S,eff}}(V_{\text{GS}}) \). For a non-linear mapping of the gate bias \( (V_{\text{GS}}) \) to the trap level \( (E_t) \) through the effective surface potential \( \psi_{\text{S,eff}} \), we used...
E_{i(V_{GS})} = E_f + \frac{E_g}{2} - q\psi_f + q\psi_{eff}(V_{GS})  \quad (25)

with \(E_f\), \(E_g\), and \(q\psi_f\) as the valence band maximum, the band gap, \(q\psi_f = kT \times \ln(p_{sub}/n_i)\), \(n_i\) as the intrinsic carrier concentration, and \(p_{sub} = n_{A}\) as the substrate hole concentration in the In_{0.53}Ga_{0.47}As channel region, respectively.

5. Experimental result

We characterized the interface state distribution through the proposed subthreshold current technique for the bottom-gate In_{0.53}Ga_{0.47}As–On-Insulator MOSFETs with wafer bonded on Si wafer. Experimentally obtained and fitted data of \(m(V_{GS})\) are shown in Fig. 5(a). Fig. 5(b) shows the distribution of \(D_{it}(E)\) at the Al_{2}O_{3}/In_{0.53}Ga_{0.47}As interface in In_{0.53}Ga_{0.47}As channel III–V–OI MOSFETs with \(W/L = 100/50, 100/25,\) and \(100/10 \mu m/\mu m\). Extracted \(D_{it}(E)\) increases as the \(E_f\) decreases to the conduction band edge. \(D_{it}(E)\) values were ranged from \(10^{11}\) to \(10^{12}\) eV\(^{-1}\) cm\(^{-2}\) over the forbidden bandgap of the In_{0.53}Ga_{0.47}As channel layer and we confirmed that \(D_{it}(E)\) values from the proposed method were similar to the results from other groups for the similar structure [19]. Also, extracted \(D_{it}(E)\) distribution was almost same for devices with different dimensions, indicating the validity of the applied \(D_{it}(E)\) extraction technique only with the fully subthreshold current characteristics. Finally, as shown in Fig. 5(b), we comparatively verified the extracted \(D_{it}(E)\) through the proposed technique with that through the Terman method using a large area MOS capacitor (Au/Al_{2}O_{3}/n-In_{0.53}Ga_{0.47}As). We used the conventional semi-classic model to determine the ideal C-V curve. To calculate the carrier concentration and potentials, we used the Poisson’s equation combined with the Boltzmann distribution and the parabolic band model considering only the \(\Gamma\)-valley in the conduction band [10]. Therefore, we obtained a similar \(D_{it}(E)\) distribution as a function of the energy. We note that the proposed technique is fully subthreshold current-based and, therefore, is fully applicable to extraction of the interface states \((D_{it}(E))\) at the Al_{2}O_{3}/InGaAs heterojunction interface in extremely scaled In_{0.53}Ga_{0.47}As channel III–V–OI MOSFETs. On the other hand, the Terman method is based on the \(C-V\) characteristics and requires a large geometry device for MOS structures. Due to a limited availability of III–V–OI MOSFETs, which are focused on the fully current-based characterization technique, III–V–OI MOSFETs are not large enough applicable to the \(C-V\) characterization in the Terman method. Therefore, we employed MOS capacitors with different epitaxial structure and fabrication process from the III–V–OI MOSFETs with small geometry suitable for the proposed fully current-based characterization. We note that the difference in the extracted \(D_{it}(E)\) through the proposed technique compared with the result from the Terman method comes from the different epitaxial structure and/or different gate metals in MOSFET and MOSCAP [20] employed in the experiment.

6. Summary

We reported a fully subthreshold current-based technique for extraction of the interface states \((D_{it}(E))\) at the Al_{2}O_{3}/InGaAs heterojunction interface in the In_{0.53}Ga_{0.47}As channel III–V–OI MOSFETs. We successfully obtained \(D_{it}(E)\) near the conduction band edge \((E_c)\) without a channel length dependence. Since only the subthreshold \(I-V\) characteristics are employed both for \(D_{it}(E)\) and for the nonlinear mapping of the gate bias \((V_{GS})\) to the trap level \((E_f)\) via the effective surface potential \((\psi_{eff})\), we expect that the proposed technique will offer instructions for future development of high performance devices in these fields.

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