Impact of Ground Plane Doping and Bottom-Gate Biasing on Electrical Properties in $In_{0.53}Ga_{0.47}As$-OI MOSFETs and Donor Wafer Reusability Toward Monolithic 3-D Integration With $In_{0.53}Ga_{0.47}As$ Channel

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***Abstract*— In this paper, we fabricated $In_{0.53}Ga_{0.47}As$-on insulator (OI) MOSFETs on Si substrates with different doping types to mimic ground plane doping using direct wafer bonding and epitaxial lift-off (ELO) techniques. We investigated the impact of doping types on the ground plane and the backgate biasing, which are important and preferable components in monolithic 3-D (M3D) integration, on the electrical properties of MOSFETs, such as the threshold voltage (V_T) and the effective mobility (μ_{eff}). It was found that V_T and μ_{eff} were significantly modulated by the back-substrate doping and the backbiasing. These observations were explained by the change of carrier distributions, which were confirmed by technology computer-aided design simulation. Furthermore, we investigated the reusability of InP donor substrates for sequential epitaxial growth after ELO process toward a cost-effective M3D integration with the $In_{0.53}Ga_{0.47}As$ channel.**

***Index Terms*— III–V, compound semiconductor, epitaxial lift-off (ELO), InGaAs, InGaAs-OI, monolithic 3-D (M3D), MOSFETs, wafer bonding, wafer reuse.**

I. Introduction

MONOLITHIC 3-D (M3D) integration has received much attention from the industry as well as academia due to their benefits in high integration density of devices and the reduction of power consumption via vertical device stacking [1]–[3]. Moreover, an interconnection delay can be reduced by minimizing the resistance of interconnection wires [4]. On the other hand, in terms of the fabrication process for the M3D integration, a low-temperature processing is necessary to fabricate devices to protect bottom devices during the fabrication of top devices. From this aspect, high mobility channels, such as III–V compound semiconductors and Ge, have a strong advantage, because processing temperature for them is typically lower than 400 °C [4]–[10]. Among III–V compound semiconductors, InGaAs has been actively studied as a channel material for n-FETs of the next node logic applications, because InGaAs has quite attractive characteristics of high effective mobility and injection velocity than those of silicon [8]–[18]. There are several methods for stacking the InGaAs channel toward the M3D integration, such as the direct epitaxial growth, the aspect ratio trapping, the confined epitaxial lateral overgrowth, and the direct wafer bonding (DWB) [6]–[12], [14], [16]–[18]. Among these methods, the DWB using an oxide bonding material is the most straightforward and the best way to stack high-quality films at low process temperature for M3D, because the epitaxy-based

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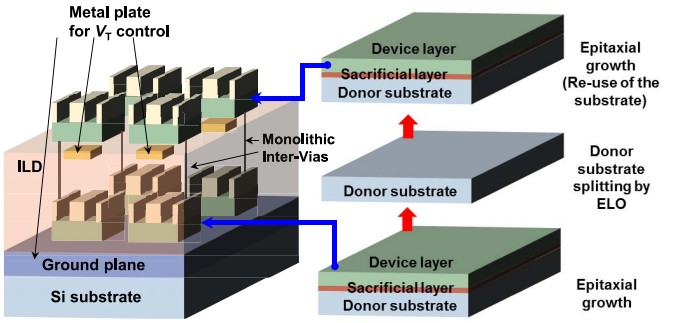

Fig. 1. Schematic of M3D integration with the InGaAs channel and its stacking flow. The proposed integration concept includes the ground plane and the metal plate in ILD for V_T control and the use of DWB/ELO) for donor wafer reuse.

method needs high process temperature, typically over 500 °C, during the growth of the channel layer. Fig. 1 shows the schematic of M3D integration with the InGaAs channel and its stacking flow of the DWB and the epitaxial lift-off (ELO) with a donor-wafer recycling.

A stacked structure by oxide bonding naturally has a backgate structure of the metal plate and the doped ground plane in top-level device (>2nd tier) and bottom-level device, respectively. As observed in SOI devices, a ground plane plays an important role in the control of the short-channel effect, the mobility, and the threshold voltage (V_T) in MOSFETs [19]–[21]. However, there are quite limited studies on these issues in InGaAs-OI MOSFETs [22]. Here, the metal plates patterned in the interlayer dielectric (ILD) seem to affect the wafer bonding, but the wafer with an additional oxide can be used for sequential wafer bonding after surface planarization. Moreover, hybrid bonding with a mixed pattern of metal and also oxide can be the viable solution to fabricate stacked structure even for higher tier device layers (second tier and above).

On the other hand, to explore M3D with the InGaAs channel, cost issues are quite problematic, because III–V substrate is typically more expensive than Si. Therefore, the M3D process design with the InGaAs channel must take account of the integration route for the process cost reduction.

In this paper, we demonstrated InGaAs-OI MOSFETs on Si substrates with different doping types to mimic the ground plane doping using the DWB and the ELO process [7]–[10]. We systematically investigated the impact of the ground plane doping and the backgate bias on the electrical characteristics. Furthermore, we investigated the wafer reusability of the InP donor wafer after the ELO process for a cost-effective M3D integration.

II. Fabrication of $In_{0.53}Ga_{0.47}As$-OI MOSFETs

Fig. 2(a) shows a schematic of the device structure and the fabrication process flow. To fabricate $In_{0.53}Ga_{0.47}As$-OI MOSFETs, first, we fabricated $In_{0.53}Ga_{0.47}As$-OI wafer via the DWB and the ELO processes [7]. Device layers were composed of a 20-nm-thick $In_{0.53}Ga_{0.47}As$ channel [unintentionally doped (UID)], a 5-nm-thick InP etch stop (UID), and a 50-nm-thick n^+ $In_{0.53}Ga_{0.47}As$ contact

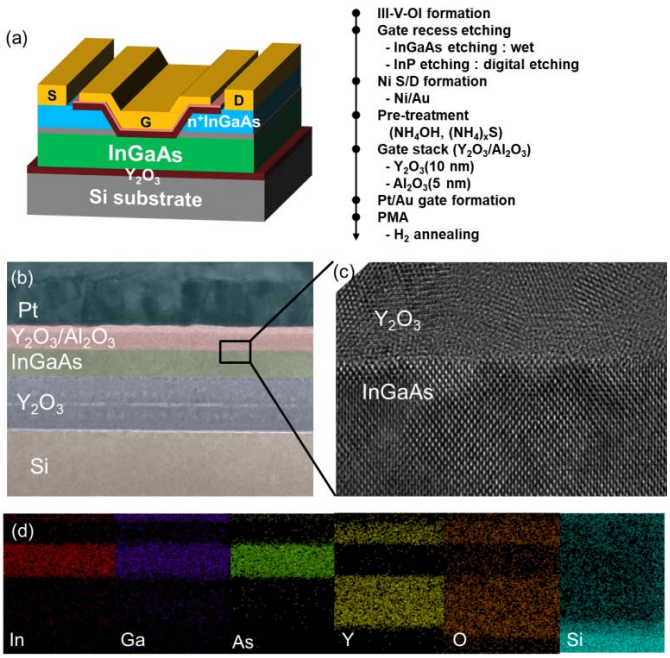

Fig. 2. (a) Schematic of the device structure and fabrication process of $In_{0.53}Ga_{0.47}As$-OI MOSFETs. (b) Cross-sectional TEM image of $In_{0.53}Ga_{0.47}As$-OI MOSFETs. (c) High-resolution cross-sectional TEM image of $In_{0.53}Ga_{0.47}As$ region. (d) EDX mapping profile of $In_{0.53}Ga_{0.47}As$-OI MOSFETs.

layer ($N_D \sim 1 \times 10^{19}$ cm^{-3}) from the bottom side. In this paper, we used a channel thickness of 20 nm, but a thinner channel thickness less than 10 nm will be needed to achieve a good short-channel effect control. In that channel thickness regime, a channel thickness fluctuation scattering will also impact on the mobility characteristics. Therefore, forming uniform InGaAs layer and/or introducing quantum well structure will be helpful to further explore these kinds of InGaAs-OI devices [14], [23]–[25]. Furthermore, introducing Fin structure even in III–V-OI will provide a better electrostatics [26]. Next, n^+ $In_{0.53}Ga_{0.47}As$ was recessed in gate regions by a citric acid. Subsequently, InP was recessed by digital etching using O_2 plasma and the HF solution. Then, Ni/Au was deposited for the source and drain contacts [27], [28]. Before the gate-stack formation, the wafer was cleaned by acetone, NH_4OH, and $(NH_4)_xS$ solutions to remove the native oxide and to passivate the surface by sulfur (S) atoms. As a gate dielectric, 10-nm-thick Y_2O_3 and 5-nm-thick Al_2O_3 were deposited. Here, the equivalent oxide thickness of the gate-stack was 4.6 nm, which can be further scaled by thickness thinning and/or using higher k second layer materials instead of Al_2O_3. In this process, we first formed S/D contacts and then carried out gate-stack formation, but this sequence can be changed with slight process modification. The gate metal (Pt/Au) was formed by the electron-beam evaporation, followed by the thermal annealing at 300 °C for 30 min in H_2 ambient [29]. A cross-sectional transmission electron microscope (TEM) image of fabricated $In_{0.53}Ga_{0.47}As$-OI MOSFETs is shown in Fig. 2(b). It clearly shows the gate-stack and $In_{0.53}Ga_{0.47}As$-OI on Si with a sharp MOS interface. High-resolution image of $In_{0.53}Ga_{0.47}As$ regions confirmed a high quality of the bonded $In_{0.53}Ga_{0.47}As$ film and clean MOS interface, as shown

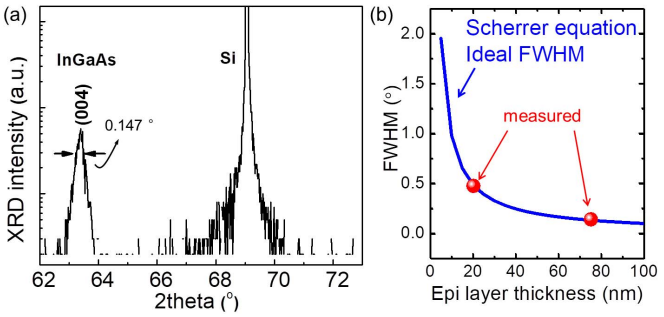

Fig. 3. (a) XRD spectra of $In_{0.53}Ga_{0.47}As/Y_2O_3/Si$ substrates. (b) Ideal and measured FWHM of XRD peak as a function of layer thickness.

in Fig. 2(c). An energy-dispersive X-ray spectroscopy (EDX) mapping image of the device in Fig. 2(d) highlights the atomic distributions of devices, showing sharp MOS interfaces of the top and bottom of the $In_{0.53}Ga_{0.47}As$ channel.

To examine the crystal quality of bonded $In_{0.53}Ga_{0.47}As$-OI, we measured X-ray diffraction (XRD) spectra of the sample. Fig. 3(a) showed the XRD spectra of transferred $In_{0.53}Ga_{0.47}As$/InP/ $In_{0.53}Ga_{0.47}As$ layer (50/5/20 nm) on Si layer. Clear two peaks were found at 63.4° and 69.2°, corresponding to the peaks from $In_{0.53}Ga_{0.47}As$ and Si, confirming the high quality of $In_{0.53}Ga_{0.47}As$-OI on the Si structure. Furthermore, we extracted the full-width half-maximum (FWHM) of the $In_{0.53}Ga_{0.47}As$ peak and plotted it in an ideal FWHM value calculated by Scherrer's equation as a function of the film thickness in Fig. 3(b). The peak from the thin film with a thickness of 20 nm is also shown. Measured FWHM points clearly ride on the ideal line, showing that the DWB and the ELO process allow almost perfect crystal.

III. Electrical Characteristics of $In_{0.53}Ga_{0.47}As$-OI MOSFETs

Electrical characterization was carried out for the fabricated $In_{0.53}Ga_{0.47}As$-OI MOSFETs. Fig. 4 shows the typical drain current (I_{DS})–gate voltage (V_{GS}) and I_{DS}–drain voltage (V_{DS}) characteristics of the $In_{0.53}Ga_{0.47}As$-OI MOSFETs with a gate length (L_G) of 100 μm fabricated on n^+ and p^+ Si substrates, respectively. Here, the resistivity of n^+ and p^+ Si were both around 0.005 $\Omega \cdot$ cm. N^+ and p^+ Si was doped by arsenic and boron, respectively. Thickness was 525 $\pm$ 20 μm. For both samples, well-behaved transfer characteristics were observed with the ON/OFF ratio of 10^5–10^6. Also, output curves show a clear current saturation [Fig. 4(b) and (d)]. It was found that threshold voltage (V_T) of the device on n^+ Si substrates is more negative than that of the device on p^+ Si substrates. Decreased Fermi level of n^+ Si substrates makes efficient channel formation, resulting in negative V_T shift. Consistently, lower OFF-current was obtained in the device on p^+ Si substrates. Extremely low OFF-current of approximately 10^{-13} A/μm is found in Fig. 4(c). Furthermore, I_{DS} itself at the same gate overdrive (V_{GS}–V_T) is larger in the device on n^+ Si substrate than that on p^+ Si substrates, as shown in Fig. 5(a).

To compare the transport characteristics of $In_{0.53}Ga_{0.47}As$-OI MOSFETs on n^+ and p^+ Si substrates, we evaluated

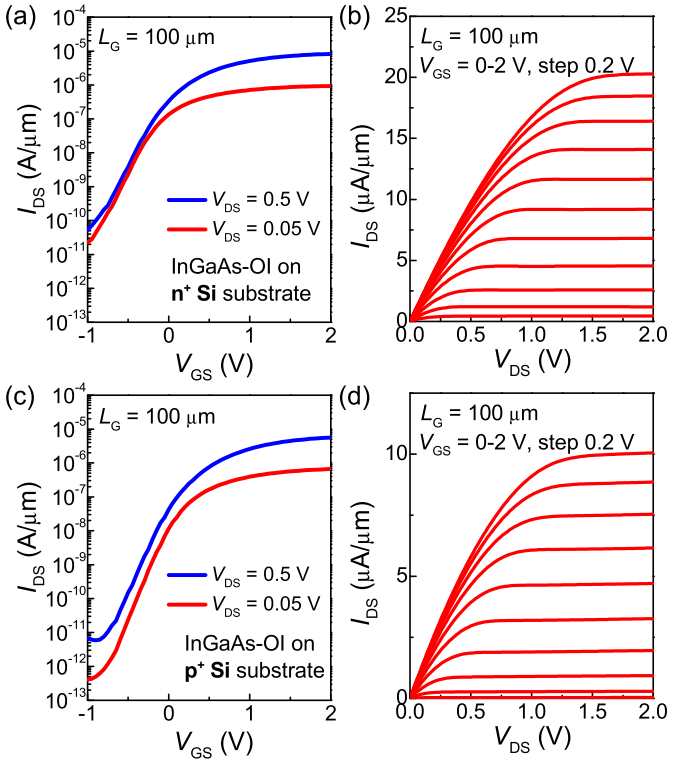

Fig. 4. (a) Transfer and (b) output characteristics of $In_{0.53}Ga_{0.47}As$-OI MOSFETs with L_G of 100 mm on n^+ Si substrate. (c) Transfer and (d) output characteristics of $In_{0.53}Ga_{0.47}As$-OI MOSFETs with L_G of 100 mm on p^+ Si substrate. Good transfer and output characteristics were observed and on/off ratio of 10^5–10^6.

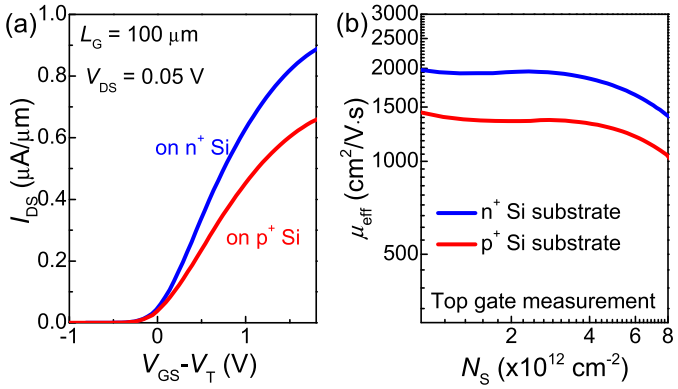

Fig. 5. (a) I_{DS} curves of $In_{0.53}Ga_{0.47}As$-OI MOSFETs on n^+ and p^+ Si substrates as a function of overdrive voltage. (b) The m_{eff} characteristics of $In_{0.53}Ga_{0.47}As$-OI MOSFETs on n^+ and p^+ Si substrates. m_{eff} of devices on n^+ Si substrates is about 33% higher than that of devices on p^+ Si substrates.

the effective mobility (μ_{eff}) in Fig. 5(b), which showed μ_{eff} in the $In_{0.53}Ga_{0.47}As$-OI MOSFETs on n^+ and p^+ Si substrates as a function of the sheet charge density (N_s). Here, Ns was estimated by $C_{ox} \cdot (V_{GS}–V_T)$, where C_{ox} is oxide capacitance measured from control capacitor fabricated on n-$In_{0.53}Ga_{0.47}As$ ($N_D = 5 \times 10^{16}$ cm^{-3}) to exclude the effect of parasitic capacitance in present devices. We obtained μ_{eff} of approximately 2000 and 1500 cm^2/V $\cdot$ s at N_s of 1.2 $\times$ 10^{12} cm^{-2} for n^+ Si and p^+ Si substrates, respectively. The μ_{eff} characteristics of the device on n^+ Si showed 33% higher mobility than that of the device on p^+ Si. To further investigate

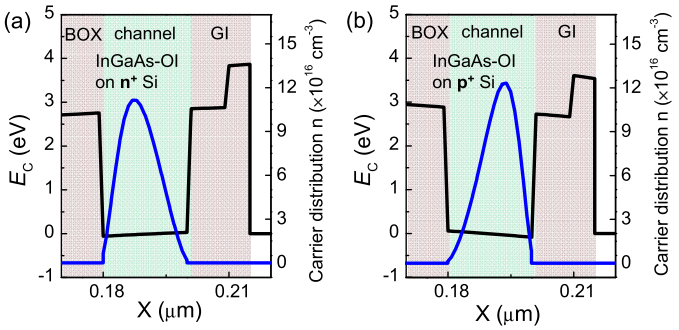

Fig. 6. Conduction band alignment and carrier distribution of $In_{0.53}Ga_{0.47}As$-OI MOSFETs on (a) n^+ and (b) p^+ Si substrates.

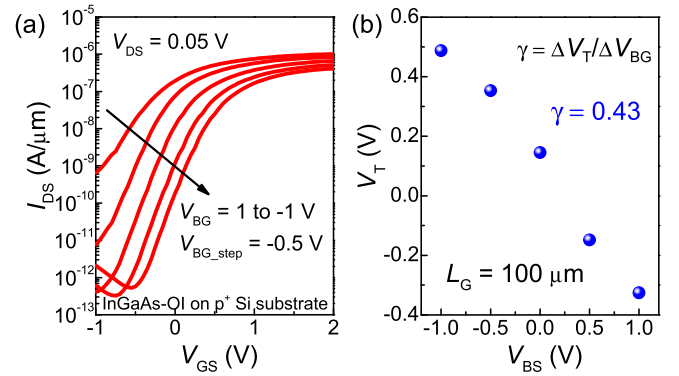

Fig. 7. (a) Transfer curves of $In_{0.53}Ga_{0.47}As$-OI MOSFETs on p+ Si substrates with different V_{BG} values from 1 to −1 V. (b) V_{BG} dependence of V_T value in $In_{0.53}Ga_{0.47}As$-OI MOSFETs. Large body factor of 0.43 was obtained in the $In_{0.53}Ga_{0.47}As$-OI MOSFETs.

the physical origin of these phenomena, we calculated carrier distribution of $In_{0.53}Ga_{0.47}As$-OI MOSFETs on n^+ and p^+ Si by solving 1-D Poisson's and Schrodinger's equations using the technology computer-aided design (TCAD) simulator, Silvaco. Fig. 6(a) and (b) shows the conduction band alignment and the carrier distribution of the devices on n^+ Si and p^+ Si substrates, respectively. The carrier distribution of the devices on n^+ and p^+ Si substrates were quite different, which is caused by the difference of the Fermi energy level between n^+ and p^+ Si substrates. It was found that the carrier distribution of the device on n^+ Si is more in the centroid of the channel than that of devices on p^+ Si substrates. It would be derived that the carrier distributes more in the centroid of the channel and possibly helps to be less influenced by the carrier scattering at the MOS interface.

One interesting benefit of $In_{0.53}Ga_{0.47}As$-OI MOSFETs from their device structure is the V_T tunability, which gives more flexibility of circuit design and power management of the chip [30]. Fig. 7(a) shows the transfer curves of devices on p^+ Si substrates with changing the bottom gate bias (V_{BG}) from 1 to −1 V. With a decrease of V_{BG}, positive V_T shift was observed due to the potential change by V_{BG}. V_{BG} dependence of V_T value of $In_{0.53}Ga_{0.47}As$-OI is shown in Fig. 7(b). The body factor ($\gamma = \Delta V_T/\Delta V_{BG}$) was observed to be 0.43, which is very high compared with the reported values in SOI, GOI, and III-V-OI so far [26]–[31]. The γ value is typically decided by the ratio of C_{BG} and C_{TG}, where C_{BG} and C_{TG} are the

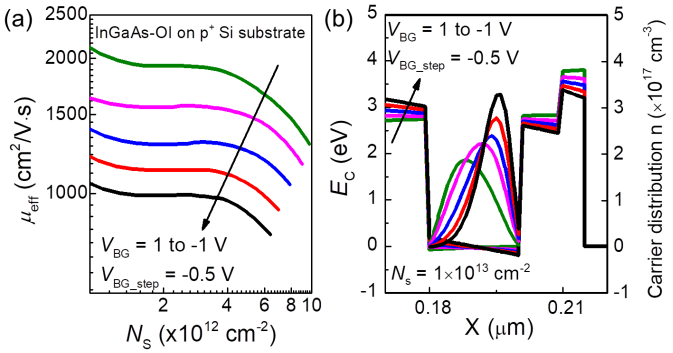

Fig. 8. (a) Effective mobility m_{eff} characteristics of $In_{0.53}Ga_{0.47}As$-OI MOSFETs on p+ Si substrates with different V_{BG} values from 1 to −1 V. (b) Simulated carrier distributions in $In_{0.53}Ga_{0.47}As$-OI MOSFETs at the same carrier concentration of 1×10^{13} cm^{-2} with V_{BG} of −1, −0.5, 0, 0.5, and 1 V.

bottom gate-to-channel capacitance and the top gate-to-channel capacitance. Since C_{BG}/C_{TG} was around 0.44 in our device, extracted γ value is quite reasonable. From this, it is assumed that buried oxide (BOX) thickness scaling allows further enhancement of the γ value directly.

Fig. 8(a) shows the μ_{eff} characteristics of $In_{0.53}Ga_{0.47}As$-OI MOSFETs with different V_{BG} values. The gradual decrease of μ_{eff} was observed with a decrease of V_{BG}, indicating that the relationship between μ_{eff} and V_{BG} should be considered to use bottom-gate biasing in the circuits. This μ_{eff} change by applying backgate biasing should be taken into account for active backgate biasing. It may make difficult to balance power consumption and high performance. However, forward (positive) and reverse (negative) backgate biasing are typically used to increase the performance (reduce V_{th}) and reduce the power consumption (increase V_{th}), respectively. In this line, our results indicate that μ_{eff} increases in the forward bias mode (high-performance mode), and OFF leakage current decreases in the reverse bias mode (low-power mode). Therefore, the impact of drive current reduction with a negative bias should not be so crucial if we consider corresponding operation mode. Of course, both V_{th} tuning and μ_{eff} change are very important and should be considered for the circuit design. Similarly, the ground plane doping should be considered depending on the application.

To understand these μ_{eff} behaviors, we simulated carrier distributions in the channel layer using TCAD. Fig. 8(b) shows the simulated carrier distributions of $In_{0.53}Ga_{0.47}As$-OI MOSFETs with different V_{BG} values at the same carrier concentration as 1×10^{13} cm^{-2}. Naturally, carrier distributions were significantly changed by applying V_{BG}. Carriers are more concentrated in the channel centroid when V_{BG} is changed from negative to positive, as shown in Fig. 8(b). These potential change would be the physical origin of the μ_{eff} change with V_{BG} by minimizing the effect from the Coulombic scattering at the MOS interface, as also shown in SOI and GOI MOSFETs [34], [35]. Here, we did not take into account the interface trap density (D_{it}) at the interface between Y_2O_3 and InGaAs, whereas a good MOS interface is very important to achieve high carrier mobility in thin body-OI channel devices [35]. However, the mobility behaviors with a

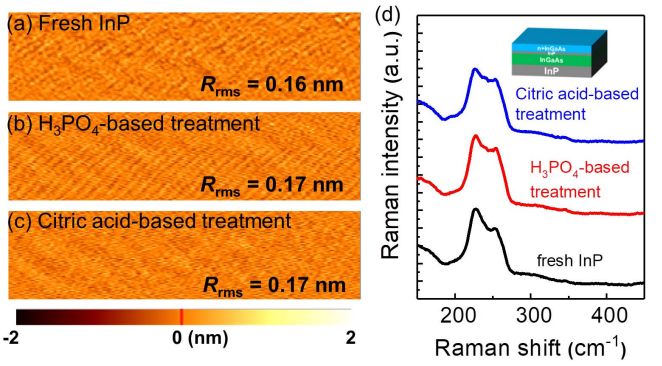

Fig. 9. AFM images of the $In_{0.53}Ga_{0.47}As$ surface grown on (a) fresh and regrown $In_{0.53}Ga_{0.47}As$ surface on reused InP substrates with (b) H_3PO_4- and (c) citric acid-based treatments before the epitaxial growth. (d) Raman spectra of the $In_{0.53}Ga_{0.47}As$ surface of the same sample for AFM measurement.

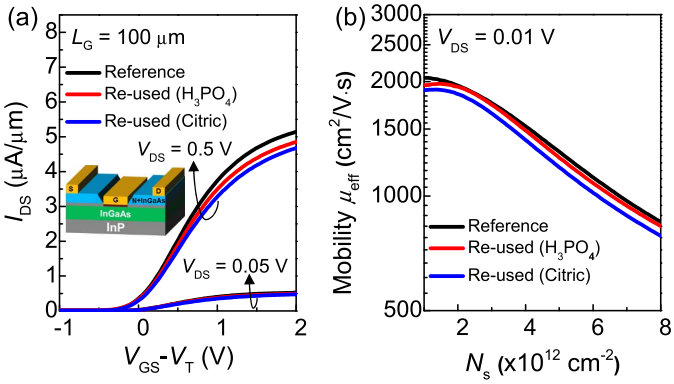

Fig. 10. (a) Transfer curves and (b) comparative effective mobility μ_{eff} characteristics of the $In_{0.53}Ga_{0.47}As$ grown on fresh and reused InP substrates.

different backgate biasing can still be explained by the relative carrier distribution across the channel layer, because the back-MOS interface and front MOS interface are the same as that of Y_2O_3/InGaAs and should have similar interfacial properties.

Considering physical dimension of the devices, thinner Y_2O_3 BOX will provide more sensitive change of the potential distribution, which leads to the change of μ_{eff}, as thinner BOX provides a larger body factor ($\gamma \propto C_{BG}/C_{TG}$).

Also, to address the cost issue of the III–V layer stacking, we investigated the wafer reusability of the InP donor wafer by treating the surface after ELO process. After growing the $In_{0.53}Ga_{0.47}As$/AlAs layer on InP, we mimicked the ELO process and removed all of the layers on InP with two different treatments of H_3PO_4-based and citric acid-based solutions. Sequentially, we repeated the epitaxial growth of the $In_{0.53}Ga_{0.47}As$ layers and the fabrication of MOSFETs on these treated wafers.

The quality of the epitaxial layers on the fresh and reused InP substrates was comparatively evaluated through the AFM image and the Raman spectra. Fig. 9(a)–(c) shows the AFM images of the fresh and reused wafers with two different treatments before the growth. They showed very smooth surface with R_{rms} of 0.16, 0.17, and 0.17 nm, indicating that a smooth epitaxial layer surface can be obtained even on the reused InP wafer. Fig. 9(d) shows the Raman shift of the reused wafer from the fresh wafer. The Raman shift of the $In_{0.53}Ga_{0.47}As$ layer grown on the reused wafers with both pretreatments before the epitaxial growth was comparable to that from the $In_{0.53}Ga_{0.47}As$ layer grown on the fresh InP wafer.

Finally, to investigate the electrical properties of the epitaxial layer grown on reused wafer, we fabricated typical $In_{0.53}Ga_{0.47}As$ on InP MOSFETs [28]. Fig. 10 showed transfer and mobility characteristics of devices from fresh and reused wafer, respectively. Transfer and mobility characteristics of device from reused wafer with H_3PO_4-based solution treatment showed almost comparable characteristics with that of the device from fresh wafer. These results indicate that wafer separated from the device layer during the ELO can be reused for a next epitaxial growth, which lead to dramatic cost reduction for the device layer stacking toward M3D integration with $In_{0.53}Ga_{0.47}As$ channel materials. However, that citric acid-based solution-treated sample shows slightly a smaller mobility than H_3PO_4-based solution-treated sample and the control sample on a fresh substrate, whereas surface morphology was almost the same. These results strongly indicate that surface roughness is not only impacting a factor for the epitaxial growth, and chemical termination or surface preparation before the growth is also an important factor for the reusability of the wafer after chemical treatment. We believe that dedicated surface preparation before the growth should be further explored, since this will also impact on the variability and reliability in short-channel devices.

IV. Conclusion

In this paper, we fabricated $In_{0.53}Ga_{0.47}As$-OI MOSFETs on n^+ and p^+ Si substrates using the DWB and the ELO processes and systematically investigated the effect of the ground plane doping (n^+ and p^+ Si) and the backgate biasing on electrical properties of devices. The ground plane doping, represented by the doping of the bottom Si substrate, and the backgate biasing greatly influence on V_T and effective mobility characteristics of devices as shown before. Furthermore, for cost reduction of $In_{0.53}Ga_{0.47}As$ stacking processes, we investigated the reusability of InP substrates for the sequential epitaxial growth. We obtained very smooth and sharp Raman spectra of the $In_{0.53}Ga_{0.47}As$ layer grown on a reused wafer. Fabricated $In_{0.53}Ga_{0.47}As$ MOSFETs grown on a reused InP wafer also showed almost identical transfer and mobility characteristics with those from the fresh InP wafer. We expect that the proposed scheme provides a possible tuning of mobility and V_T and cost-effective $In_{0.53}Ga_{0.47}As$-OI fabrication for M3D integration.

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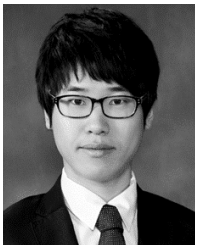

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