A capacitorless 1T-DRAM cell on independent double-gate FinFET

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Dynamic random access memory (DRAM) and embedded DRAM (eDRAM) manufacturers face a tremendous challenge to shrink the basic memory cell area as the technology feature size F continues to scale down. Therefore, capacitorless one-transistor (1T) DRAM has received a great deal of attention as a next-generation type of DRAM due to the lack of demand for intrinsically tall capacitor and simplified fabrication process. The previously reported operation principle of 1T-DRAM relies on a distinctive binary state by sensing excess holes in a floating body, which generally requires impact ionization with harsh bias conditions, such as a high gate and drain voltages [1]. This adversely leads to poor device reliability and corresponding short time retention.

In this work, we propose a new concept of 1T-DRAM based on independent double-gate (IDG) FinFET itself. It features a silicon fin implemented on a SOI wafer, a control gate (G1) for current driving, and a floating gate (G2) for charging sensing. We found that the significant threshold voltage (V_T) shift occurs in the IDG FinFET when the G2 is charged only by small bias (1.0 V) because there is no electrical path of the accumulated electrons of holes in G2. Our concept does not require high bias conditions and therefore results in long-term endurance after cyclic operations due to low bias conditions. Moreover, long retention time was obtained up to 10 min. Thus, the concept presented here will provide a new means of overcoming the limitations in conventional 1T-DRAM.

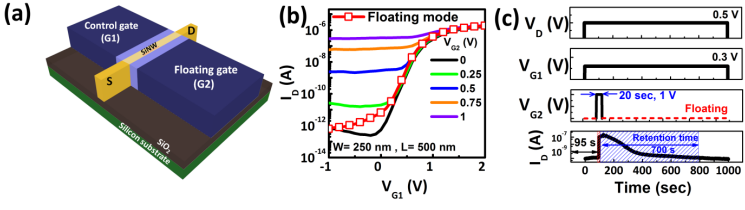

Fig. 1. (a) A schematic illustration of the independent double-gate FinFET for our 1T-DRAM concept (b) Transfer curves of independent double gate mode (V_{G2} = -1 V ~ 1V sweep) and floating mode (V_{G2} = floating) (c) Bias conditions for the evaluation of 1T-DRAM and characteristics of hold retention time

[1] S. Okhonin, *et al., IEEE Electron Device Lett*., vol. 23, no. 2, p. 85, 2002
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