[WC2-G-4]

Interfacial properties of Ge (111)/ La_2O_3 by Density Functional Calculations

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As silicon-based field-effect transistor (FET) technology is approaching its technological and physical limits, much research interest has been focused on channel material with high mobility, which can provide continued improvement in the performance of nanoscale MOSFETs [1]. Therefore, it becomes important to look at the higher mobility materials such as Ge to continue scaling of the MOSFET devices. For the Ge-based MOSFET technologies, the properties of high-k materials with Ge must be carefully studied and associated problems should be solved. Previous experiments have demonstrated the potential advantage of La_2O_3 dielectric on Ge substrates, with the high dielectric constant and large band offset for the conduction band and valence band [2]. It has been also reported that La_2O_3 layer can be epitaxially grown on Ge(111) without an interfacial GeO_2 layer [3, 4]. The GeO_2 interfacial layer is reported to be soluble in water and thermally dissolves into GeO_x above 425℃, resulting in degradation of the device performance [5].

In our study, we construct Ge(111)/La_2O_3 interface structure to investigate the atomic and electrical characterization. Electrical properties, such as interface state property, defect charge trapping, electron injection barrier and effects of the strain, are studied in detail for Ge(111)/La_2O_3 structures. The minimum thickness of La_2O_3 on Ge surface, at which the bulk conduction band offset between high-k layer and Ge still remains, are evaluated.

References

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[WC2-G-5]

Universal bias stress-induced instability model in the inkjet-printed carbon nanotube network FETs

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The inkjet-printed carbon nanotube (CNT) network field effect transistor (FET) is a fundamental building block for wearable, IoT, and macroelectronics era. The understanding of biass stress (BS) instability is indispensible for the manufacturing of CNT FET-based circuits and systems. However, the study on BS instability has been rarely carried out and somewhat diverse [1, 2]. In this paper, we propose the universal BS-induced instability model which successfully explains the instability mechanism on a negative bias stress (NBS, V_{GS}= −15 V) as well as a positive bias stress (PBS, V_{GS}= 15 V) in CNT FETs. The bottom gate structure CNT network FETs with p^+ Si gate and SiO_2 gate insulator (GI) were used in this study [Fig. 1(a)]. The BS instability in air ambient [Fig. 1(b)] was also compared with that in vacuum environment [Fig. 1(c)]. Based on TCAD simulation and the extraction of interface trap density (D_{it}), the universal BS model was established by consolidating three kinds of mechanisms: electron trapping into GI, generation /annihilation of D_{it} during BS, and the absorption/desorption of chemical species OH^-. Under NBS, the negative threshold voltage shift (ΔV_T) is dominated by the hole trapping into GI, which is more accelerated by the desorption of OH^- in vacuum. On the other hand, the positive ΔV_T under PBS is dominated by the electron trapping in GI, which is enhanced by the absorption of OH^- in air ambient [Fig. 1(d)]. Furthermore, it is noteworthy that the negative ΔV_T under PBS occurs especially in vacuum, which is due to the D_{it} generation [Fig. 1(d)]. Our result is expected to be useful for the robust design of CNT network FET-based circuits printed on flexible and/or wearable substrate.

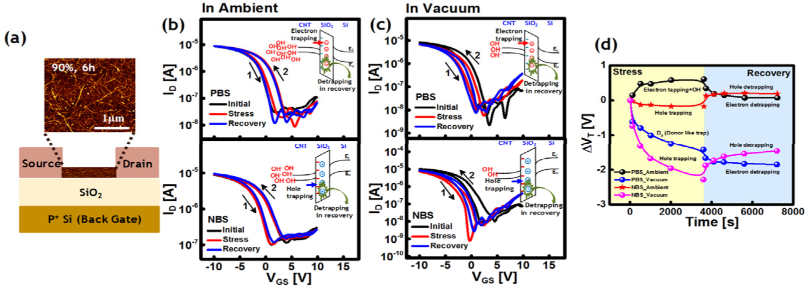

Fig. 1. (a) Schematic of the inkjet-printed CNT FETs. Bias stress/recovery time-dependence of transfer characteristics in (b) air ambient and (c) vacuum conditions. (d) Bias stress/recovery time-dependence ΔV_T.

References

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