[TC1-G-5]

A Trap Characterization Method for Float Body PMOSFET using Pulsed Drain Current Transient

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Floating body devices have drawn much attention due to high performance and scalability such as FinFETs and GAAFETs. However, the floating body device characterization methods are limited, especially trap detection techniques. We have introduced a trap characterization method for floating body PMOSET using pulsed drain current transients. Gate voltage setup was shown in Fig. 1. At pre-stress stage (A), hole traps was empty. Trapped holes at the high-k/Si interface and electrons injected from the gate in high-k during stage (B) would be neutralized by electrons generated in body at stage (C). The number of electrons needed for hole emission corresponds to number of holes detrapped at stage (C). The electron generation in body reduced drain current with time until all hole traps are empty again (see Fig. 2). Pulse stress voltage was varied to distinguish hole trap in high-k dielectric and interface. Random trapping-detrapping could be observed during relaxation.

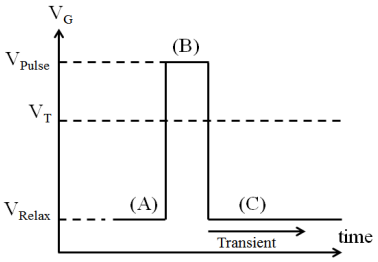

Fig. 1. Gate voltage set-up for DCTS

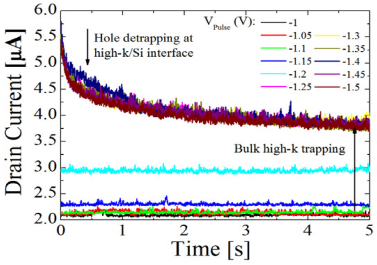

Fig. 2. Drain current transients with different stress voltage

Bulk traps in high-k dielectric could be separated from the interface trap states using the detrapping behaviors. Detrapping of interface states follows exponential rule because of exponential dependence of electron generation. Electrons trapped in high-k increase the drain current value by hole accumulation to keep the electric charge neutralization. The trapping or detrapping in bulk high-k causes a discrete change of drain current due to the local electric filed change (conduction path change). We have suggested an equation for the detrapping behaviours:

$$I_D = I_{D0} + \triangle I_{DB} + \sum_i \triangle I_{DI,i}\, e^{-\frac{t}{\tau_i}}$$

where I_D, I_{D0} , ΔI_{DB}, $\Delta I_{DI,i}$, t and τ_i are drain current, pre-stress drain current, drain current shift due to bulk trap states, drain current shift due to interface trap states, time after pulsing and emission time constant of hole traps. The negative sign of $\Delta I_{DI,i}$ correspond to detrapping with electron assistance. Trap density could be extracted using the linear relations between threshold voltage shift, drain current shift and trap density.

[TC1-G-6]

Influence of active layer thickness on the abnormal output characteristics in amorphous In-Ga-Zn-O TFTs under high current-flowing operation

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Thin-film transistors (TFTs) using amorphous In-Ga-Zn-O (a-IGZO) as channel layer material have attracted attention as one of promising candidates for large-area high-frame rate display backplanes for AMLCD and AMOLED displays [1]. Precise understanding of degradation mechanisms under high current-flowing operation is indispensable for manufacturing IGZO-driven displays [2]. However, the influence of active film thickness (T_{act}) on the high current-flowing degradations has been rarely studied although the T_{act} is a fundamental and important parameter to control the device parameters such as threshold voltage, on current, on/off current ratio, and subthreshold slope. In this study, we report and analyze the abnormal output characteristic and its T_{act}-dependence in a-IGZO TFTs whose T_{act} is modulated by varying only the sputtering deposition time among process conditions. Observed abnormal output curves of the devices (W/L=200/100 μm) with thin and thick (15 and 110 nm) T_{act}'s are shown in Fig. 1(a) and 1(b). To investigate the T_{act}-effect, the pulsed I-V measurement are used with varying either the duty or ON/OFF time of pulse which controls the temperature accumulated in active layer [Fig. 1(c)]. Analysis results are as follows: The combination of self-heating and charge trapping mechanism explains the abnormal output characteristics very well [Fig. 1(d)]. Degradation model is proposed, herein Joule heating becomes more accelerated with the decrease of T_{act} due to both higher resistance and higher drain current. Our result is potentially useful in the design and optimization of IGZO TFT structure for AMOLED displays driven by a very high current level.

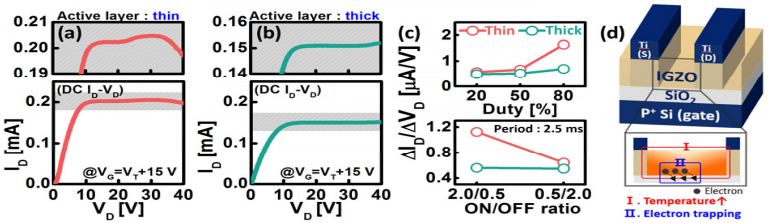

Fig. 1. Output characteristics with (a) thin and (b) thick T_{act}. (c) The maximum slope of pulsed output characteristics with varying duty and ON/OFF time of pulse. (d) Schematics illustrating the structure and abnormal characteristic model under the high gate voltage drain voltage in a-IGZO TFT

References

[1] T. Kamiya, et al., *Sci. Technol. Adv. Mater.*, vol. 11, p. 044305 (2010). [2] M. Mativenga, et al., *Appl. Phys. Lett.*, vol. 102, no. 2, p. 023503 (2013).

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