[TC3-G-6]

TCAD-based comparative study on the positive bias stress instability between the single-gate and double-gate structured In-Ga-Zn-O TFTs

Sungju Choi, Jun Tae Jang, Hara Kang, Jae-Young Kim, Daehyun Ko, Jihyun Rhee, Jun Tae Jang, Hye Ri Yu, Jisun Park, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim*

School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea

(E-mail : drlife@kookmin.ac.kr)

Recently, amorphous In-Ga-Zn-O (IGZO) thin-film transistor (TFT) has been employed as driving device in manufacturing the next-generation displays. Various IGZO TFT structures, such as the top-gate (TG), bottom-gate (BG), and double-gate (DG), have been investigated in terms of performance and stability. Although the observed better stability of DG TFTs than that of BG TFTs has been frequently attributed to the relaxation of electric-field [1, 2], it has been seldom quantitatively proven.
In this work, the origin on the superiority of positive bias stress (V_{GS}/V_{DS}=30 V/0 V) stability in DG TFT to BG TFT is quantitatively investigated by using TCAD simulation [3]. Although the PBS-induced ΔV_T of BG TFT ($\Delta V_{T,BG}$) is larger than that of DG TFT ($\Delta V_{T,DG}$) [Fig. 1(a), (b), and (c)], a simulation result shows the trapped charge density ($n_{trapped}$) in a top and bottom gate insulator is the same each other (TG, BG, and DG) [Fig. 1(e) and (g)]. It suggests the better stability of DG (compared with BG) is attributed not to an electric-field relaxation followed by less charge trapping but to the larger gate-coupling capacitance [Fig. 1(f)]. Our finding accounts for the more sophisticated design and optimization of DG a-IGZO TFTs.

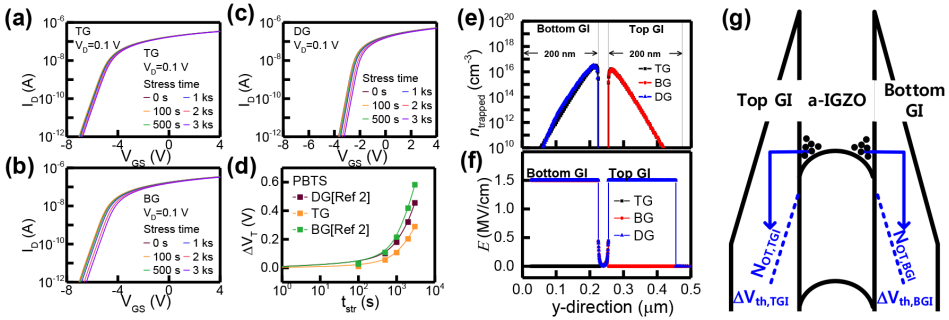

Fig. 1. I_D-V_G curves of (a) TG, (b) BG, and (c) DG IGZO TFTs. (d) The TCAD-simulated ΔV_T-t_{str} characteristic, (e) profile of trapped charges, (f) vertical electric field, and (g) schematic illustrating charge trapping mechanism.

References
[1] G. Baek, et. al., *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1109–1115, (2014), [2] X. He, et al., *SID 2015 Digest*, pp. 1151-1154(2015), [3] Atlas User's Manual, Silvaco (2016).

Acknowledgement
This work was supported by the National Research Foundation of Korea(NRF) Grant funded by the Korean Government(MSIP)(NRF-2016R1A5A1012966)

[TD3-E-1]

PECVD SiON for Normally-off AlGaN/GaN-on-Si Recessed MIS-HFETs

Hyun-Seop Kim[1], Sang-Woo Han[1], Won-Ho Jang[1], Kwang-Seok Seo[2], and Ho-Young Cha[1*]

[1]*School of Electronic and Electrical Engineering, Hongik University 94 Wausan-ro, Mapo-gu, Seoul, Republic of Korea, 04066*

[2]*Department of Electrical Engineering and Computer Science, Seoul National University 1 Gwanak-ro, Gwanak-gu, Seoul, Republic of Korea, 08826*

(E-mail : hcha@hongik.ac.kr)

In this study, we have developed a silicon oxynitride (SiON) deposition process using a plasma enhanced chemical vapor deposition system for the gate insulator of AlGaN/GaN metal-insulator-semiconductor heterostructure field-effect transistors (MIS-HFETs). A SiON insulator was deposited by using SiH_4, N_2O, and NH_3 mixtures as reactant gases. The refractive index increased with SiH_4 and NH_3 flow rate while it decreased with N_2O flow rate. The deposition conditions as follows; a gas flow rate of SiH_4/N_2O/NH_3 (=50/25/25 sccm), a source RF power of 100 W, a chamber pressure of 500 mTorr, a deposition temperature of 350°C. The fabricated device exhibited a excellent characteristics in terms of pulsed I-V and dynamic on-resistance characteristics ($R_{DS(on)}$), especially. We investigated the temperature dependent dynamic on-resistance of the fabricated device without a source field plate. The $R_{DS(on)}$ was increased by only 1.36 times at 200°C operation. It was found that a SiON gate insulator for use in normally-off AlGaN/GaN recessed MIS-HFETs had superior switching and reliability characteristics.

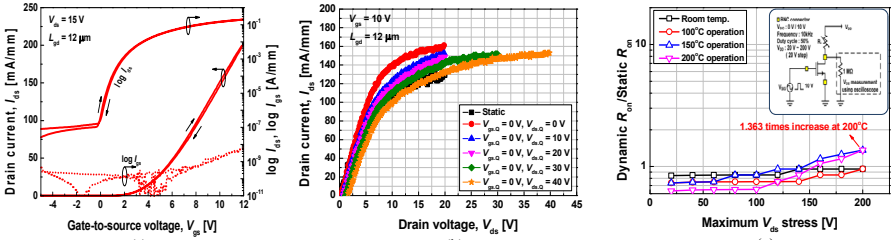

Fig. 1. (a) Transfer, (b) pulsed output, and (c) temperature dependent dynamic on-resistance characteristics of fabricated AlGaN/GaN-on-Si MIS-HFETs