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Study on Negative Bias Stress-induced Instability in Zinc Oxynitride Thin-Film Transistors using Systematic Decomposition

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Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) are subject of intensive research due to their high potential for application in switching and driving devices in liquid crystal displays and organic light emitting diode displays [1]. Especially, AOS TFTs with high-mobility are necessary for driving high resolutions and to reduce power consumption. Therefore, zinc oxynitride (ZnON) TFTs with very high mobility up to 110 $cm^2 / V{\cdot}s$ [2] are promising candidates for practical applications, and the electrical stability issue should be addressed in detail for these applications. In particular, since TFTs used as the switching elements of the display is mostly turned off, instability under negative bias stress (NBS) should be noted. In previous studies, the NBS instability has been reported to be due to one dominant mechanism without the quantitative analysis of various mechanisms. In this study, we report and analyze that the degradation mechanism under NBS by quantitatively decomposing the threshold voltage shift (ΔV_T) using the stress time-divided experimental method [3] in ZnON TFTs.

The ZnON TFTs with the inverted staggered bottom gate top-etch stopper structure are used in this study. The degradation mechanisms under NBS are the charge trapping in the gate insulator (GI) and the change in defect states in the active region (Act.) [Fig. 1(a)]. When the gate voltage of -30 V is applied for 10k seconds, negative ΔV_T is shown, and relatively small positive ΔV_T during the recovery time for 5k seconds [Fig. 1(b)]. Time-divided measurements including these experimental data are conducted for 0.1k, 2.0k, and 10k seconds of stress conditions, and the threshold voltage (V_T) and subthreshold slope (SS) shift are extracted from read-out with measurement time [Fig. 1(c)]. Consequently, we find out that hole trapping occurs in the GI and density of states (DOS) near the conduction energy edge is generated under NBS [Fig. 1(d)]. Additionally, hole trapping occurs more rapidly in time than creation of DOS in the active layer. Our study is useful for the further development and design of ZnON TFTs and for improving reliability.

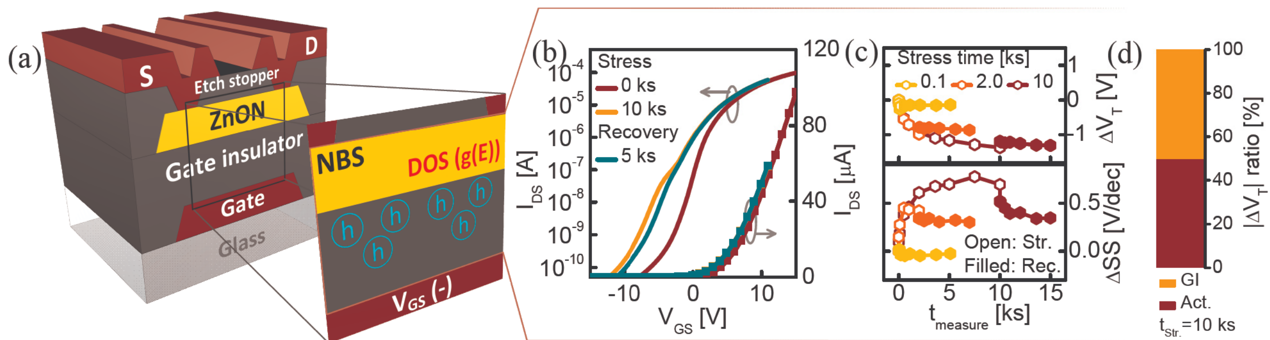

Fig 1. (a) Schematics 3D structure of ZnON TFT and cross-section view illustrating negative gate bias stress mechanisms, (b) Transfer characteristics during stress and recovery. (c) Threshold voltage shift and changed subthreshold slope extracted from stress-time-divided measurements at stress times (Str.) of 0.1 ks, 2.0 ks, and 10 ks with recovery time (Rec.) condition of 5.0 ks. (d) Quantitative analysis of decomposed $|\Delta V_T|$ by hole trapping and defect creation at stress time of 10 ks.

References: [1] E. Fortunato, et al., *Adv. Mater.,* vol. 24, pp. 2945-2986 (2012). [2] H. S. Kim, et al., *Scientific Reports* (2013). [3] S. Choi, et al., *IEEE Electron Device Lett.,* vol. 38, pp. 580-583 (2017).

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