Single-Electron Transistors with Sidewall Depletion Gates on an SOI Nanowire and Their Application to Single-Electron Inverters

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(Received 23 April 2002)

Single-electron transistors with sidewall depletion gates on a silicon-on-insulator (SOI) nanowire are proposed and were fabricated using a combination of conventional lithography and process technology. The island-size dependence of the electrical characteristics showed good controllability. Based on the high-voltage gain and the current peak position control by the sidewall gate voltage, the basic operation of a single-electron inverter was demonstrated at 12.5 K.

PACS numbers: 85.35.Gv, 73.23.Hk, 73.23.-b.
Keywords: Silicon-on-insulator, Sidewall, Depletion gate, Nanowire, Single-electron inverter

I. INTRODUCTION

Single-electron transistors (SETs) have recently attracted much attention for their potential as building blocks for ultra-high-density, low-power nanoelectronic integrated circuits. Among many approaches using various materials, Si-based SETs have a few advantages in terms of the maturity and the variety of the process technology. From the viewpoint of logic circuit applications, inherent limitations of SETs, such as no gain and low drivability, imply that realizable systems in the near future will probably be MOSFET-SET hybrid circuits [1]. Consequently, a fabrication method compatible with conventional CMOS process technology is strongly required for the purpose of integration with conventional MOSFETs.

In this paper, SETs with sidewall depletion gates on a silicon-on-insulator (SOI) nanowire are proposed. Such SETs were fabricated, using a combination of conventional lithography and process technology. The size dependence of the device characteristics showed good controllability. Based on the high-voltage gain and the current peak position control by using the sidewall depletion gates, the basic operation of a single-electron inverter was successfully demonstrated at 12.5 K.

II. FABRICATION AND ELECTRICAL CHARACTERISTICS

Figure 1 shows a schematic of a SET with sidewall depletion gates on a SOI nanowire. The electron channel in the SOI nanowire is formed by the back gate voltage, \( V_{bg} \), and two tunnel junctions are formed by the sidewall depletion gate voltage, \( V_{sg} \). The potential of the electrically formed island is controlled by the control gate voltage, \( V_{cg} \).

![Figure 1](image-url)

Fig. 1. (a) Schematic diagram of the SET with sidewall depletion gates on an SOI nanowire. (b) Cross section of the fabricated SET including the bias symbols.
A schematic of SOI nanowire formation technology, namely, the sidewall masking technology [2], is shown in Fig. 2(a). This method enables a nanoscale patterning by using a combination of conventional lithography and process technology. In addition, Fig. 2(b) shows the process sequence for the formation of sidewall depletion gates on a SOI wire. Details of the fabrication method have been given elsewhere [3].

Figure 3(a) shows the scanning electron microscopy (SEM) image of a uniform 30-nm-wide SOI wire formed by using sidewall masking technology, which effectively suppresses the formation of unintentional potential barriers due geometric irregularities in the nanowire [4]. The final width of the SOI wire $W_{ch}$, its thickness, the thickness of the control gate oxide $T_{ctrl}$, the thickness of the sidewall gate oxide $T_{sg}$, and the width of the sidewall gate $W_{sg}$ were 30, 45, 60, 38, and 30 nm, respectively, while the separation between two sidewall gates $S_{sg}$ was controlled to be in the range of 40~190 nm by varying the width of the Si$_3$N$_4$ groove, $W_{Grv}$. Figures 3(b)~(c) show the SEM images of poly-Si sidewall depletion gates on a SOI wire. The sidewall gate structure has a merit in that it can implement a feature size smaller than the limit of e-beam lithography and depends not on the lithographic limit but on the controllability of chemical-vapor deposition (CVD) and reactive ion etching.

Figure 4 shows the size dependence of the device characteristics. Both the Coulomb oscillation period, $\Delta V_{cg}$, and the maximum Coulomb gap, $\Delta V_{MAX}$, are clearly modulated according to $S_{sg}$. The capacitance between the control gate and the island, $C_{cg}$, corresponds to 1.3, 0.76, and 0.24 aF, respectively, when the values of $\Delta V_{cg}$ are 123, 210, and 675 mV [Fig. 4(a)], and the values of $\Delta V_{MAX}$ are 45, 59, 76, and 104 mV, respectively [Fig. 4(b)], as $S_{sg}$ is varied from 190 nm to 40 nm.

If the field effect of the increasing $V_{cg}$ alleviates the depletion of the electron density by means of the field effect of $V_{sg}$, the effective size of the electrically formed island will increase as $V_{cg}$ increases at fixed $V_{sg}$. Nevertheless, in our devices, $\Delta V_{cg}$ is constant as $V_{cg}$ increases, as shown in Fig. 4(a). This insensitivity of $\Delta V_{cg}$ to $V_{cg}$ is noticeable in that the island size is controlled mainly by $S_{sg}, W_{ch}$, and $V_{sg}$, while the island potential is independently controlled by $V_{cg}$. These characteristics stem from the strong controllability of the tunnel barriers by $V_{sg}$, which is attributed to the three-dimensional structure of...
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Fig. 4. Island size dependence of (a) the Coulomb oscillation characteristics at 77 K and (b) the Coulomb gap characteristics at 15 K.

the sidewall depletion gate wrapping the SOI wire.

Figure 5(a) shows the temperature dependence of the Coulomb oscillation of SETs with $S_{sg}=40$ nm. Clear single-island characteristics are observed at 4.2~188 K [3].

Figure 5(b) shows the drain current, $I_{ds}$, contour of the SET with $S_{sg}=190$ nm. From the $I_{ds}$ contour, the total capacitance of the island ($C_{total}$) varied from 2.86 to 5.08 aF and the voltage gain ($K_V$) from 0.185 to 1.3 [5], as the island size, $S_{sg}$, or the capacitive coupling between the gate and the island was increased.

III. SINGLE-ELECTRON INVERTER

In our SETs, the position of Coulomb oscillation peak could be modulated by $V_{sg}$ [5] due to a sharing of the island charge between the control gate and the sidewall depletion gates. Based on the high-voltage gain and the current switching by the sidewall gates voltage, a single-electron inverter [6] was implemented at 12.5 K. Figure 6 shows the circuit diagram of the directional current switch and its characteristics. By controlling $V_{sg1}$ and $V_{sg2}$, we demonstrated complementary current switching at $V_{dd}=20$ mV, as shown in Fig. 6(b). Figure 7 shows the circuit diagram of a single-electron inverter and its voltage transfer characteristics. The basic operation of a
single-electron inverter with $K_V=1.395$ was successfully demonstrated at $V_{dd}=20$ mV, as shown in Fig. 7(b).

**IV. CONCLUSIONS**

SETs with sidewall depletion gates on SOI nanowires were proposed and were fabricated by using a combination of conventional lithography and process technology. The unique feature of our fabrication method is that all critical dimensions depend not on the limit of lithography but on the controllability of conventional VLSI technology. The island size dependence of the electrical characteristics showed good controllability. Moreover, tunnel barriers and current peak positions were strongly controlled by the sidewall depletion gates. Based on the high-voltage gain and on the control of the Coulomb oscillation peak position by using the sidewall depletion gates, the basic operation of single-electron inverter was demonstrated at 12.5 K. The proposed SET offers feasibility of device design and optimization for SET logic circuits, in that the device parameters are controllable by using conventional VLSI technology.

**ACKNOWLEDGMENTS**

This work has been supported by the BK 21 program and the functional nano-device & circuit application technology development project, Korean Ministry of Commerce, Industry, and Energy. The work at iQUIPS has been supported by the Creative Research Initiative (CRI) program, Korean Ministry of Science and Technology.

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