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Novel Fabrication Method for Forming Damage-Free Sensing Oxide and Threshold Voltage-Tunable Complementary Metal-Oxide Semiconductor in a pH Sensor-CMOS Hybrid System

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A novel fabrication process is proposed to form an ion-sensitive field effect transistor (ISFET) with damage-free gate oxide and a threshold voltage (V_T)-tunable complementary metal-oxide semiconductor (CMOS) readout circuit with oxide-nitride-oxide (ONO) stacked gate dielectric simultaneously. In the ISFET, high-quality sensing oxide can be obtained by adopting a three-step sensing-area etch process that uses silicon nitride as an etch stopper. Furthermore, the V_T value of the CMOS can be tuned appropriately by storing electrons or holes in the silicon nitride of the ONO gate stack through Fowler–Nordheim (FN) tunneling. By using a mixed-mode device and circuit simulations, the ability of minute V_T tuning is verified in the ONO-stacked CMOS. Moreover, the influence of V_T tuning on the sensitivity is investigated in a common source amplifier (CSA) readout circuit consisting of the ISFET and a MOSFET with the ONO gate stack.

Keywords: ONO Gate Stack, ISFET, pH Sensor, CSA, Mixed-Mode Device Simulation.

1. INTRODUCTION

Since the development of nano-fabrication technology, biomedical detection devices capable of detecting small biological entities such as DNA, proteins, and viruses have been widely researched.[1–3] Among these biomedical detection devices, the silicon nanowire (SiNW) FET-based biosensor has been considered as a promising device due to its merits of high sensitivity, a low cost, and label-free/real-time detection which originates from its high surface-to-volume ratio and rapid depletion/accumulation of charges.[4–8] In addition, a CMOS (for the readout circuit) can be co-integrated with SiNW biosensors by a top-down fabrication process.[8,9]

Despite these advantages, several challenges for commercialization as chemical/biomedical sensors remain unsolved. Particularly, unstable operation caused by current drift (a change of the drain current with the measurement time under a fixed bias) has been one of the main obstacles. In previous studies,[8,10,11] it was reported that the drift of the drain current (I_D) is mainly caused by the diffusion of ions into damaged sensing materials. Thus, a fabrication method by which damage-free sensing material can be simply obtained should be introduced.

In this report, we propose a simple fabrication method by which to form damage-free silicon oxide as a sensing material by means of the deposition of a top-oxide/nitride/bottom-oxide (ONO) gate stack and the selective wet etching of the top oxide-nitride material. By adopting the proposed process, damage-free silicon oxide can be obtained in an ISFET region and the V_T value of a CMOS in a readout circuit can simultaneously be adjusted by injecting electrons or holes into the nitride of the ONO gate stack given that the ONO of the CMOS is protected during the wet etching process. Through mixed-mode device and circuit simulations, the effects of V_T tuning on the sensitivity of the sensor system consisting of the ISFET and the CMOS with the ONO gate stack are rigorously investigated.

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2. FABRICATION SCHEME OF THE ONO STACKED SENSOR SYSTEM

A top-down fabrication method is used for the SiNWISFET, as this method enables CMOS-compatible fabrication and accurate nanowire alignment. The schematic diagram of the fabricated SiNWISFET with the co-integrated CMOS is shown in Figure 1(a). Excluding the opening of the sensing area, all process steps of the ISFET are conducted simultaneously with the CMOS, as shown in the process flow of Figure 1(b). Here, it should be noted that the channel of the SiNWISFET is opened (the opening of the sensing area) by photolithography and reactive ion etching (RIE) with CHF_3/CF_4 plasma. The ILD oxide should be etched carefully because the ISFET channel on which the sensing oxide is formed can be damaged by the plasma. Therefore, a timed etch process (repeated ILD oxide etching and monitoring of the ILD oxide thickness) is conducted. In spite of the discreet measurement and etching process, the risk of damage remains due to the inaccuracy of the measurement system in the range of several tens of nanometers. Insufficient etching can result in damaged oxide; in contrast, excessive etching can damage the surface of the channel or even destroy the nanowire.

In order to obtain damage-free sensing oxide, a three-step etching process using silicon nitride as a wet etch stopper is proposed. A schematic diagram of the proposed

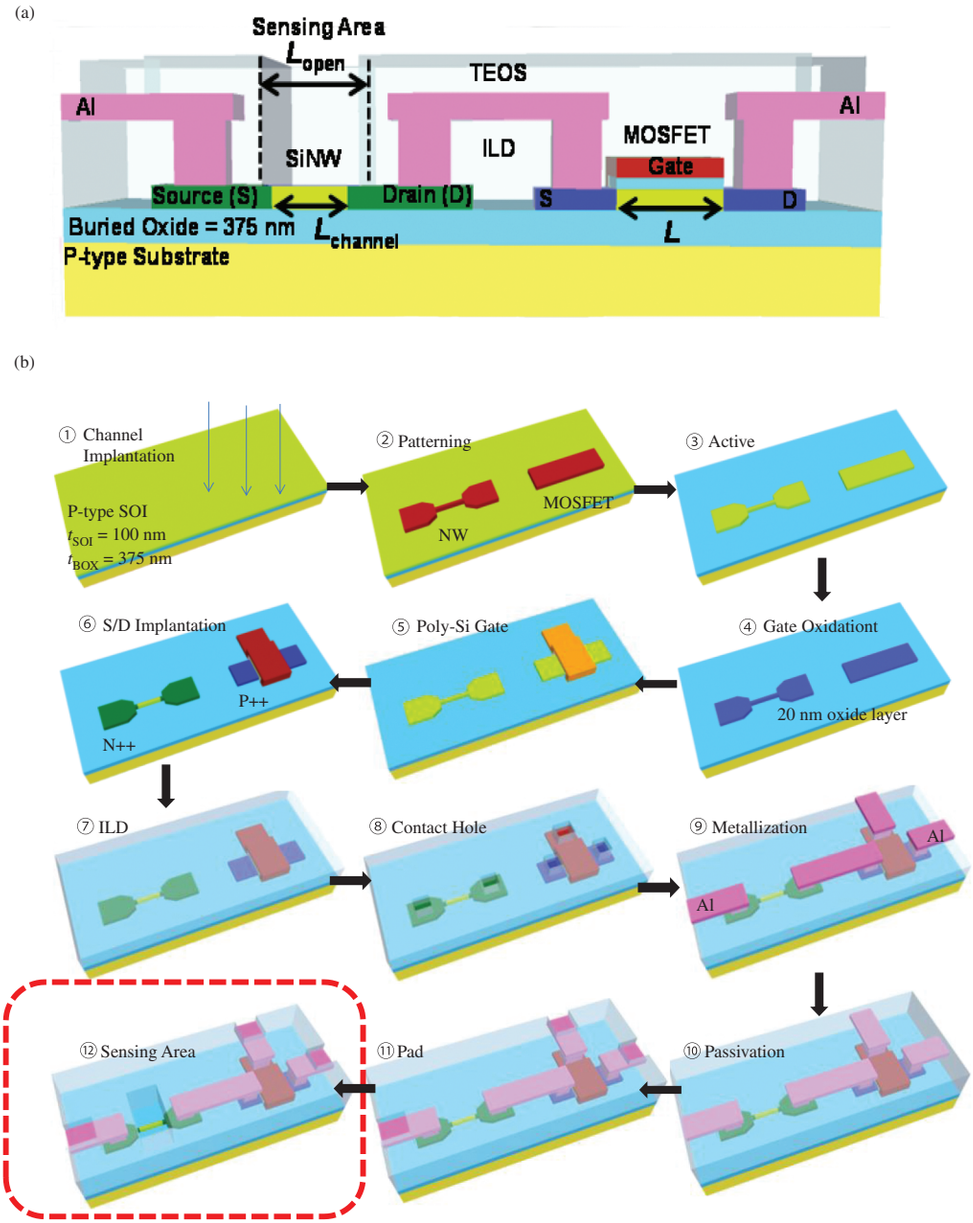

Figure 1. (a) Cross sectional schematic diagram and (b) fabrication process of the co-integrated SiNW ISFET and CMOS for a readout circuit.

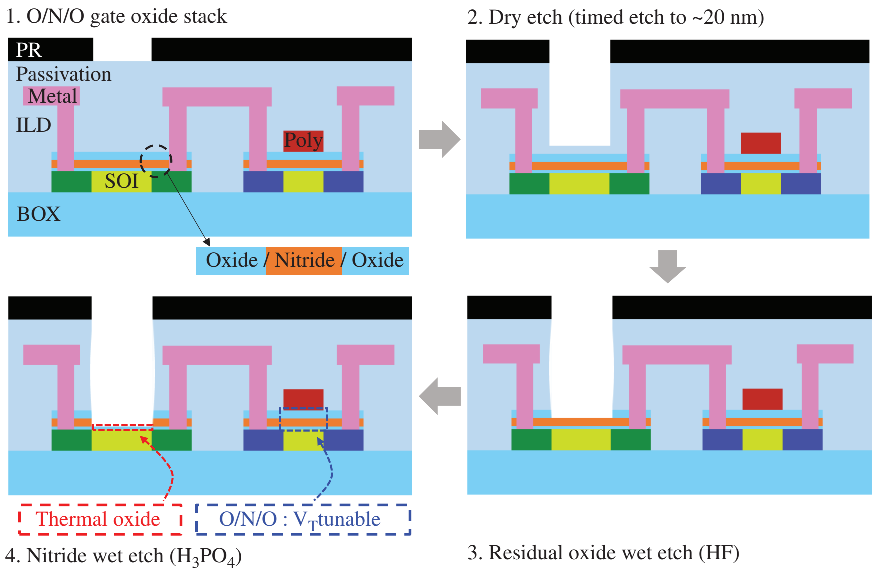

Figure 2. Proposed fabrication method (three-step etching process) using the depositing top oxide-nitride-bottom oxide (ONO) and selectively wet etching top oxide-nitride layer.

etching method is illustrated in Figure 2. The overall fabrication process is identical to that shown in Figure 1(b), except for the formation of the ONO gate stack and the etching of the sensing area. Instead of oxidation for the gate oxide in Figure 1(b), an ONO gate insulator stack is deposited. The bottom oxide is formed by thermal oxidation and the nitride and top oxide are deposited by CVD. In the first step to open the sensing area, timed etching is conducted until approximately 20 nanometers of ILD oxide remains. Secondly, the residual ILD oxide and the top oxide are wet-etched using hydrofluoric acid (HF). In this step, the silicon nitride layer acts as an etch stopper. Figure 3(a) confirms that the silicon nitride layer can serve as an etch stopper because it has excellent selectivity against HF wet etching. The nitride is then wet-etched selectively by phosphoric acid (H_3PO_4). Figure 3(b) indicates that the removal of the oxide is negligible during the wet etching of the silicon nitride, indicating that damage-free thermal bottom oxide with a targeted level of thickness can be obtained. After the three-step etching process, only the damage-free thermal bottom oxide will remain, which clearly shows much more stable sensing properties in terms of the current drift than the damaged oxide (As shown in Figs. 4(a) and (b), showing that the ISFET with damaged sensing oxide experiences serious I_D drift). Moreover, note that the CMOS in the readout circuit can have an ONO gate stack, as the entire region except for the sensing area of the ISFET is blocked throughout the proposed sensing-area etching process. Hence, the V_T value of the CMOS in the readout circuit can be modulated by injecting electrons or holes into the nitride (i.e., the charge trapping layer) of the ONO gate stack.

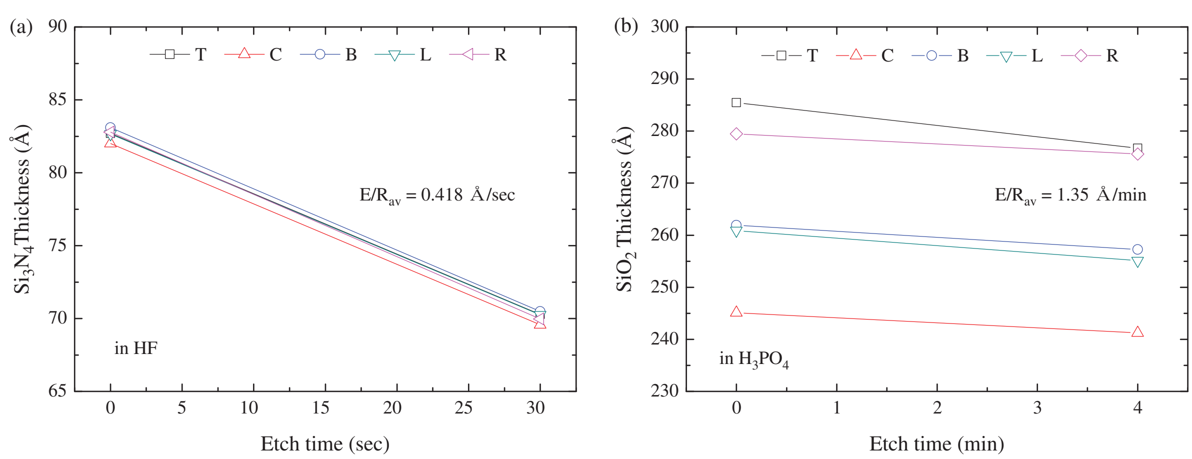

Figure 3. (a) Etch rate of the nitride in HF and (b) that of silicon oxide in H_3PO_4 which verifies high selectivity exceeding 70:1 and 30:1 respectively.

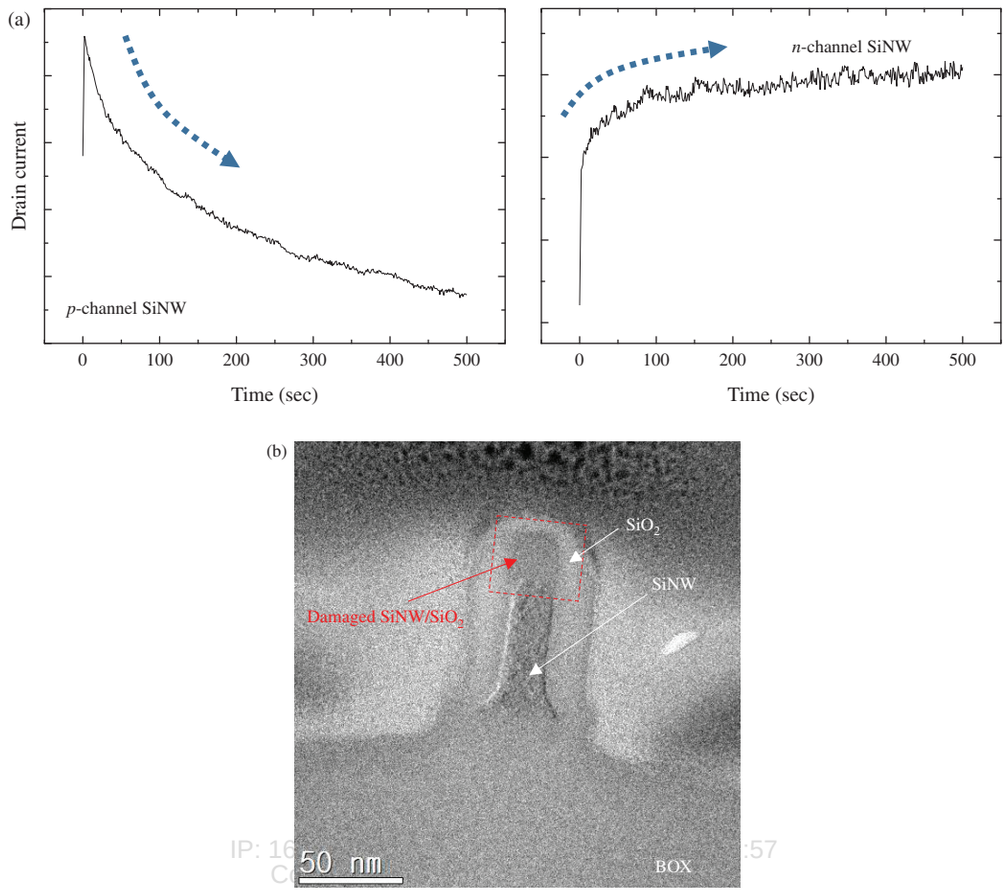

Figure 4. (a) Transient characteristics of n/p-channel SiNW ISFETs with damaged sensing oxide leading to current drift and (b) cross-sectional Transmission Electron Microscopic (TEM) image of damaged SiNW/SiO_2 after the sensing area etching.

3. MIXED-MODE COMMON SOURCE AMPLIFIER (CSA) SIMULATION

Considering the degree of process variability, V_T variation of CMOSs in a readout circuit is unavoidable. At a fixed operation voltage, an inappropriate V_T in the CMOS could directly affect the sensitivity of the ISFET-CMOS sensor system. To investigate the effects of a mismatched V_T on the sensitivity of the sensor system, mixed-mode device and circuit simulations were conducted using a Sentaurus™ TCAD simulator by Synopsys Inc.

The structure and physical parameters of the ISFET (pH sensor) used in this simulation are shown in the insets of Figure 5. First, the change of the transfer curve according to a change in the pH is verified in the ISFET. Figure 5 shows that the transfer curve becomes shifted positively with an increase in the pH. (In the simulations, the Stern layer is considered as a dielectric layer with a thickness of a few angstroms,[12] and the pH change is mimicked by adjusting the number of negative charges on the sensing oxide.) The program characteristics of the MOSFET with the ONO gate stack ($MOSFET_{ONO}$) are then simulated. The device structure of the $MOSFET_{ONO}$ is depicted in the inset of Figure 6. All of the physical parameters of the $MOSFET_{ONO}$ are matched to those of the ISFET, and top oxide (10 nm)/nitride (7 nm)/bottom oxide (5 nm) are applied without a Stern layer. Figure 6 demonstrates that the V_T of the $MOSFET_{ONO}$ can be

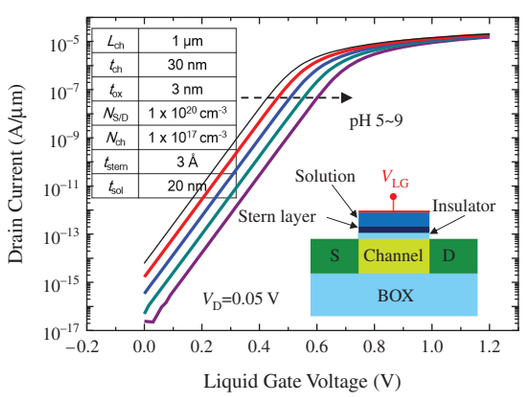

Figure 5. Transfer characteristics of a simulated ISFET (pH sensor) at various pH levels and the structure of the pH sensor (inset, right) with the physical parameters (inset, left).

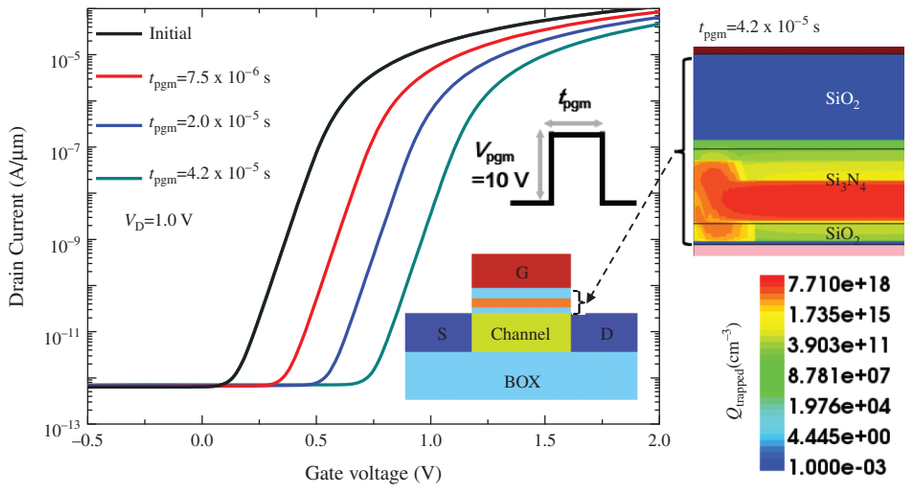

Figure 6. Program operation of the $MOSFET_{ONO}$ device at various program pulse widths (left) and a concentration of trapped electron in the silicon nitride layer at $t_{pgm} = 4.2 \times 10^{-5}$ s (right).

finely modulated by adjusting the program voltage (V_{pgm}) and pulse width (t_{pgm}), which implies that the V_T of MOSFET in a readout circuit can be adjusted to a targeted value of V_T.

To clarify the influence of a mismatched V_T of a MOSFET on the sensitivity of the ISFET-CMOS sensor system, a common source amplifier (CSA) voltage-readout circuit consisting of the ISFET and the $MOSFET_{ONO}$ was used. As shown in Figures 7(a and b), in the CSA, the ISFET and the $MOSFET_{ONO}$ are connected in a series and a fixed liquid gate bias (V_{LG})/gate bias (V_G) condition is applied to each devices.[9] The CSA converts the pH-induced current change of the ISFET to that of the output voltage (V_{OUT}) according to the resistance ratio between the resistance of the ISFET (R_{ISFET}) and the resistance of the $MOSFET_{ONO}$ (R_{MOS}). Figure 8 shows the voltage transfer characteristics (VTCs) of the CSA for different pH levels at a fixed V_{LG} value of 1.5 V. The VTC shifts negatively at a higher pH level because as the pH level increases (i.e., as the concentration of H^+ ions decreases), the I_D of the ISFET decrease and thus R_{ISFET} increases. The sensitivity levels of

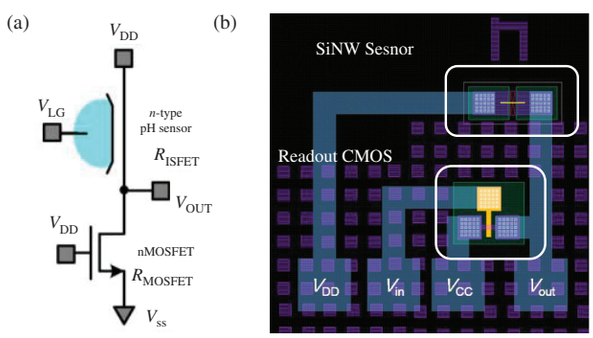

Figure 7. (a) Configuration of the ISFET-CMOS hybrid common source amplifier (CSA) and (b) image of its mask layout image.

the CSAs including the MOSFETs with various V_T values are determined. The change in V_{OUT} caused by a change in the pH ($\Delta V_{OUT}/\Delta pH$) at a fixed V_G is defined as the sensitivity of the CSA, as shown in the inset of Figure 8. (In the inset, a V_G of 1.1 V is used to determine the sensitivity of the CSA.) This level of sensitivity at a fixed V_G is reasonable given that a fixed operation voltage should be used for commercialization regardless of the V_T variation in MOSFETs. Figure 9 shows the extracted sensitivities of the CSAs with a V_G value of 1.1 V as a function of the V_T value of the $MOSFET_{ONO}$. The sensitivity is maximized within the range between $V_T = 0.5$ V and 0.9 V. (Out of this range, the sensitivity decreases sharply). This sensitivity reduction results from the resistance mismatch between R_{ISFET} and R_{MOS} because the sensitivity is aggravated when R_{ISFET} or R_{MOS} is much larger than its respective counterpart.[9]

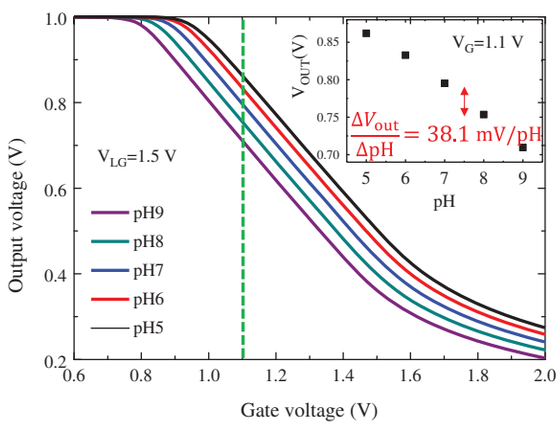

Figure 8. VTCs of CSA consisting of an ISFET and $MOSFET_{ONO}$ for various pH levels and V_{OUT} values as a function of pH level at a fixed V_G (Inset).

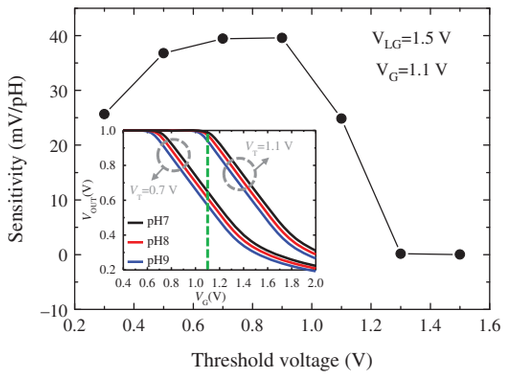

Figure 9. Sensitivities at a fixed V_G as a function of V_T of the $MOSFET_{ONO}$ and VTCs at different V_T values and pH levels (inset).

4. CONCLUSION

In this study, we proposed a simple fabrication method which uses the deposition of an ONO gate stack and the selective etching of a top-oxide nitride layer to obtain damage-free silicon oxide in the ISFET region. In the proposed fabrication scheme, both the V_T—tunability of CMOSs in a readout circuit as well as the stable silicon oxide of the ISFET were realized because the ONO stack in the CMOS region is entirely blocked throughout the sensing-area etching process. The V_T value of the CMOS with the ONO gate stack could be adjusted appropriately by controlling V_{pgm} and t_{pgm}, as demonstrated in a device simulation. The importance of V_T matching in the ISFET-CMOS system was also verified using a mixed-mode device and a circuit (CSA) simulation.

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