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The fabrication of InGaAs MOSFET with Y_2O_3 gate insulator

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Gate stack formation using high-k dielectric materials has been extensively studied on InGaAs channel as an alternative for next node transistors. It is known that a trivalent oxide has good interfacial proeprties with InGaAs. Many studies on Al_2O_3/HfO_2 double-layer gate insulator showed low interface trap density as well as low capacitance equivalent thickness (CET) [1]. On the other hand, Y_2O_3 is also expected for an oxide material with good interfacial properties and larger dielectric constant than that of Al_2O_3. In previous work, we demonstrated bottom gate MOSFET using Y_2O_3 gate insulator with InGaAs channel [2]in which Y_2O_3/InGaAs evidently showed low interface trap density of around 10^{12} $cm^{-2}eV^{-1}$ and high effective mobility (μ_{eff}).

In this study, we investigated top gate InGaAs MOSFET (gate recess type) using the Y_2O_3/InGaAs gate stack. We used n^+InGaAs/InP(cap)/InGaAs(intrinsic)/InP(buffer)/S.I.InP substrate. Figure 1 shows the schematic image of final device structure. First, a mesa was defined by wet etching, followed by gate recess etching. The n^+InGaAs was etched by citric acid and then InP was etched by HCl based solutions. Next, 15 nm-thick Y_2O_3 was depositied by electron beam (E-beam) evaporation. Then, 5 nm-thick Al_2O_3 was subsequently deposited by atomic layer deposition. After gate metal deposition, source and drain metal was deposited by E-beam evaporation. We obtained a good transfer curves with 10^6 on/off ratio and subthreshold swing of about 110 mV/dec as shown in Fig. 2. Also, the high peak mobility of approximately 1,200 $cm^2/V{\cdot}s$ was obatained as shown in Fig. 3.

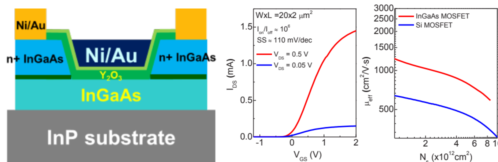

Fig. 1. Schematic image of InGaAs MOSFET (**left**). Fig. 2, 3. The transfer (**center**) and μ_{eff} (**right**) curves of InGaAs MOSFET.

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[2] S. –H. Kim *et al.*, *EDL* **36**, p. 451 (2015)

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