Solid State Electronics xxx (xxxx) xxx-xxx



Contents lists available at ScienceDirect

Solid State Electronics



journal homepage: www.elsevier.com/locate/sse

Universal model of bias-stress-induced instability in inkjet-printed carbon nanotube networks field-effect transistors

Haesun Jung, Sungju Choi, Jun Tae Jang, Jinsu Yoon, Juhee Lee, Yongwoo Lee, Jihyun Rhee, Geumho Ahn, Hye Ri Yu, Dong Myong Kim, Sung-Jin Choi, Dae Hwan Kim*

School of Electrical Engineering, Kookmin University, 861-1 Jeongneung-dong, Seongbuk-gu, Seoul 136-702, South Korea

ARTICLE INFO

Keywords: Carbon nanotube networks FETs Bias stress instability Interface trap Technology computer-aided design (TCAD) simulation

ABSTRACT

We propose a universal model for bias-stress (BS)-induced instability in the inkjet-printed carbon nanotube (CNT) networks used in field-effect transistors (FETs). By combining two experimental methods, i.e., a comparison between air and vacuum BS tests and interface trap extraction, BS instability is explained regardless of either the BS polarity or ambient condition, using a single platform constituted by four key factors: OH^- adsorption/desorption followed by a change in carrier concentration, electron concentration in CNT channel corroborated with H_2O/O_2 molecules in ambient, charge trapping/detrapping, and interface trap generation. Under negative BS (NBS), the negative threshold voltage shift (ΔV_T) is dominated by OH^- desorption, which is followed by hole trapping in the interface and/or gate insulator. Under positive BS (PBS), the positive ΔV_T is dominated by OH^- adsorption, which is followed by electron trapping in the interface and/or gate insulator. This instability is compensated by interface trap extraction; PBS instability is slightly more complicated than NBS instability. Furthermore, our model is verified using device simulation, which gives insights on how much each mechanism contributes to BS instability. Our result is potentially useful for the design of highly stable CNT-based flexible circuits in the Internet of Things wearable healthcare era.

1. Introduction

The inkjet-printed carbon nanotube (CNT) networks used in field effect transistors (FETs) are a fundamental building block for wearable devices used in the Internet-of-Things (IoT) and macroelectronics era [1–4]. CNT networks have various merits such as high mobility, current drivability, low temperature, low-cost fabrication, transparency, and compatibility with flexible substrates. For the commercialization of inkjet-printed CNT network FETs, the reliability and robustness of their electrical characteristics under the condition of real circuit operation need to be guaranteed. Therefore, the understanding of bias-stress (BS) instability is indispensible for the manufacturing of CNT FET-based circuits and systems. However, attempts to develop a universal model of BS instability have rarely been made [5,6].

In this paper, we propose a universal BS-induced instability model that successfully explains the instability mechanisms under negative bias stress (NBS) with gate-to-source voltage (V_{GS}) = -15 V and under positive bias stress (PBS) with V_{GS} = 15 V in CNT FETs with a single framework. By fully taking into account the adsorption/desorption of silanol groups, the generation of interface traps, electron concentration in CNT channel associated with H_2O/O_2 molecules in ambient, and

* Corresponding author.

E-mail address: drlife@kookmin.ac.kr (D.H. Kim).

http://dx.doi.org/10.1016/j.sse.2017.10.022

0038-1101/ © 2017 Published by Elsevier Ltd.

electron/hole trapping, a universal model of BS instability is successfully established and verified using technology computer-aided design (TCAD) simulation.

2. Fabrication process and device structure

Bottom-gate-structure CNT network FETs with a p^+ Si gate and a SiO₂ gate insulator (GI) were used in this study (see Fig. 1(a)). CNT FETs were fabricated on highly p-doped silicon substrates with a thermally grown 50-nm-thick SiO₂ layer. First, the surface was treated with ultraviolet rays to make the surface clean and hydrophilic. Second, the top surface of the SiO₂ layer was functionalized with poly-L-lysine solution (0.1% w/v in water; Sigma Aldrich) to form an amine-terminated surface, which acted as an effective adhesion layer when CNT was deposited. After immersing 90% of the semiconducting CNT solution for several minutes, a CNT network channel was formed. Third, the device was rinsed with isopropanol and deionized (DI) water. To form the source/drain (S/D), silver nanoparticles of the electrodes were printed using an inkjet printer (Unijet UJ200MF) and then annealed (150 °C, 10 min). Poly-4-vinylphenol (PVP) was printed onto the surface to define the channel width; this was followed by one more oxygen plasma-



Fig. 1. (a) Schematic of the inkjet-printed CNT FETs. (b) AFM image of the CNT network using a 90% semiconducting CNT solution. Device width/length is defined as 400/250 μ m.

etching step to remove the unwanted CNT paths. Finally, PVP was removed using warm acetone (70 °C), isopropanol, and flowing nitrogen [7]. Fig. 1(b) shows the atomic force microscopy (AFM) image of the fabricated CNT network.

The current-voltage (I-V) and BS characteristics were measured using the Keithley 4200 system at room temperature under dark conditions. The readout condition was that the gate voltage (V_G) was swept from -10 to +10 V at a drain voltage (V_D) of -0.5 V and a source voltage (V_S) of 0 V in the pulsed I–V mode [8]. The BS test was performed in vacuum and in ambient air, and the results of these two tests were compared each other. The condition of NBS/PBS was V_G = -15/+15 V, V_D = 0 V, and V_S = 0 V. The condition of recovery was V_G = V_D = V_S = 0 V.

3. Results and discussion

The fabricated CNT FET showed a typical transfer characteristic of the p-channel transistor. The BS and recovery time evolutions of the I-V curves are different according to the NBS/PBS and vacuum/air cases, as shown in Fig. 2.

In the NBS case, a negative shift of the threshold voltage (V_T) is observed. The magnitude of the V_T shift (ΔV_T) in vacuum is larger than that in air, whereas a positive ΔV_T is observed during the recovery period, as shown in Fig. 2(a) and (b). The NBS/recovery-induced ΔV_T is shown in Fig. 3(a).

Conversely, in the PBS case, negative or positive ΔV_T is observed in vacuum/air, whereas a negative ΔV_T is observed during the recovery period, as shown in Fig. 2(c) and (d). The PBS/recovery-induced ΔV_T is shown in Fig. 3(b). Furthermore, the PBS test under a relative humidity (RH) 80 % was also performed in order to investigate the ambient effect more in detail (see Fig. 3(b)).

To take the trap-generation-induced ΔV_T into account, the interface

trap density (D_{it}) between CNT and GI was extracted using the multifrequency capacitance-voltage (C-V) spectroscopy [9,10]. No change was observed in D_{it} under NBS; this is denoted by symbols in Fig. 4(a). As shown by the lines in Fig. 4(a), the extracted D_{it} is well-fitted with the superposition of one exponential and one Gaussian function as follows:

$$D_{it} = N_{TD} \times \exp\left(\frac{E_V - E}{kT_{TD}}\right) + N_{GD} \times \exp\left(-\left(\frac{E_V - E + E_{GD}}{kT_{GD}}\right)^2\right)$$
(1)

where N_{TD} and N_{GD} are the densities of the donor-like tail and deep states, respectively; kT_{TD} and kT_{GD} are the characteristic energies of the tail and deep states, respectively; and E_{GD} is the characteristic energy level of the Gaussian deep state. The D_{it} parameters are shown in Fig. 4. Unlike in the NBS case, an increase in the D_{it} tail states is clearly observed in the PBS case, as shown in Fig. 4(b). This increase is one of the origins on negative ΔV_T because the interface trap has the nature of a donor and the CNT FET is a p-channel device.

In the interface between CNT and SiO_2 , a well-known electrochemical reaction in terms of the adsorption/desorption of the silanol group (SiOH⁻) is described as follows [11,12]

$$2Si + 2H_2O + 2e^- \rightarrow 2SiOH^- + H_2 \text{ (adsorption)}$$
(2)

$$2SiOH^{-} \rightarrow 2Si + H_2 + O_2 + 2e^{-} \text{ (desorption)}$$
(3)

The adsorption of silanol groups occurs more actively in air than in vacuum because of the existence of H_2O in air. It would be also maximized under RT = 80 % condition. Therefore, a larger number of silanol groups is supplied to the CNT/SiO₂ interface in air than in vacuum, regardless of the polarity of BS. After SiOH⁻ is adsorbed, the electrons in CNT are annihilated and more abundant holes are accumulated in CNT channel. However, when SiOH⁻ is desorbed, electrons are generated, diffused into CNT, and recombined with holes in the p-channel of the CNT FET. This decreases the hole concentration in CNT.

Fig. 5 illustrates the proposed BS instability model. The SiOH⁻ concentration in the CNT/SiO₂ interface increases in the following order: humid PBS > air PBS > air NBS > vacuum NBS > vacuum PBS, as shown in Fig. 5(a)–(d), respectively. The hole concentration in the CNT FET under NBS is higher in vacuum (Fig. 5(b)) than in air (Fig. 5(a)). Similarly, the electron concentration in CNT under PBS is higher in vacuum (Fig. 5(d)) than in air (Fig. 5(c)).

Under NBS, the negative ΔV_T is dominated by OH⁻ desorption, which is followed by hole trapping in the interface and/or GI. Hole trapping is relatively more suppressed in air than in vacuum because activated OH⁻ desorption reduces the hole concentration more effectively. Thus, a CNT FET under NBS is more unstable in vacuum than in air. During recovery, the holes are detrapped out of the interface and the GI, and OH⁻ is adsorbed because of the electrostatic force resulting from the change in bias. Thus, ΔV_T shifts in the positive direction during recovery. This model is consistent with Fig. 3(a).

Under PBS, the positive ΔV_T is dominated by OH⁻ adsorption, which is followed by electron trapping in the interface and/or GI. Electron trapping is relatively more suppressed in air than in vacuum because more activated OH⁻ adsorption reduces the electron concentration [10,13]. Here, it should be noted that H₂O or O₂ molecules on the CNT surface attracts electrons away from the channel in the bottom gate FET structure [5,6]. Therefore, under PBS, the electron concentration in the CNT channel would increase in the following order: humid < air < vacuum, which is consistent not only with Fig. 5(c) and (d) but [6] as well. The ambient effect on the electron concentration in the CNT channel under PBS is illustrated in Fig. 3(c) as the ΔV_T component associated with electron trapping.

However, unlike in NBS, a D_{it} increase occurs in PBS, as shown in Fig. 4; this increase shifts ΔV_T in a negative direction. In vacuum, OH⁻ adsorption is negligible in comparison to that in air. Although electron trapping is more significant in vacuum than in air, its contribution to achieving a positive ΔV_T is smaller than that of OH⁻ adsorption

H. Jung et al.

10⁻⁴ Initial NBS (air) Initial NBS (vacuum) Stress (3600 sec) Stress (3600 sec) Recovery (3600 sec) Recovery (3600 sec) 10⁻⁵ -I_{DS} [A] 10⁻⁶ . V_⊤ shift V_{τ} shi 10⁻⁷ (b) (a) 10⁻⁸ -5 0 5 -10 -5 0 V_{GS} [V] V_{GS} [V] 10⁻⁴ PBS (air) PBS (vacuum) Initial Initial Stress (3600 sec) Stress (3600sec) Recovery (3600 sec) Recovery (3600sec) 10⁻⁵ 10⁻⁶ -I_{DS} [A] V_{τ} shift V_{τ} shift -10⁻⁷ (d) (c) 10⁻⁸-10 -5 0 5 -10 -5 0 5 V_{GS} [V] V_{GS} [V] 4 (a) Stress Recovery (b) Stress Recovery OH' a on trapping 2 2 OH adsorption hole trapping OH adsorption ΔV_{T} [V] OH desorption electron detrapping ron trappin $\Delta V_{T}\left[V\right]$ hole detrapping OH desorption 0 0 OH adsorption D. increase hole detrapping PBS condition -2 -2 NBS condition – air OH desorption electron detrapping hole trapping → air - vacuum - RH 80 % OH desorption -4 -4 4000 0 2000 6000 0 2000 4000 6000 Time [sec] Time [sec] (c) NBS (air) NBS (vacuum) PBS (RH 80 %) PBS (air) PBS (vacuum) Hole trapping $\Delta V_{\rm T} \left[V \right]$ OH⁻ desorption Electron trapping ■ OH⁻ adsorption D_{it} creation

Solid State Electronics xxx (xxxx) xxx-xxx

Fig. 2. Time-dependences of the transfer characteristics under NBS in (a) air and (b) vacuum, and under PBS in (c) air and (d) vacuum.

Fig. 3. Bias stress and recovery time dependences of $\Delta V_{\rm T}$ (a) under NBS and (b) PBS. (c) The summarized $\Delta V_{\rm T}$ schematic under NBS and PBS in air and vacuum.



10¹⁴ 10¹ PBS NBS $N_{TD} = 2x10^{13} [cm^{-2}eV^{-1}]$ Symb. = Meas. kT_{TD} = 0.02 [eV] Symb. = Meas. Line = Model N_{GD} = 2x10¹² [cm⁻²eV⁻¹] ine = Model $N_{TD} = 5 \times 10^{13} [cm^{-2} eV^{-1}]$ E_{gp} = 0.2 [eV] kT_m = 0.03 [eV] 10¹³ kT_{gp}=0.4 [eV] 10¹³ D_{it} (E) [eV⁻¹ cm⁻²] (E) [eV⁻¹ cm⁻²] N_{gp} = 2x10¹² [cm⁻²eV⁻¹] E_{cp} = 0.2 [eV] kT_{cp}=0.4 [eV] $N_{TD} = 2 \times 10^{13} [cm^{-2} eV^{-1}]$ $N_{TD} = 2x10^{13} [cm^{-2}eV^{-1}]$ 10¹² 10¹² kT_{TD} = 0.02 [eV] kT_{TD} = 0.02 [eV] ت (a) (b) $N_{gD} = 2x10^{12} [cm^{-2}eV^{-1}]$ N_{gp} = 2x10¹² [cm⁻²eV⁻¹] E_{cp} = 0.2 [eV] initial E_{cp} = 0.2 [eV] initial after stress kT_{gp}=0.4 [eV] after stress kT_{gp}=0.4 [eV] **10**¹¹ 10¹¹ 0.0 0.2 0.4 0.0 0.2 0.4 E, + E (E) [eV] E_v + E (E) [eV]

Solid State Electronics xxx (xxxx) xxx-xxx

Fig. 4. The BS time-evolution of D_{it} which is extracted using the multi-frequency C-V method under (a) NBS and (b) PBS. The D_{it} increases only under PBS.

because the electron is a minority carrier in CNT. In the case of vacuum PBS, a small positive ΔV_T is overcompensated by a large negative ΔV_T resulting from the D_{it} increase; consequently, a negative ΔV_T is observed. However, in the case of air/humid PBS, a large positive ΔV_T is undercompensated by the D_{it} -generation-induced negative ΔV_T ; consequently, a positive ΔV_T is observed. During recovery, the electrons are detrapped out of the interface and GI, and OH⁻ are desorbed because of the electrostatic force resulting from the change in bias. Thus, ΔV_T shifts in a negative direction during recovery. This model is also consistent with Fig. 3(b).

Our model combines two experimental methods, i.e., the comparison between air and vacuum and $D_{\rm it}$ extraction, and universally

explains NBS and PBS on a single platform, which is constituted by four key factors: OH^- adsorption/desorption followed by a change in carrier concentration, electron concentration in CNT channel corroborated with H_2O/O_2 molecules in ambient, charge trapping/detrapping, and interface trap generation. Furthermore, our model provides insights on how much each mechanism contributes to BS instability, which is schematically illustrated in Fig. 3(c).

To validate our model, TCAD simulation was performed [14]. The experimentally extracted D_{it} was incorporated into the simulation. Fig. 6 shows that our model-based TCAD reproduces the measured I-V curve very well in all cases involving PBS/NBS and air/vacuum; this suggests that the proposed model is reasonable. The equivalent density



Fig. 5. Energy band diagram under NBS in (a) air and (b) vacuum and under PBS in (c) air and (d) vacuum. These energy band diagrams indicate the different carrier concentrations in CNT. Also, the charge trapping mechanism and OH^- adsorption/desorption under air and vacuum conditions are shown.



Solid State Electronics xxx (xxxx) xxx-xxx

Fig. 6. Comparison of the measured I-V curve with the simulated one. The measured I-V characteristics are reproduced well by using our model-based TCAD simulation under NBS in (a) air and (b) vacuum, and under PBS in (c) air and (d) vacuum conditions.

of charges normalized by the elementary charge $(1.6 \times 10^{-19} \text{ C})$ was estimated to be $4 \times 10^{11} \text{ cm}^{-2}$ (positive charge in vacuum under NBS), $8 \times 10^{11} \text{ cm}^{-2}$ (negative charge in air under PBS), and $4 \times 10^{11} \text{ cm}^{-2}$ (negative charge in vacuum under PBS).

4. Conclusion

We proposed a universal model for BS-induced instability in the inkjet printed CNT network used in FETs. By taking into account the adsorption/desorption of silanol groups, the generation of interface traps, electron/hole trapping, and electron concentration in CNT channel corroborated with H_2O/O_2 molecules in ambient, the proposed model successfully explains NBS- as well as PBS-induced instability on a single framework. Furthermore, the model was verified using TCAD simulation.

As further study, more quantitative analysis, e.g., the decomposition of ΔV_T into respective BS instability mechanism, would be experimentally possible. Useful method is the most likely to be either comparing the dc and ac BS or using the difference between the dc I-V and pulsed I-V measurement corroborated with the hysteresis because distinct instability mechanisms have their own recovery rate when the BS is illuminated. If our result is established as more quantitative model, our model is potentially very useful for the robust design of CNT network FET-based circuits printed on flexible and/or wearable substrate.

Acknowledgement

This work was supported by the National Research Foundation of Korea (NRF) Grant funded by the Korean Government (MSIP) under Grant 2016R1A5A1012966, and in part by the Ministry of Education, Science and Technology (MEST) Grant 2017R1A2B4006982.

References

- Chen H, Cao Y, Zhang J, Zhou C. Large-scale complementary macroelectronics using hybrid integration of carbon nanotubes and IGZO thin-film transistors. Nat Commun 2014;5:4097. http://dx.doi.org/10.1038/ncomms5097.
- [2] Zhao Y, Li Q, Xiao X, Li G, Jin Y, Jiang K, et al. Three-dimensional flexible complementary metal-oxide-semiconductor logic circuits based on two-layer stacks of single-walled carbon nanotube networks. ACS Nano 2016;10:2193–202. http://dx. doi.org/10.1021/acsnano.5b06726.
- [3] Sun D, Timmermans MY, Tian Y, Nasibulin AG, Kauppinen EI, Kishimoto S, et al. Flexible high-performance carbon nanotube integrated circuits. Nat Nanotechnol 2011;6:156–61. http://dx.doi.org/10.1038/nnano.2011.1.
- [4] Yang Y, Ding L, Han J, Zhang Z, Peng L-M. High-performance complementary transistors and medium-scale integrated circuits based on carbon nanotube thin films. ACS Nano 2017:acsnano.7b00861. http://dx.doi.org/10.1021/acsnano. 7b00861.
- [5] Lee SW, Suh D, Young Lee S, Hee Lee Y. Passivation effect on gate-bias stress instability of carbon nanotube thin film transistors. Appl Phys Lett 2014;104:163506. http://dx.doi.org/10.1063/1.4873316.
- [6] Lee SW, Lee SY, Lim SC, Kwon Y, Yoon J-S, Uh K, et al. Positive gate bias stress instability of carbon nanotube thin film transistors. Appl Phys Lett 2012;101:53504. http://dx.doi.org/10.1063/1.4740084.
- [7] Lee J, Yoon J, Choi B, Lee D, Kim DM, Kim DH, et al. Ink-jet printed semiconducting carbon nanotube ambipolar transistors and inverters with chemical doping technique using polyethyleneimine. Appl Phys Lett 2016;109:263103. http://dx.doi. org/10.1063/1.4973360.
- [8] Estrada D, Dutta S, Liao A, Pop E. Reduction of hysteresis for carbon nanotube mobility measurements using pulsed characterization. 2009 Dev Res Conf, IEEE; 2009:bl 27–8. http://dx.doi.org/10.1109/DRC.2009.5354903.
- [9] Yoon J, Choi B, Choi S, Lee J, Lee J, Jeon M, et al. Evaluation of interface trap densities and quantum capacitance in carbon nanotube network thin-film transistors. Nanotechnology 2016;27:295704. http://dx.doi.org/10.1088/0957-4484/27/ 29/295704.

H. Jung et al.

Solid State Electronics xxx (xxxx) xxx-xxx

- [10] Lee S, Park S, Kim S, Jeon Y, Jeon K, Park JH, et al. Extraction of subgap density of states in amorphous ingazno thin-film transistors by using multifrequency capacitancevoltage characteristics. IEEE Electron Dev Lett 2010;31:231–3. http://dx.doi. org/10.1109/LED.2009.2039634.
- [11] Lee JS, Ryu S, Yoo K, Choi IS, Yun WS, Kim J. Origin of gate hysteresis in carbon nanotube field-effect transistors. J Phys Chem C 2007;111:12504–7. http://dx.doi. org/10.1021/jp074692q.
- [12] Kim W, Javey A, Vermesh O, Wang O, Li YM, Dai HJ. Hysteresis caused by water molecules in carbon nanotube field-effect transistors. Nano Lett 2003;3:193–8. http://dx.doi.org/10.1021/nl0259232.
- [13] McGill SA, Rao SG, Manandhar P, Xiong P, Hong S. High-performance, hysteresisfree carbon nanotube field-effect transistors via directed assembly. Appl Phys Lett 2006;89:1–4. http://dx.doi.org/10.1063/1.2364461.
- [14] ATLAS Device Simulation Software User's Manual. Silvaco, Santa Clara, CA; 2016.