Comparative studies on electrical bias temperature instabilities of In–Ga–Zn–O thin film transistors with different device configurations

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We investigated the effect of positive bias temperature stress (PBTS) on the device stabilities of In–Ga–Zn–O thin film transistors with bottom gate and top gate structures. Under the PBTS conditions at the gate voltage of +20 V and the temperature of 60 °C, the turn-on voltage experienced a negative shift of ∼1.5 V for the top gate device, while a larger positive shift of 3.0 V was observed for the bottom gate device. From the variations in transfer characteristics at various temperatures and the discussions on the thermal activation energy, it was suggested that these different behaviors of two devices originated from interface trap densities caused by the plasma damage and the pinning of Fermi energy level for the bottom and top gate devices, respectively. It was very encouraging that the variation of the turn-on voltage could be minimized when the top gate device was fabricated to have a very controlled interface.

1. Introduction

Technical potentials of oxide semiconductor thin-film transistors (TFTs) have been aggressively exploited as promising backplane devices for large-area and high resolution flat-panel displays such as active-matrix organic light-emitting diode (AMOLED) and active-matrix liquid crystal display (AMLCD) [1–4]. For the full-scale commercialization of these panels, device reliabilities of oxide TFT backplanes should be carefully controlled with their high performances including high field-effect mobility and superior uniformity. Amorphous In–Ga–Zn–O (z-IGZO) is one of the most typical material compositions of the oxide semiconductors and have been mainly employed for the fabrication of oxide TFTs [5–7]. So far, device reliability characteristics of z-IGZO TFTs have been investigated under various stress conditions such as negative/positive gate bias stress (NBS/PBS) [8,9], negative gate bias illumination stress (NBIS) [11,12,10], gate bias temperature stress (BTS) [13,14], drain bias stress [15,16], constant current stress [17], and ambient effects [18–21], in which instability mechanisms at various stress situations and suitable strategies for stability improvements have been actively discussed. Typical observations could be classified into two kinds of feasibilities: (1) hole trapping into the gate insulator bulk and/or at the interface between the gate insulator and oxide channel layer, (2) changes of carrier density in the active channel due to the additional state creation. Related discussions and investigations on these issues are now on process and definite conclusions are still controversial. Furthermore, these stability characteristics of oxide TFTs were observed to be very sensitively affected by the process methodologies and device structures [22–24]. Actually, we previously demonstrated an excellent NBS and NBIS characteristic of the z-IGZO TFT by introducing the interface protection layer (PL) between the gate insulator and active channel layers [25]. On the other hand, most devices evaluated in many literatures were fabricated to be bottom gate (BG) structures. Gate insulators of the BG oxide TFTs are easy to be damaged during the sputtering process of IGZO channel layer, even though they can be manufactured by using conventional fab facilities for the a-Si TFTs. Consequently, the top gate (TG) structure can be also a promising alternative to obtain both high performance and excellent stability for the practical applications of oxide TFT backplanes. From these viewpoints, systematic comparative studies on device reliabilities between the BG and TG-structured z-IGZO TFTs would provide some very interesting and important insights to understand the stability issues of oxide TFTs. In this letter, two types of BG and TG z-IGZO TFTs were fabricated and their positive gate bias temperature stabilities (PBTS) were investigated and compared. The degree of instabilities and possible mechanisms were totally different between two types of devices. From the obtained results, it was elucidated that the
appropriate design scheme for the device structure and fabrication process are very important to realize highly reliable x-IGZO TFTs.

2. Experimental details

x-IGZO TFTs with BG and TG structures were fabricated with following procedures. For the first step, a 150 nm thick indium-tin-oxide (ITO) thin film was deposited by radio-frequency (rf) magnetron sputtering and patterned into gate electrodes on the glass substrate of BG device. Al₂O₃ films with thickness of 185 nm were prepared via atomic layer deposition (ALD) method using an Al precursor of trimethylaluminium and water vapor at 150 °C for both TFTs, which correspond to the gate insulator and buffer layers for the BG and TG devices, respectively. The second ITO layers were deposited and patterned into source/drain (S/D) electrodes. 25 nm thick x-IGZO active layer was formed by rf sputtering of a single IGZO (In:Ga:Zn = 1:1:1 atomic ratio) target as active channel layers of both devices. The deposition process was carried out in a mixed atmosphere of Ar and O₂ at room temperature. Al₂O₃ layers with thickness of 9 nm were subsequently formed by ALD method at 200 °C as interface PLs to protect underlying IGZO active layers from chemical damages during the channel patterning process [25]. For this reason, the PL was introduced right before the active patterning process for both TG and BG devices. Then, 176 nm thick Al₂O₃ layers were prepared via atomic layer deposition (ALD) method as interface PLs to protect underlying IGZO active layers from chemical damages during the channel patterning process [25]. For this reason, the PL was introduced right before the active patterning process for both TG and BG devices. The measurements were successively carried out at two drain voltages (V_DS’ s) of 0.1 and 10.1 V at forward and reverse sweeps of V_GS for each device with the gate width (W) and length (L) of 40 and 20 μm, correspondingly. For the BG device, the field effect mobility (μ_FE), threshold voltage (V_TH), turn-on voltage (V_ON), which was defined as the voltage when the I_D was launched from the off-current level, and subthreshold swing (SS) were measured to be 15.0 cm² V⁻¹ s⁻¹, 0.38 V, −0.49 V, and 0.08 V/dec, respectively. Both devices exhibited excellent device behaviors and there were not so marked differences between the devices. Irrespective of these good characteristics, it is important to check the electrical bias and/or temperature instabilities of the devices. In order to confirm the variations in PBS stabilities of the BG and TG devices, a V_GS of +20 V was applied to the gate terminals for 10⁴ s at room temperature and corresponding transfer curves (linear and logarithmic) were measured at V_DS of 10.1 V, as shown in Fig. 2(c) and (d), respectively. As can be seen in figures, it can be very noticeable that the characteristics did not experience any remarkable instability for both devices. After the PBS stress for 10⁴ s, the μ_FE, V_ON, and SS values of BG and TG devices were measured to be 16.3 and 16.2 cm² V⁻¹ s⁻¹, 0.26 and −0.32 V, and 0.10 and 0.10 V/dec, respectively. Although small positive shifts in V_ON were observed, both fabricated devices showed good immunity to the PBS stress at room temperature. On the other hand, for the cases of NBS and NBTS evaluations, there were no marked variations in their transfer characteristics for 10⁴ s and no marked differences between the BG and TG devices. If any electron–hole pair would not be generated by a photon energy with illumination effect, as expected during the NBTS test, undesirable hole trapping caused by the NBTS would not be a critical issue for the well-fabricated IGZO TFTs.

The next evaluations were carried out at 60 °C, in which a V_GS of +20 V was also applied to the gate terminals for 10⁴ s. Fig. 3(a) and (b) shows the variations in I_DS-V_GS transfer characteristics for the fabricated BG and TG devices with the lapse of stressed time, respectively. The increase in temperature under the positive gate bias made big differences in device characteristics from those tested at room temperature as well as between the BG and TG devices. Fig. 3(c) and (d) summarize variations in V_ON, SS, and μ_FE for both devices with the evolution of PBTS test time, respectively. The most marked difference was that the instability in V_ON of the BG device was much larger than that of the TG device. The positive shift in V_ON under PBTS condition without marked degradation of the μ_FE and SS can be generally explained to be due to the electron trapping into the bulk region of gate insulator and/or interface between the gate insulator and active channel layers [8]. It can be considered that a large ΔV_ON of more than 3.0 V for the BG device was caused by some plasma-induced mechanical damages to the gate insulator during the sputtering process for the IGZO formation. Especially, considerable increase in trap sites at the interface may greatly influence on the electron trapping mechanism at an elevated temperature. On the other hand, it is also very important to note that the instability of the TG device appeared to be some negative shift of the V_ON which was completely different from the general trend observed for the PBTS condition. This anomalous behavior confirmed for our TG device suggests that its PBTS instability could be caused by other possibilities than the electron trapping mechanism. We believe that this negative shift in V_ON under PBTS can be observed for only limited devices fabricated with
Fig. 2. $I_{DS}-V_{GS}$ transfer characteristics of the fabricated (a) bottom-gate and (b) top-gate $\alpha$-IGZO TFTs. The gate width and length of each device was 40 and 20 $\mu$m, respectively. The measurements were successively carried out in forward and reverse directions of $V_{DS}$ at two $V_{DS}$'s of 0.1 and 10.1 V. Variations in the $I_{DS}-V_{GS}$ characteristics for the (c) bottom-gate and (d) top-gate TFTs as a function of the stressed time for $10^4$ s at room temperature under the positive bias stress at $V_{GS}$ of 20 V.

Fig. 3. Sets of $I_{DS}-V_{GS}$ transfer curves of the (a) bottom-gate and (b) top-gate $\alpha$-IGZO TFTs with the lapse of stressed time at 60 $^\circ$C under the positive bias stress condition at $V_{CS}$ of 20 V. Variations in (c) $V_{ON}$, (d) $S$ and $\mu_0$ for the bottom- and top-gate TFTs as a function of the stressed time for $10^4$. 
careful prescriptions for the very excellent interface quality. Otherwise, the electron trapping phenomena are dominantly activated and the positive shift of $V_{on}$ is conventionally defined as the PBTS instabilities. From this reason, there have hardly been oxide TFTs reported to experience the negative shift of $V_{on}$ under the PBTS tests among previous literatures. Some feasibility can be expected for these behaviors of the TG device. One possible scenario is that the excess holes injected from the ITO gate electrode into the ITO/Al$_2$O$_3$ interface, which might be a little damaged by the sputtering process of ITO, can cause the negative shift in $V_{on}$ under the PBTS. However, it is supposed that the $V_{on}$ does not shift as much as for the case of charges trapped near the IGZO/Al$_2$O$_3$ interface because the trapped charges are near the gate. Although we cannot completely rule out the hole injection mechanism, an observed $\Delta V_{on}$ of approximately $-1.5$ V for our fabricated TG device can also be explained as shown in Fig. 4(a)–(d).

Before the test of PBTS, the energy band diagram for the metal-insulator-semiconductor (MIS) structure can be described in Fig. 4(a), in which the work function difference between the metal and semiconductor is assumed to be negligible. If the positive bias with a given electric field starts to be applied to the gate terminal, the energy difference between the Fermi level ($E_F$) and the intrinsic level ($E_i$) locally increases at the interface compared with that in the bulk region due to the energy band bending [Fig. 4(b)]. This is the initial stage of PBTS test, which is not so different from the normal gate-bias condition. On the other hand, a continuous application of positive bias stress at a higher temperature may induce additional carriers below the conduction band minimum ($E_C$) and near the tail states. These carriers can be generated from the shallow donors originated by the hydrogen doping effect. The residual hydrogen within the PL of ALD-grown Al$_2$O$_3$ film can be supposed to be incorporated into the IGZO channel at an elevated temperature condition with the lapse of stressed time during the PBTS tests. As results, the amount of free electrons contributing the electronic conduction is expected to increase [26]. However, the free electrons accumulate even in the extended states of the conduction band and band bending is somewhat released, which results from the fact that the $E_F$ is subject to be pinned due to the extrinsically generated bulk defects within the IGZO. Consequently, the energy difference between the $E_F$ and the $E_i$ is reduced and the energy band diagram changes as shown in Fig. 4(c). At this situation, the electron density, which is determined by the difference between the $E_F$ and $E_i$, increases from the bulk to the interface regions. The energy bands modified due to the Fermi level pinning is not recovered even when the PBTS is terminated as shown in Fig. 4(d). Therefore, an accumulation mode of electrons at interface may cause the small negative shift in $V_{on}$ after the PBTS test. It was found from lots of evaluation of devices that this negative shift in $V_{on}$ cannot be observed for the device having severely damaged interfaces with a lot of interface trap sites for electrons.

Fig. 4. Schematics of changes in energy band diagrams for (a) before the PBTS, (b) initial stage during the PBTS, (c) final stage during the PBTS, and (d) after the PBTS.

For the same reason, the Fermi level pinning can also be considered for the BG device. It is expected that the negative shift of $V_{on}$ could be observed even for the BG device if its IGZO/Al$_2$O$_3$ interface quality was guaranteed in an excellent manner. Actually, we have found the BG device experiencing the negative shift of $V_{on}$ after the PBTS test when the gas mixing ratio of Ar/O$_2$ was specifically controlled to 9:1 during the IGZO deposition. However, in this work, the Ar/O$_2$ mixing ratio of 8:2 was chosen as a typical process parameter, because we had a difficulty in obtaining sufficient process window for the device fabrication and reproducibility in device characteristics. In other words, it can be said for the BG device that the effect of Fermi level pinning was screened owing to the dominant action of electron trapping mechanism. It can be found from these results that the plasma damage into the interface, which was caused by the ion bombardment effect of oxygen ions, might have a dominant influence on the device performances of the BG device rather than on the IGZO film quality itself.

Here, we have to note that the differences in amounts of interface trap density between the BG and TG devices are not so large as to be reflected in a marked variation in the SS value, which is an important criterion to evaluate the interface quality. Actually, both devices exhibited similar values of SS even after the PBS evaluations. These results strongly suggest that both devices were basically well fabricated and optimized with a sufficiently good interface properties. However, under more severe evaluation tests such as PBTS, it would be important to note that only a very small difference could make considerable changes in device reliabilities.

In this work, a detailed investigation on the temperature dependent PBTS could not be carried out because the temperature during the PBTS tests was fixed at 60 °C. However, the negative shift in $V_{on}$ was typically confirmed to be accelerated for the IGZO-based oxide TFTs with the increase in the stress temperature during the PBTS test. In order to clearly claim the above-mentioned explanation, the temperature instabilities of BG and TG devices were investigated before [Fig. 5(a) and (b)] and after [Fig. 5(c) and (d)] the PBTS tests, respectively, in which $I_{on}$–$V_{GS}$ transfer curves were measured at the temperatures of 40, 60, 80, and 100 °C. Before the positive bias stress was applied to the device, the $V_{on}$ was observed to be shifted into the negative direction for both devices with the increase of measurement temperature. This negative shift in the $V_{on}$ with increasing the temperature can be explained by the thermal excitation process of the subthreshold drain current, that is, the activated electrons into the conduction band of the IGZO channel. The $I_{on}$ in the subthreshold region for amorphous, polycrystalline Si, and oxide semiconductor TFTs has been described by the Arrhenius model related to the thermal activation process [27–29]. In other words, at elevated temperature, more negative gate voltage is required to completely turn-off the TFTs. In this model, thermally activated electrons from the deep states of trap sites into the conduction band contribute to the current flow of $I_{on}$. The observation that a relatively large shift in the
$V_{on}$ was observed between 80 and 100 °C, as shown in Fig. 5(a) and (b), can be related to the fact that there are some relationship between the generated shallow donors and the threshold value of required energies.

After the PBTS tests, the activated electron carriers are expected to be differently behaved between the BG and TG devices according to their initial situations. For the case of BG device, the $V_{on}$ was also negatively shifted from the point where it had been positively shifted during PBTS due to the electron trapping mechanism, as shown in Fig. 5(c). Parts of activated electron carriers contribute to the negative shift in $V_{on}$ and remains may be simultaneously trapped at shallow interface traps beneath the conduction band, because the temperature of 100 °C is too low for trapped electrons to be completely relieved. Eventually, the $\Delta V_{on}$ of negative shift was smaller than that for the initial BG device. On the other hand, for the case of TG device, the $V_{on}$ finally obtained from the previous PBTS test did not change any more even at the elevated temperature up to 100 °C, as shown in Fig. 5(d). It can be postulated that there was no additional shift in the $V_{on}$ with the temperature increase because the Fermi level was already pinned at certain position near the conduction band, especially for the interface region, during the PBTS tests.

It was sometimes reported that the heat treatment performed at around 100 °C could lead to the thermal recovery of instabilities caused by the positive bias stress [30]. Therefore, it is important to check whether the high-temperature measurements may cause some additional effects after the PBTS tests. For our devices, the annealing process at the temperature of higher than 200 °C was found to be necessary for the PBTS recovery. It was also confirmed that the device characteristics were almost the same when the device was heated to 110 °C and cooled down to room temperature. Consequently, the results obtained in Fig. 5 can be concluded to fairly describe the differences in PBTS instabilities between the BG and TG devices and their temperature dependences without any recovery effect.

As mentioned above, the increase in the $I_D$ at a given $V_{GS}$ would be limited by the thermal excitation of the carriers trapped at energy states located in deep levels within the band gap. If the electrons thermally activated from these deep trap sites into the conduction band are assumed to transport quickly toward the drain electrode owing to the laterally applied electric field, the rate-determining process would be the thermal excitation of the trapped electrons [31]. Thus, the corresponding activation energy ($E_A$) for the conductance of the activated electrons can be calculated as a function of $V_{GS}$ from the Arrhenius plot using the following equation.

$$I_D = I_{DS0} \cdot \exp\left(-\frac{E_A}{kT}\right)$$

where $I_{DS0}$ and $\kappa$ are the constant current factor for a given $V_{GS}$ and the Boltzmann constant, respectively. In this discussion, the $E_A$ is defined as $(E_C - E_F)$ by assuming the Boltzmann statistics [27,28]. From this background, it would be very useful to compare the location of $V_{GS}$ for the maximum $E_A$ and the changing rate of $E_A$ as a function of $V_{GS}$ in understanding the internal natures of device structures. Fig. 6(a) and (b) shows variations in $E_A$ of $I_D$ as a function of $V_{GS}$ for the BG and TG devices, respectively, in which the estimated values of $E_A$ of each device were compared between before and after the PBTS tests. For the BG device, the maximum $E_A$ value of 1.91 eV, which corresponds to the highest energy barrier for thermal activation of trapped electrons, was calculated at a $V_{GS}$

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Fig. 5. Variations in the $I_D$–$V_{GS}$ characteristics of the (a) bottom-gate and (b) top-gate a-IGZO TFTs before the PBTS tests when the measurement temperature was varied to 40, 60, 80, and 100 °C from room temperature. Comparisons of variations in the $I_D$–$V_{GS}$ characteristics of the stressed (c) bottom-gate and (d) top-gate a-IGZO TFTs after the PBTS tests at the same temperature conditions.
of $-0.5 \text{ V}$. After the PBTS, while the maximum $E_A (1.77 \text{ eV})$ did not change so much, the corresponding $V_{GS}$ was positively shifted to 3.1 V, as shown in Fig. 6(a). In contrast, the maximum $E_A$ value of 1.85 eV for the TG device was observed at a $V_{GS}$ of $-1.1 \text{ V}$ and dramatically decreased to 0.91 eV at a $V_{GS}$ of $-2.3 \text{ V}$ after the PBTS, as shown in Fig. 6(b). These results suggest that there was big difference in energy level and density of the trap states within the band structure composed of gate insulator and IGZO active channel between BG and TG devices after the PBTS tests. While only the movement of flatband position occurs due to the dominant electron trapping mechanism during the PBTS for the BG device, the change in the Fermi level affected the decrease in the $E_a$ for the TG device. The actual evaluations on the energy distribution of the total trap densities, including the gate-state density of the active channel and interface trap density, will be performed by careful calculation using Meyer-Neldel rule [29] as future works. It can be concluded from the obtained results that appropriate prescription should be carefully optimized according to the device structures and employed fabrication processes in order to ensure the electrical bias and/or temperature stabilities of IGZO TFTs.

4. Conclusions

In summary, the effect of PBTS on the device behaviors of IGZO TFTs with BG and TG structures was investigated. While there was no marked differences between the BG and TG devices under only PBS, a much larger variation of $V_{th}$ was observed for the BG device compared to the TG device under the PBTS condition at the temperature of 60 °C. Furthermore, it was very impressive that the directions of $V_{th}$ variations were totally different, those are positive and negative, for the BG and TG devices, respectively. An adverse physical damages by ion bombardment to the gate insulator during the IGZO deposition was one of the main origins for the generation of larger interface trap density and the eventual positive shift of $V_{th}$ due to the electron trapping mechanism for the BG device. On the other hand, for the TG device, thanks to the absence of considerable trap sites at the interface, only a small negative shift of $V_{th}$ was observed because of the pinning of Fermi energy level in the semiconductor band gap. The estimations on the thermal activation energy of the subthreshold drain current as a function of $V_{GS}$ well explained these situations. From these comparative studies on the bias and temperature instabilities of IGZO TFTs with BG and TG structures, the strategies to optimize the device reliabilities can be suitably planned for the IGZO TFTs with specified device structures.

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