Highly Scaled, High Endurance, Ω-Gate, Nanowire Ferroelectric FET Memory Transistors

Jong-Ho Bae, Daewoong Kwon, Namho Jeon, *Graduate Student Member, IEEE*, Suraj Cheema, Ava Jiang Tan, Chenming Hu, *Life Fellow, IEEE*, and Sayeef Salahuddin, *Fellow, IEEE*

***Abstract*— In this work, we demonstrate highly scaled, non-volatile memory transistors with ferroelectric Zr-doped HfO_2(HZO) as gate insulator. Ω-gate transistors with gate length ~30 nm and width ~85 nm were fabricated on ~20 nm thick SOI. We demonstrate robust memory operation with ≤100 ns program and erase speed at ±5 V, projected memory retention time up to 10 years at 85 °C, and ~0.5 V memory window after 10^8 endurance cycles. The impact of V_D on erase speed provides insights into the importance of holes on memory operation.**

***Index Terms*— Ferroelectrics, *hafnium zirconium oxide*, *ferroelectric memory*, *FeFET*.**

I. Introduction

THERE is a rekindled interest in ferroelectric field effect transistors (FeFETs) [1] due to the discovery of ferroelectricity in doped HfO_2 [2]–[5] – which makes it CMOS compatible [6]–[10]. FeFET on 22 nm FDSOI process has been demonstrated [11]. In addition, FeFET in 3D NAND structure has also been reported [12], demonstrating applicability in 3D topology. Doped HfO_2 shows robust ferroelectricity in films with ≤10 nm thickness [13]–[16]. This allows operation of these devices at potentially smaller voltages compared to conventional floating body type memory devices. In addition, larger than 10 years retention time can also be achieved in devices based on these thin films, as shown by a number of reports [15]–[22].

For use in advanced technology, scaling of FeFET devices need to be studied properly. In this context, despite an early demonstration [23], many questions remain in terms of the scalability of FeFETs to ultra-small dimension. Especially, it is interesting to know how the memory window, endurance, retention time etc. will behave as the lateral dimension of the gated area scaled to a footprint of just a few individual domains.

In this work, we aim to address these questions by fabricating Zr doped HfO_2 FeFETs of dimensions 30 nm × 85 nm. Our devices show less than 100 ns switching speed, a projected retention time exceeding 10 years at elevated temperature, a memory window of >0.5 V and large endurance of 10^8. Pulsed measurements show clear activation induced switching for both polarities of the voltage, indicating the double-well nature of the ferroelectric even in these scaled dimensions. We also elucidate the influence of holes in device operation, which is often ignored in FeFET device analysis.

II. Device Structure DC Characteristic

Figs. 1(a)-(d) show the schematic cross-section and TEM images of the fabricated FeFET. The gate length (L_G) and width (W) of the smallest FeFET were approximately 30 nm and 85 nm, respectively, and the device has Ω-gate structure (see Figs. 1(b) and (c)). The devices were fabricated on 6-inch FDSOI with 20 nm-thick Si (p-type, $<10^{16}$cm^{-3}). After patterning Si, chemical oxide interfacial layer (IL) was formed by RCA-1, and Zr doped HfO_2 (4:1) layers (FE) were deposited using atomic layer deposition under 250 °C. Typical devices have a 2 nm dielectric layer (DE), 6.5 nm Zr doped HfO_2 ferroelectric layer (FE), and sputtered W as gate (see Fig. 1(d)). After gate patterning, n^+-doped source (S) and drain (D) were formed by self-aligned ion implantation (As, 5×10^{15} cm^{-2}, 5 keV). Post metallization annealing (N_2, 475 °C, 30 s) was performed to obtain FE phase and activate the dopant. Inter-Layer Dielectric (ILD, PECVD SiO_2) deposition, via formation, contact metal (Ti/TiN) deposition and patterning were performed subsequently. Si active layer and gate are patterned by exploiting deep UV stepper and e-beam lithography. Fig. 1(e) shows the DC transfer curves measured from four scaled FeFETs. The memory window is ≥ 0.7 V in the beginning, and the anticlockwise hysteresis due to polarization switching can clearly be observed. We define going from small drain current (I_D) to large I_D as write 1 (W1), and the opposite as write 0 (W0).

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Jong-Ho Bae is with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA 94720 USA, and also with the School of Electrical Engineering, Kookmin University, Seoul 02707, South Korea.

Daewoong Kwon is with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA 94720 USA, and also with the Department of Electrical Engineering, Inha University, Yonghyeon Campus, Incheon 22212, South Korea (e-mail: dw79kwon@inha.ac.kr).

Namho Jeon, Ava Jiang Tan, Chenming Hu, and Sayeef Salahuddin are with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA 94720 USA (e-mail: sayeef@berkeley.edu).

Suraj Cheema is with the Department of Material Science, University of California at Berkeley, Berkeley, CA 94720 USA.

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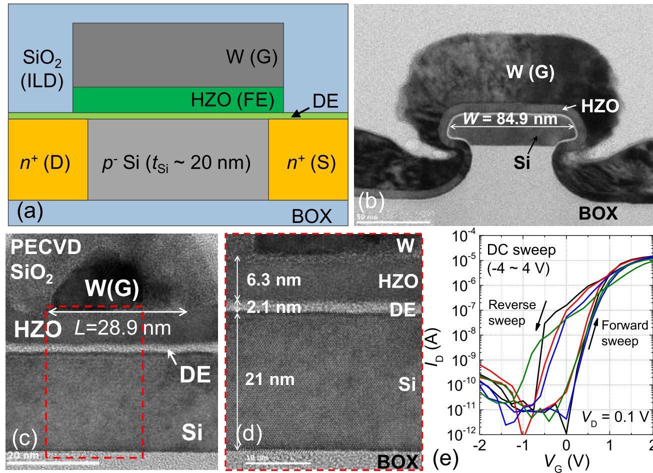

Fig. 1. (a) Schematic and (b), (c) TEM cross-sectional images of a fabricated FeFET. (d) The magnified image of the red square area in (c). (e) Transfer curves measured on four FeFETs ($L_G = 30$ nm, $V_D = 0.1$ V). V_G was swept in the range of -4 to 4 V and the sweep directions are indicated by arrow head on the plot.

III. Results and Discussion

We start with measurement of the switching speed of the fabricated devices. To do this, I_D at $V_G = 0$ V and $V_D = 0.1$ V was measured after applying W1 or W0 pulses ($V_{G,W1}$, $V_{G,W0}$) with different pulse amplitudes and pulse widths (t_p). $|V_{G,W1}|$ and $|V_{G,W0}|$ was changed from 3.75 to 5 V, and t_p was changed from 100 ns to 1 ms (Fig. 2(a)). Figs. 2(b) and (c) show I_D after W1 and W0 as a function of t_p at various $V_{G,W1}$ and $V_{G,W0}$, respectively. W1 to 100 nA can be accomplished in < 100 ns at $V_G = 4.5$ V and < 1 us at $V_G = 4$ V. W0 to 10 pA is slower and requires 700 ns at $V_G = -5$ V and 70 us at $V_G = -4$ V. The slower 1→0 transition can be explained by the fact that, for 20 nm thick SOI, there is hardly any holes in the body to form an accumulation layer, therefore, the body potential is closely coupled to the applied V_G. In other words, the applied V_G is partially consumed by the SOI body and less is available as the voltage across the HZO. One way to remedy this situation is to exploit the GIDL current to inject holes in the floating body [24]. Indeed, as shown in Fig. 2(d), W0 becomes systematically faster with increased V_D for W0 ($V_{D,W0}$) and is accelerated by 20x or reduce the required $V_{G,W0}$ by 0.5 V when 1 V $V_{D,W0}$ is applied. This illustrates the importance of holes in the FDSOI based devices. While increased $V_{D,W0}$ is a way to bring in holes, the speed of operation is restricted by the GIDL hole current that can be generated at the drain side. Bulk devices may enjoy an advantage in this respect. Figs. 3(a) and (b) show log t_p versus $V_{G,W0}$ and $V_{G,W1}$ diagrams for switching between 100 nA and 10 pA. Each specific symbol corresponds to a single device. Data for multiple devices are shown and found to follow a very similar trend line. The nearly straight-line behavior is a signature of an activation barrier. The fact that it is found for both switching voltage polarities indicates that the system has a double well energy barrier – reminiscent of a ferroelectric free energy. This data thus indicates that the classical ferroelectric behavior is preserved down to very small lateral dimension. We note here, although not done in this report, a similar measurement as a function of temperature should be able to pin-point the energy barrier, much the same way it is done for ferromagnets [25]. From Figs. 3(a) and (b), we find that both W1 and W0 operations of 100 ns are possible with at an applied V_G pulse of ±5 V with the help of 1 V V_D during W0. Data retention properties were measured up to 10^4 s at 85 °C (Fig. 4(a)). After applying single W1 or W0 pulse, I_D was measured repeatedly over time. One of the devices was measured for 10^5 s retention time, there is no sign of degradation on memory window. V_T tends to

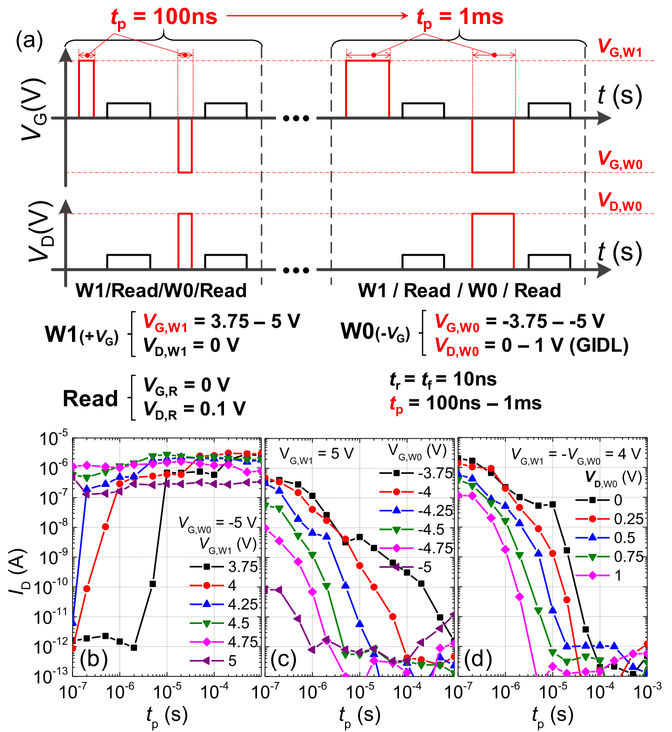

Fig. 2. (a) Pulse scheme for measuring t_p–I_D plots. t_p–I_D plots of a FeFET ($L_G = 30$ nm) at various (b) $V_{G,W1}$ (3.75 ∼ 5 V), (c) $V_{G,W0}$ (−3.75 ∼ −5 V) and (d) $V_{D,W0}$ (0 ∼ 1 V). In (b) and (a), $V_{D,W1} = V_{D,W0} = 0$ V, and $V_{G,W0}$ and $V_{G,W1}$ were fixed at −5 and 5 V, respectively. In (c), $V_{G,W1}$ and $V_{G,W0}$ were fixed at 4 and −4 V, respectively. I_D was measured at $V_G = 0$ V and $V_D = 0.1$ V.

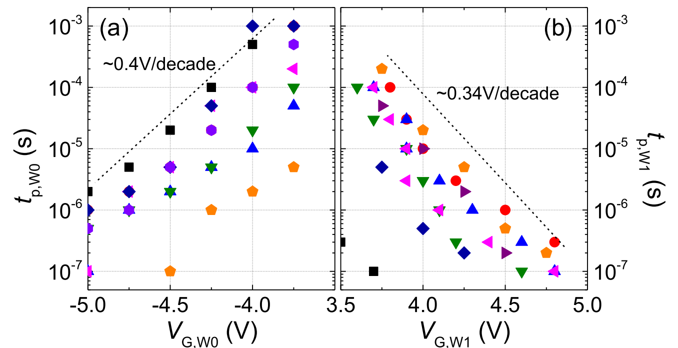

Fig. 3. (a) $V_{G,W0}$–$t_{p,W0}$ and (b) $V_{G,W1}$–$t_{p,W1}$ plots measured from several FeFETs. $t_{p,W0}$ and $t_{p,W1}$ were defined as the t_p value where the I_D becomes smaller and larger than 10 pA and 100 nA, respectively ($I_{D,W1}/I_{D,W0} = 10^4$). Data was measured with the same operation scheme for Fig. 2(a) and (b). The L_G of the devices is between 29 and 40nm.

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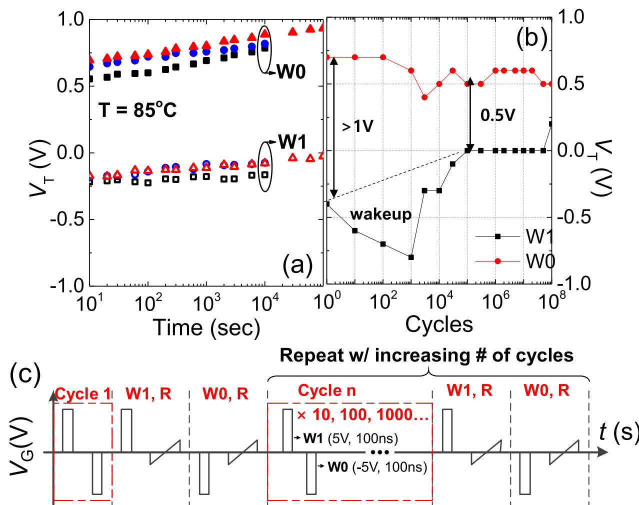

Fig. 4. (a) Data retention measured from three FeFETs at 85 °C (L_G = 29-40 nm). Data retention of a FeFET was measured up to 10^5s (red symbol). (b) V_T after W1 and W0 vs. the number of P-E cycles. V_T was extracted from I_D = 10 pA. L_G = 30 nm. (c) Pulse scheme for endurance test. For each cycles, ±5 V/100 ns pulses were applied with 1 μs intervals.

increase after W1 and W0, which seems to be related to e^- trapping in deep traps due to the elevated temperature. Fig. 4(b) shows measured V_T through 10^8 cycles of endurance cycling. As shown in Fig. 4(c), for each cycle, a bi-directional V_G pulse of ±5 V of 100 ns duration was applied. Fig. 4(c) also shows the ramp used to read out the memory V_T. From Fig. 4(b), we find that positive V_T (W0) is hardly affected while the negative V_T (W1) shows significant degradation with cycling. This suggests generation of acceptor-like traps with cycling perhaps in the interfacial layer. These traps negatively charged after each W1 ($+V_G$) pulse as the channel electrons tunnel into the traps. As a result, there is a positive shift of the V_T(W1). On the other hand, when a W0 ($-V_G$) pulse is applied, the traps are emptied and hence there is not any substantial shift for the V_T(W0).

IV. Conclusion

To summarize, highly scaled (30 nm × 85 nm) FeFET memory devices were demonstrated with fast speed, high endurance and long retention. This shows promise for very high-density embedded memory. Notably, we found that, by applying a 1 V V_D, GIDL generated holes allow rapid formation of an accumulation layer in the SOI FeFET channel and accelerate the Write 0 operation by 20x. Without the applied V_D, about 0.5 V more V_G is needed to generate the same GIDL current and achieve the same W0 speed. Lack of holes also limits the amount of polarization that can be switched, in turn, limiting the memory window. Use of bulk substrates could mitigate both these effects. Additionally, increased memory window could allow much thinner FE, decreasing trapping and thus further increasing endurance. Also note that $V_T \leq 0$ for the erased state is not desirable as this could lead to bit-line shorting. Gate workfunction engineering will be needed to push the V_Ts up and mitigate this problem.

References

[1] S.-Y. Wu, "Metal-ferroelectric-semiconductor transistor," *IEEE Trans. Electron Devices*, vol. 21, no. 8, pp. 499–504, Aug. 1974, doi: 10.1109/T-ED.1974.17955.

[2] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Appl. Phys. Lett.*, vol. 99, no. 10, Sep. 2011, Art. no. 102903, doi: 10.1063/1.3634052.

[3] J. Müller, T. S. Böscke, D. Bräuhaus, U. Schröder, U. Böttger, J. Sundqvist, P. Kücher, T. Mikolajick, and L. Frey, "Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 99, no. 11, Sep. 2011, Art. no. 112901, doi: 10.1063/1.3636417.

[4] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, "Incipient ferroelectricity in al-doped HfO_2 thin films," *Adv. Funct. Mater.*, vol. 22, no. 11, pp. 2412–2417, Jun. 2012.

[5] G. Karbasian, R. dos Reis, A. K. Yadav, A. J. Tan, C. Hu, and S. Salahuddin, "Stabilization of ferroelectric phase in tungsten capped $Hf_{0.8}Zr_{0.2}O_2$," *Appl. Phys. Lett.*, vol. 111, no. 2, Jul. 2017, Art. no. 022907, doi: 10.1063/1.4993739.

[6] J. H. Choi, Y. Mao, and J. P. Chang, "Development of hafnium based high-K materials—A review," *Mater. Sci. Eng., R, Rep.*, vol. 72, no. 6, pp. 97–136, Jul. 2011, doi: 10.1016/j.mser.2010.12.001.

[7] T. S. Boscke, J. Müller, D. Brauhaus, U. Schroder, and U. Bottger, "Ferroelectricity in hafnium oxide: CMOS compatible ferroelectric field effect transistors," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2011, pp. 24.5.1–24.5.4, doi: 10.1109/IEDM.2011.6131606.

[8] J. Müller, E. Yurchuk, T. Schlosser, J. Paul, R. Hoffmann, S. Müller, D. Martin, S. Slesazeck, P. Polakowski, J. Sundqvist, M. Czernohorsky, K. Seidel, P. Kucher, R. Boschke, M. Trentzsch, K. Gebauer, U. Schroder, and T. Mikolajick, "Ferroelectricity in HfO_2 enables nonvolatile data storage in 28 nm HKMG," in *Proc. Symp. VLSI Technol. (VLSIT)*, Honolulu, HI, USA, Jun. 2012, pp. 25–26, doi: 10.1109/VLSIT.2012.6242443.

[9] M. Trentzsch, S. Flachowsky, R. Richter, J. Paul, B. Reimer, D. Utess, S. Jansen, H. Mulaosmanovic, S. Muller, S. Slesazeck, J. Ocker, M. Noack, J. Muller, P. Polakowski, J. Schreiter, S. Beyer, T. Mikolajick, and B. Rice, "A 28nm HKMG super low power embedded NVM technology based on ferroelectric FETs," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2016, pp. 11.5.1–11.5.4, doi: 10.1109/IEDM.2016.7838397.

[10] K. Chatterjee, S. Kim, G. Karbasian, A. J. Tan, A. K. Yadav, A. I. Khan, C. Hu, and S. Salahuddin, "Self-aligned, gate last, FDSOI, ferroelectric gate memory device with 5.5-nm $Hf_{0.8}Zr_{0.2}O_2$, high endurance and breakdown recovery," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1379–1382, Oct. 2017, doi: 10.1109/LED.2017.2748992.

[11] S. Dunkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Müller, T. Melde, H. Mulaosmanovic, S. Slesazeck, S. Müller, J. Ocker, M. Noack, D.-A. Lohr, P. Polakowski, J. Muller, T. Mikolajick, J. Hontschel, B. Rice, J. Pellerin, and S. Beyer, "A FeFET based super-low-power ultra-fast embedded NVM technology for 22nm FDSOI and beyond," in *IEDM Tech. Dig.*, Dec. 2017, San Francisco, CA, USA, Dec. 2017, pp. 19.7.1–19.7.4, doi: 10.1109/IEDM.2017.8268425.

[12] K. Florent, S. Lavizzari, L. Di Piazza, M. Popovici, E. Vecchio, G. Potoms, G. Groeseneken, and J. Van IHoudt, "First demonstration of vertically stacked ferroelectric al doped HfO_2 devices for NAND applications," in *Proc. Symp. VLSI Technol.*, Kyoto, Japan, Jun. 2017, pp. T158–T159, doi: 10.23919/VLSIT.2017.7998162.

[13] S. Mueller, J. Muller, U. Schroeder, and T. Mikolajick, "Reliability characteristics of ferroelectric Si:HfO_2 thin films for memory applications," *IEEE Trans. Device Mater. Rel.*, vol. 13, no. 1, pp. 93–97, Mar. 2013, doi: 10.1109/TDMR.2012.2216269.

[14] J. Muller, T. S. Boscke, S. Muller, E. Yurchuk, P. Polakowski, J. Paul, D. Martin, T. Schenk, K. Khullar, A. Kersch, W. Weinreich, S. Riedel, K. Seidel, A. Kumar, T. M. Arruda, S. V. Kalinin, T. Schlosser, R. Boschke, R. van Bentum, U. Schroder, and T. Mikolajick, "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2013, pp. 10.8.1–10.8.4, doi: 10.1109/IEDM.2013.6724605.

[15] K. Chatterjee, S. Kim, G. Karbasian, D. Kwon, A. J. Tan, A. K. Yadav, C. R. Serrao, C. Hu, and S. Salahuddin, "Challenges to partial switching of $Hf_{0.8}Zr_{0.2}O_2$ gated ferroelectric FET for multilevel/analog or low-voltage memory operation," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1423–1426, Sep. 2019, doi: 10.1109/LED.2019.2931430.

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[16] A. J. Tan, K. Chatterjee, J. Zhou, D. Kwon, Y.-H. Liao, S. Cheema, C. Hu, and S. Salahuddin, "Experimental demonstration of a ferroelectric HfO2-based content addressable memory cell," *IEEE Electron Device Lett.*, vol. 41, no. 2, pp. 240–243, Feb. 2020, doi: 10.1109/LED.2019.2963300.

[17] J. Müller, T. S. Boscke, U. Schroder, R. Hoffmann, T. Mikolajick, and L. Frey, "Nanosecond polarization switching and long retention in a novel MFIS-FET based on ferroelectric HfO_2," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 185–187, Feb. 2012, doi: 10.1109/LED.2011.2177435.

[18] E. Yurchuk, J. Muller, J. Paul, T. Schlosser, D. Martin, R. Hoffmann, S. Mueller, S. Slesazeck, U. Schroeder, R. Boschke, R. van Bentum, and T. Mikolajick, "Impact of scaling on the performance of HfO_2-based ferroelectric field effect transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 3699–3706, Nov. 2014, doi: 10.1109/TED.2014.2354833.

[19] K. Ni, P. Sharma, J. Zhang, M. Jerry, J. A. Smith, K. Tapily, R. Clark, S. Mahapatra, and S. Datta, "Critical role of interlayer in $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric FET nonvolatile memory performance," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018, doi: 10.1109/TED.2018.2829122.

[20] T. Ali, P. Polakowski, S. Riedel, T. Büttner, T. Kämpfe, M. Rudolph, B. Pätzold, K. Seidel, D. Löhr, R. Hoffmann, M. Czernohorsky, K. Kühnel, P. Steinke, J. Calvo, K. Zimmermann, and J. Müller, "High endurance ferroelectric hafnium oxide-based FeFET memory without retention penalty," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3769–3774, Sep. 2018, doi: 10.1109/TED.2018.2856818.

[21] N. Gong and T.-P. Ma, "Why is FE–HfO_2 more suitable than PZT or SBT for scaled nonvolatile 1-T memory cell? A retention perspective," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1123–1126, Sep. 2016, doi: 10.1109/LED.2016.2593627.

[22] K.-T. Chen, H.-Y. Chen, C.-Y. Liao, G.-Y. Siang, C. Lo, M.-H. Liao, K.-S. Li, S. T. Chang, and M. H. Lee, "Non-volatile ferroelectric FETs using 5-nm $Hf_{0.5}Zr_{0.5}O_2$ with high data retention and read endurance for 1T memory applications," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 399–402, Mar. 2019, doi: 10.1109/LED.2019.2896231.

[23] H. Mulaosmanovic, J. Ocker, S. Müller, U. Schroeder, J. Müller, P. Polakowski, S. Flachowsky, R. van Bentum, T. Mikolajick, and S. Slesazeck, "Switching kinetics in nanoscale hafnium oxide based ferroelectric field-effect transistors," *ACS Appl. Mater. Interfaces*, vol. 9, no. 4, pp. 3792–3798, Jan. 2017, doi: 10.1021/acsami.6b13866.

[24] C. Caillat, K. Beaman, A. Bicksler, E. Camozzi, T. Ghilardi, G. Huang, H. Liu, Y. Liu, D. Mao, S. Mujumdar, N. Righetti, M. Ulrich, C. Venkatasubramanian, X. Yang, A. Goda, S. Gowda, H. Mebrahtu, H. Sanda, Y. Yuwen, and R. Koval, "3DNAND GIDL-assisted body biasing for erase enabling CMOS under array (CUA) architecture," in *Proc. IEEE Int. Memory Workshop (IMW)*, Monterey, CA, USA, May 2017, pp. 1–4, doi: 10.1109/IMW.2017.7939067.

[25] N. Roschewsky, C.-H. Lambert, and S. Salahuddin, "Spin-orbit torque switching of ultralarge-thickness ferrimagnetic GdFeCo," *Phys. Rev. B, Condens. Matter*, vol. 96, no. 6, Aug. 2017, Art. no. 064406, doi: 10.1103/PhysRevB.96.064406.

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