Solid State Electronics 165 (2020) 107741

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Implementation of homeostasis functionality in neuron circuit using double-gate device for spiking neural network

Sung Yun Woo[a], Kyu-Bong Choi[a], Jangsaeng Kim[a], Won-Mook Kang[a], Chul-Heung Kim[a], Young-Tak Seo[a], Jong-Ho Bae[b], Byung-Gook Park[a], Jong-Ho Lee[a,*]

[a] Department of Electrical and Computer Engineering and the Inter-University Semiconductor Research Center (ISRC), Seoul National University, Seoul 151-742, South Korea

[b] Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA 94720, USA

ARTICLE INFO

Keywords:
Double-gate MOSFET
Neuron circuit
Homeostasis functionality
Pattern recognition
Spiking neural networks (SNNs)

ABSTRACT

The homeostatic neuron circuit using a double-gate MOSFET is proposed to imitate a homeostasis functionality of a biological neuron in spiking neural networks (SNN) based on a spike-timing dependent plasticity (STDP). The threshold voltage (V_{th}) of the double-gate MOSFET is controlled by independent two-gate biases (V_{G1} and V_{G2}). By using V_{th} change of the double-gate MOSFET in the neuron circuits, the fire rate of the output neuron is controlled. The homeostasis functionality is implemented by the operation of multi-neuron system based on the proposed neuron circuit. Through the SNN based on STDP using MNIST datasets, it is demonstrated that the recognition rate (~91%) of the SNN with the proposed homeostasis functionality is higher than that (~79%) of the SNN without the proposed homeostasis functionality. Also, the results of the recognition rate with the variations ($\sigma/\mu < 0.5$) of the synaptic devices and the initial V_{th} of neuron circuits show a low degradation ($1 \sim 3\%$) in the recognition rate. Thus, it is demonstrated that the homeostasis functionality of the proposed neuron circuit has the immunity to variations ($\sigma/\mu < 0.5$) of the synaptic devices and the neuron circuits in the SNN based on STDP.

1. Introduction

Recently, hardware-based neural networks (HNNs) have been studied to reduce power consumption in processing complex computations and enormous data [1]. Especially, hardware-based spike neural networks (H-SNN) based on spike-timing dependent plasticity (STDP) rule that enable on-chip training and asynchronous systems have been researched [2–8]. To implement the hardware-based SNNs, various neuron circuits and synaptic devices such as phase change random access memory (PCRAM), resistive random access memory (RRAM) and FET-based device have been investigated [9–11]. However, there are variations in the hardware-based neural network composed of the synaptic devices array and multi-neurons. These variations cause the degradation of pattern recognition in the SNN based on the STDP rule. To compensate these variations in the hardware-based SNNs, a homeostasis functionality of the biological neuron has been proposed [12]. The homeostasis functionality in the SNNs is to control the fire rate of the neuron circuit, and various hardware-systems have been researched to mimic the homeostasis functionality [13–17]. Most studies control the fire rate of neurons by modulating the amount of current transmitted from synaptic devices. A neuron circuit using a double-gate MOSFET is relatively more stable because it compares the potential of a membrane capacitor with the voltage applied to only one independent gate.

In this paper, we propose the neuron circuit using the double-gate MOSFET that controls the fire rate of the neuron circuit. The threshold voltage change (V_{th}) of the double-gate MOSFET is investigated as a parameter of the gate bias (V_{G2}). Also, a homeostasis circuit for controlling V_{G2} of the double-gate MOSFET is proposed. The operation of the homeostasis functionality is demonstrated through the circuit-simulation of the proposed multi-neurons system. Finally, we demonstrate the immunity to variations of the synaptic devices and neuron circuits through the simulation of a 2-layer SNN based on the proposed neuron circuit.

2. Device structure and fabrication

Fig. 1 (a) and (b) show a 3-D schematic view and a cross-sectional scanned electron microscopy (SEM) image of the double-gate device fabricated on a bulk Si wafer, respectively. The structure of double-

* Corresponding author.
E-mail address: jhl@snu.ac.kr (J.-H. Lee).

https://doi.org/10.1016/j.sse.2019.107741

Available online 13 December 2019

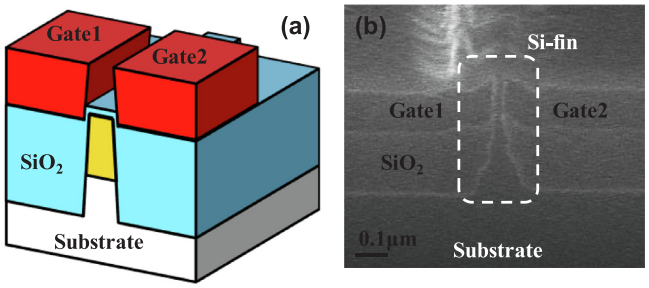


Fig. 1. (a) 3-D schematic view of the synaptic device. (b) Cross-sectional SEM image of the floating fin-body MOSFET.

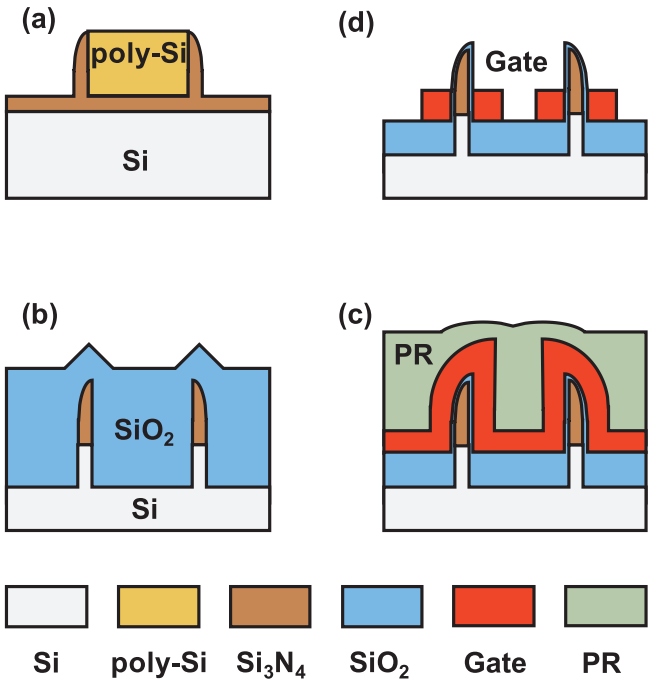


Fig. 2. Schematic views of key fabrication process steps of the floating fin-body MOSFET on p-type (1 0 0) bulk Si wafer.

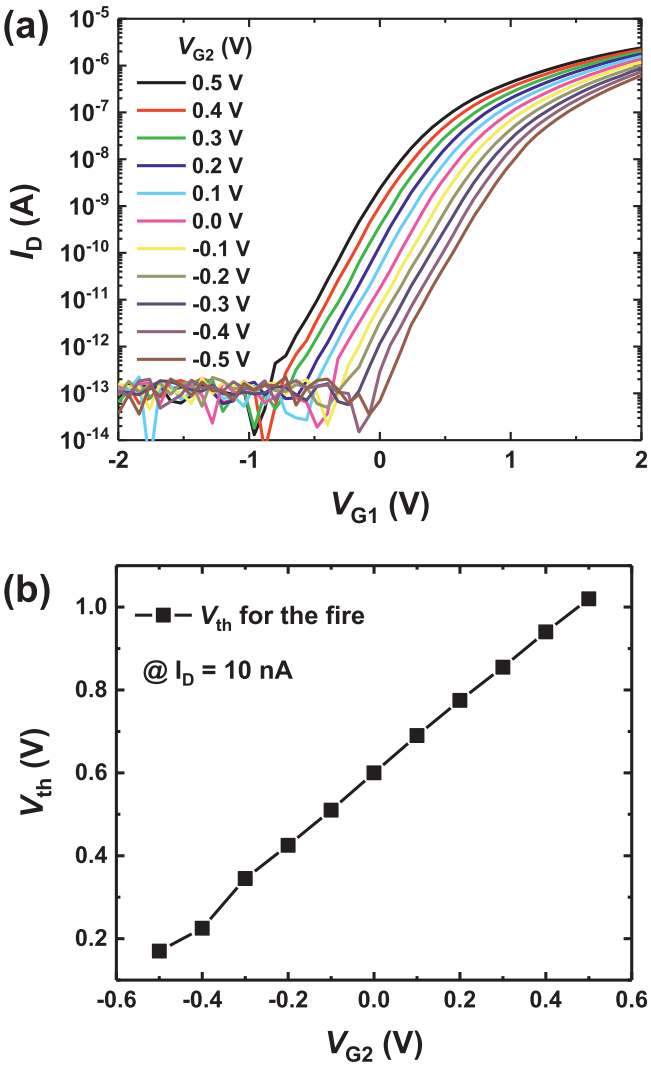


Fig. 3. (a) Measured I_D-V_{G1} curves of the double-gate MOSFET as a parameter of V_{G2}. (b) V_{th} change of the double-gate MOSFET as a parameter of V_{G2}.

gates is proposed to control a threshold voltage (V_{th}) of the MOSFET. The bulk fin-body width (W) is 35 nm. Here, the doping concentrations of fin-body, source and drain region are 1×10^{18} cm^{-3}, 2×10^{20} cm^{-3}, and 2×10^{20} cm^{-3}, respectively. The thickness of gate dielectric stack (SiO_2) is 9 nm and the gate material is the n^+-doped poly-Si. This structure was fabricated through the following process steps as shown in Fig. 2. A layer of thin Si_3N_4 is deposited on (1 0 0) Si wafer. Then, a poly-Si layer is deposited and patterned for Si_3N_4 spacer formation as shown in Fig. 2 (a). The poly-Si is stripped, and Si fins are formed by dry etching using the Si_3N_4 spacer as a hard-mask. And then, a thick SiO_2 layer is deposited by high-density plasma chemical vapor deposition (HDPCVD) process for the isolation as shown in Fig. 2 (b). After etching a SiO_2 partly, ion implantations are performed for field and channel dopings. A SiO_2 (9 nm) layer and n^+-doped poly-Si layer are deposited as the gate insulator and the gate material, respectively. By coating the wafer with a thinned PR as shown in Fig. 2 (c) and etching partly the PR, only the n^+-doped poly-Si on Si_3N_4 spacer is exposed. Then, the exposed the n^+-doped poly-Si is etched to split the n^+-doped poly-Si. Then PR is removed, followed by the n^+-doped poly-Si patterning to form the gate as shown in Fig. 2 (d). After Si_3N_4 side-wall stripped, the buffer SiO_2 is grown on Si fins for ion implantations of source and drain (S/D). After, ion implantations of S/D are performed, followed by rapid thermal annealing at temperature of 1050 °C (5 sec) for S/D activation. Then, inter layer dielectric (ILD) is deposited, and contact holes are patterned. A metal pattern is formed.

3. Results and discussion

3.1. The characteristics of the double-gate MOSFET

Fig. 3(a) shows the measured I_D-V_{G1} curves of the double-gate MOSFET as a parameter of gate bias (V_{G2}). When the positive voltage is biased to the gate2 (G2), the threshold voltage (V_{th}) of the double-gate MOSFET decreases. By biasing the negative voltage to G2, V_{th} of the double-gate MOSFET increases. Fig. 3(b) shows the measured V_{th} changes of the double-gate MOSFET as the parameter of V_{G2} at I_D of 10nA. Since the channel region of the double-gate MOSFET is fully depleted, the V_{th} change of the double-gate MOSFET is linear with V_{G2} change.

3.2. Integrate-and-fire circuit using double-gate MOSFET for SNNs

Fig. 4 (a) and (b) shows a diagram of the integrate-and-fire neuron circuit with double-gate MOSFET and a homeostasis circuit, respectively. The neuron circuit is composed of the double-gate MOSFET, a p-type MOSFET, three n-type MOSFETs, two inverters (INV1 and INV2), and two capacitors (C_{mem} of 0.5 pF and C_{reset} of 0.05 pF). The homeostasis circuit is composed of a p-type MOSFET, two n-type MOSFETs, p-

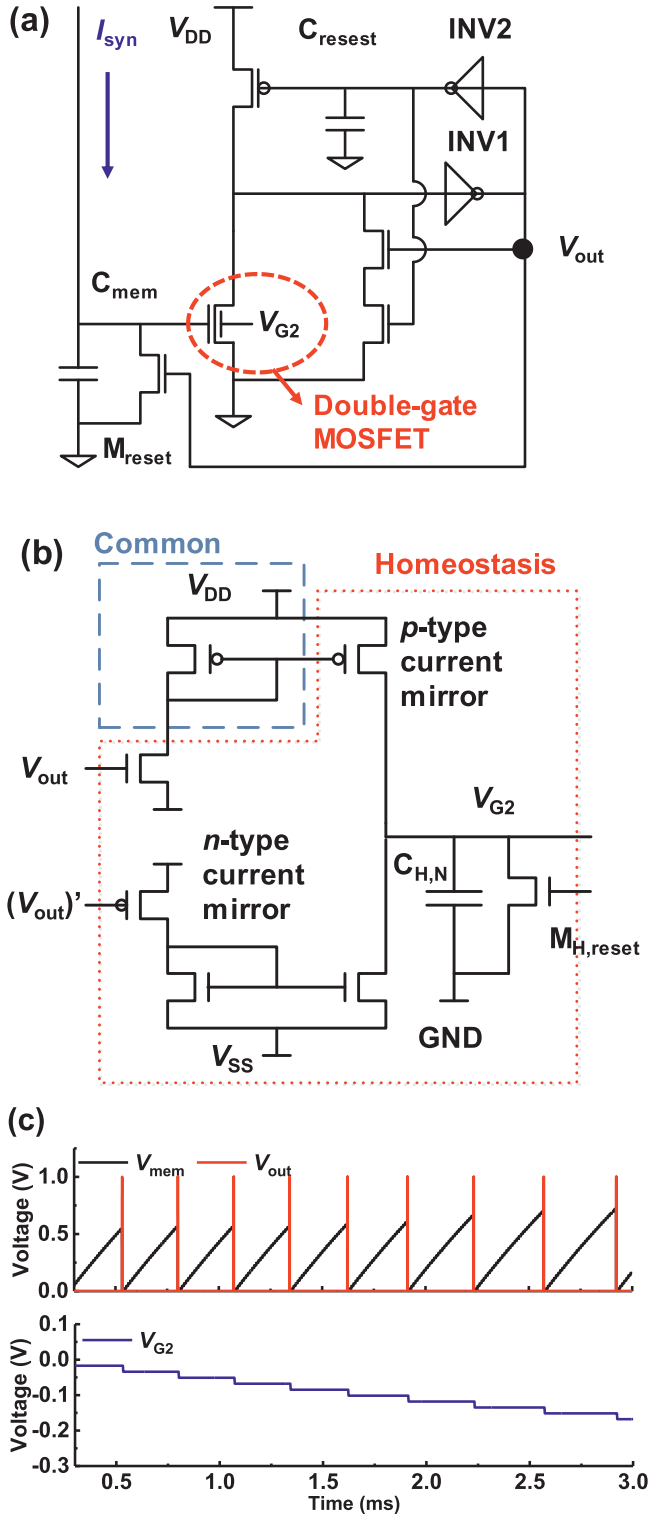


Fig. 4. (a) Diagram of the integrate-and-fire (IF) neuron circuit with double-gate MOSFET. (b) Diagram of the homeostasis circuit for controlling V_{G2} of the double-gate MOSFET. (c) The operation characteristics of the proposed IF neuron circuit.

(I_{input}:I_{ouput} = 10:1) and *n*-type current mirrors (I_{input}:I_{ouput} = 1:1), and a capacitor (C_H of 0.5 pF). The parameters of the *n*-, *p*-type MOSFETs, and supply voltage comprising the circuit are as follows: L = 0.5 μm, W = 0.1 μm, V_{DD} = 1.0 V, and V_{SS} = -1.0 V. In the neuron circuit, the C_{mem} is used to integrate signals transmitted from synaptic devices array. The double-gate MOSFET in the neuron circuit compares the membrane potential (V_{mem}) with V_{th} to trigger an output spike. When the V_{mem} is higher than the V_{th} of the double-gate MOSFET, the double-gate MOSFET turns on and the input node of INV1 goes from high to low state. Then, the output node (V_{out}) of INV1 become high state, and V_{mem} is back to the initial state by the M_{reset}. The output spike is transmitted to the next synaptic devices. The neuron circuit using the double-gate MSOFET biased by constant V_{G2} has a regular spike frequency at the same input signal without synaptic updates. If a homeostasis circuit is applied to each neuron (1 ~ N: the number of neurons) and the $C_{H,N}$ is connected to the G2 of the neuron circuit, the threshold of neuron circuit is determined by the amount of charges accumulated in the $C_{H,N}$. When the neuron circuit fires and transmits the output spike to the homeostasis circuit, the charges accumulated in the $C_{H,N}$ are discharged through the *n*-type current mirror. The potential of the $C_{H,N}$ becomes close to V_{SS} (-1V), and the threshold of neuron circuit increases as shown in Fig. 4 (c). Otherwise, the potential of the $C_{H,N}$ increases and the threshold of neuron circuit decreases when the other neurons fire since the *p*-type current mirror is connected to other neurons. These operations mimic the homeostasis functionality of the biological neuron with the self-controlled fire-frequency. When a neuron connected to the synaptic devices with large deviations is not fired, the neuron can have a chance to fire though the proposed homeostasis functionality. It can prevent the accuracy degradation in SNNs with large deviations.

Fig. 5(a) shows a block diagram of a multi-neurons system with the proposed homeostasis functionality for the SNN. Fig. 5(b) shows the IF operation and V_{G2} change of three neurons (Neurons 1, 2, and 3) with the homeostasis circuit. In a neural system based on winner-take-all (WTA) without homeostasis circuit, the neuron 2 can only perform the IF operation when the synaptic current to the neuron 2 is largest. When the homeostasis functionality is applied to the multi-neuron system, the threshold of the fired neuron 2 is increased by the output spike. On the other hand, the threshold of other neurons is decreased by the output spike of the fired neuron transmitted to *p*-type current mirror (I_{input}: I_{output} = 10:1) of the homeostasis circuit. Increasing the threshold of all neurons can slow down the learning and reasoning processes, even if the signals from the synaptic devices are sufficient. Therefore, it is necessary to lower the threshold voltage in a multi-neuron system.

3.3. The spiking neural network based on the proposed neuron circuits

To demonstrate the enhancement of classification accuracy and the immunity of the synaptic device variation in SNNs with the homeostasis functionality, the SNN based on a STDP learning rule is implemented using the proposed neuron circuit with homeostasis functionality. The number of neurons in each layer are 784 (input) and 200 (output). Each image of MNIST set is represented by 28 × 28 pixels, respectively. For training and evaluating the classification accuracy, 60,000 training and 10,000 test images of MNIST set are used. In previous work, LTP/LTD characteristics of the TFT-type synaptic devices and simplified STDP learning rule were proposed and investigated as shown in Fig. 6 (a), (b), and (c) [18,19]. The TFT-type synaptic device consists of intrinsic poly-Si as an active layer and n-doped poly-Si as a charge storage layer as shown in Fig. 6 (a). The amount of charges stored in the charge storage layer is modulated by the potential difference (V_{pre} - V_{post}) between pre- and post-signal. The synaptic weights for LTP/LTD characteristics are updated as shown in Fig. 6 (b) and (c). The TFT-type device is used as the synaptic devices to demonstrate the proposed SNN with the homeostasis functionality because it is compatible with conventional CMOS technology and has stable program/erase operation for LTP/LTD characteristics.

After 3 epochs of MNIST training, the simulated recognition rate (~91%) of the SNN with the proposed homeostasis functionality is higher than that (~79%) of the SNN without the proposed homeostasis functionality as shown in Fig. 6 (d). Because the fire frequencies of all neuron circuit are controlled by the homeostasis functionality during

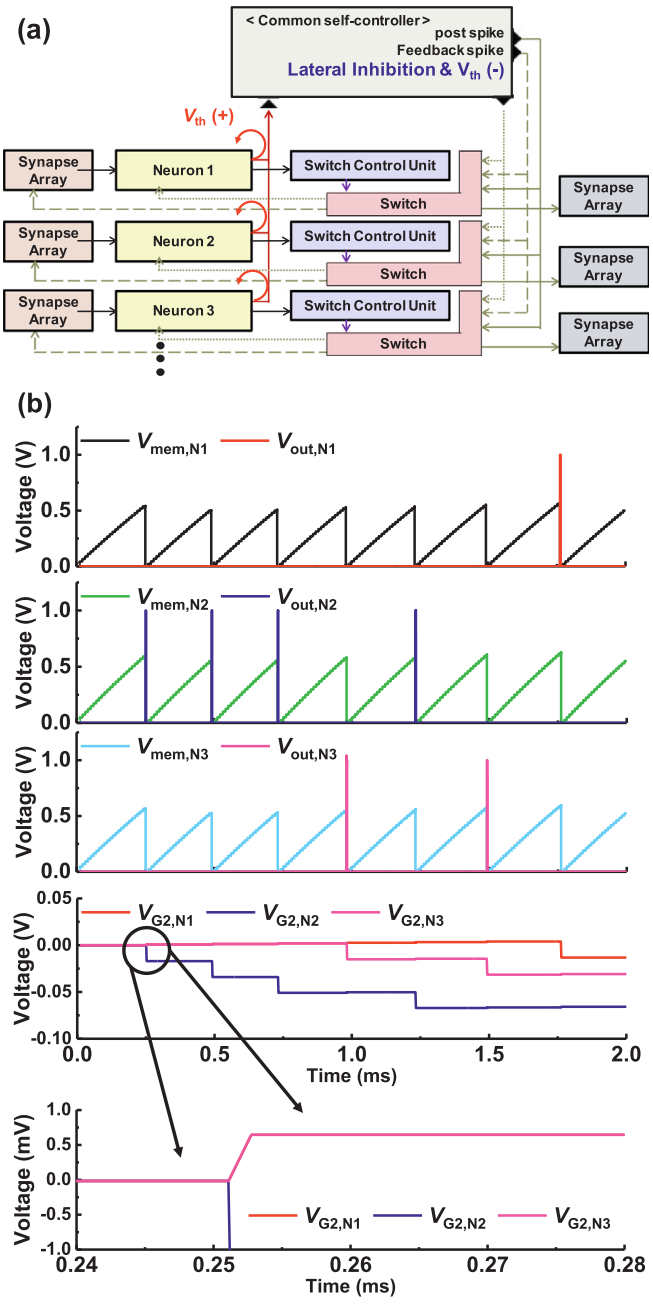


Fig. 5. (a) Spike neural network system based on the proposed neuron circuit to implement the homeostasis functionality. (b) The operation characteristics of the proposed multi-neurons.

learning process, all neuron circuits have a chance to fire and update the synaptic weights.

To implement a hardware-based SNN for the on-chip training, the variations of the synaptic devices and neuron circuits should be considered. Fig. 7(a) shows the device-to-device (D-to-D) and pulse-to-pulse (P-to-P) conductance variations of the synaptic devices to investigate the immunity of the synaptic device variations in SNNs based on the proposed homeostasis functionality.

If variations of the synaptic devices and neuron circuits are large ($\sigma/\mu > 0.3$) in the SNN without the homeostasis functionality, there are the neuron circuits with no chance to fire due to the low conductance of synaptic devices or the high thresholds of neuron circuits. However, although the variation of the synaptic devices and neuron circuits are very large ($0.3 < \sigma/\mu < 0.5$), the degradation of the recognition rate ($1 \sim 3\%$) is very low as shown in Fig. 7(b). Since the thresholds of

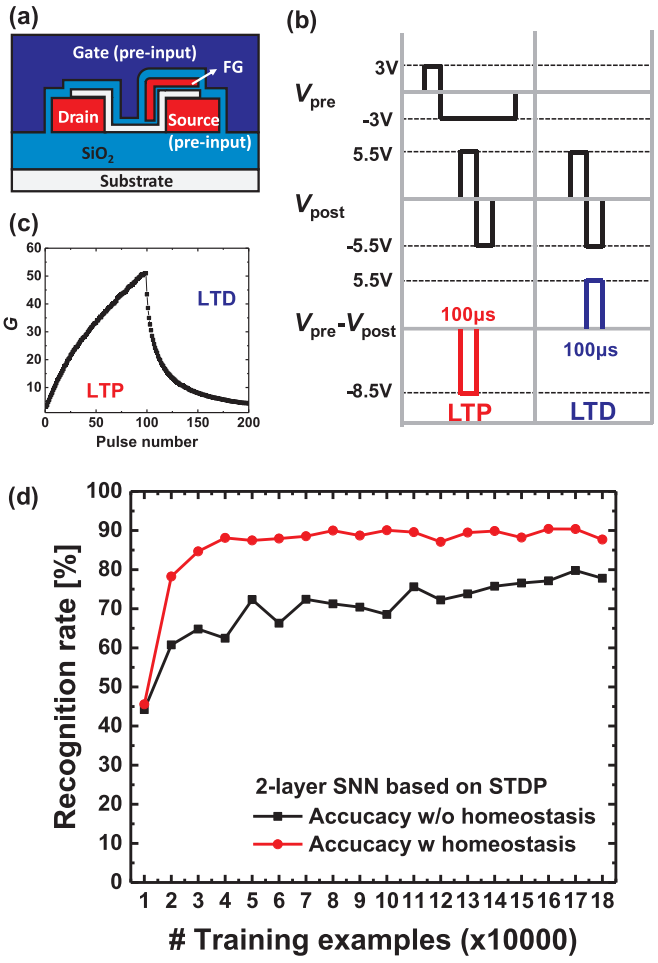


Fig. 6. (a) A schematic of TFT-type device as the synaptic device. (b) The operation scheme to update the synaptic weights. (c) LTP/LTD characteristics of the TFT-type [18,19]. (d) Classification accuracy as epochs of MNIST training sets in the HW-based neural network.

neuron circuits also are learned and changed during the synaptic weights updated, the homeostasis functionality can compensate the variation of synaptic devices and neuron circuits.

4. Conclusion

The double-gate MOSFET in the neuron circuit ~~was~~ has been proposed to implement the homeostasis functionality. The proposed transistor is compatible with the conventional CMOS technology. The DC characteristics of the double-gate MOSFET were investigated as parameter of the V_{G2}. The threshold of the neuron circuit using the double-gate MOSFET is controlled by the change of V_{G2}. The homeostasis functionality was implemented by controlling the thresholds of the neuron circuits in the multi-neurons system. The low degradation of the recognition rate ($1 \sim 3\%$) with the variation of the synaptic devices ($0.3 < \sigma/\mu < 0.5$) was confirmed through the simulation of the 2-layer SNN based on the proposed neuron circuit. It was demonstrated that the homeostasis functionality of the proposed neuron circuit can compensate the variations ($\sigma/\mu < 0.5$) of the synaptic devices and the neuron circuits in the SNN based on STDP. We believe that the idea we have proposed can be easily implemented using existing CMOS devices.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to

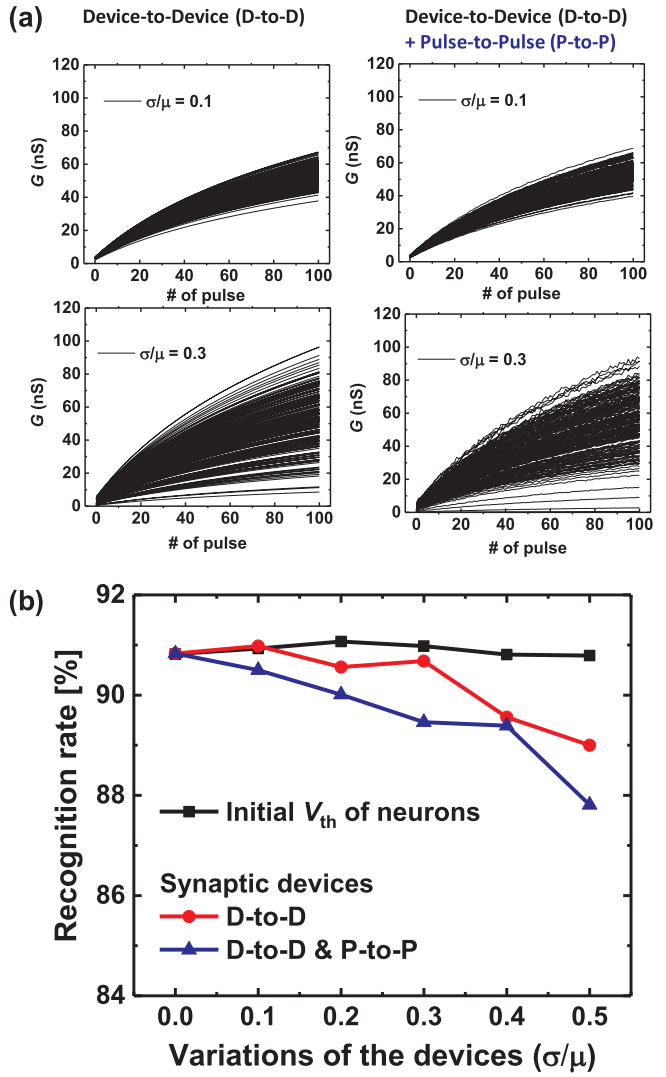


Fig. 7. (a) Device-to-device (D-to-D) and pulse-to-pulse (P-to-P) conductance variations (σ/μ) of the synaptic devices. (b) The degradation of the recognition rate with variations (σ/μ) of the synaptic devices and the initial Vth of neuron circuits.

influence the work reported in this paper.

Acknowledgment

This work was supported by Synopsys Inc., the Brain Korea 21 Plus Project in 2019, and National Research Foundation of Korea (NRF-2016M3A7B4909604).

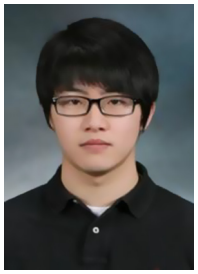
References and Notes

[1] Kuzum D, Yu S, Wong HP. Synaptic electronics: materials, devices and applications. Nanotechnology 2013;24:382001.
[2] Masquelier T, Thorpe SJ. Unsupervised learning of visual features through spike timing dependent plasticity. PLoS Comput Biol 2007;3(2):247–57.
[3] Basu A, Shuo S, Zhou H, Lim MH, Huang G-B. Silicon spiking neurons for hardware implementation of extreme learning machines. Neurocomputing 2013;102:125–34.
[4] Kasabov NK. NeuCube: A spiking neural network architecture for mapping, learning and understanding of spatio-temporal brain data. Neural Networks 2014;52:62–76.
[5] Wu X, Saxena V, Zhu K. Homogeneous Spiking Neuromorphic System for Real-World Pattern Recognition. IEEE J Emerging Sel Top Circuits Syst 2015;5(2):254–66.
[6] Poon C-S, Zhou K. Neuromorphic silicon neurons and large-scale neural networks: challenges and opportunities. Front Neurosci 2011;5:108.
[7] Qiao N, Mostafa H, Corradi F, Osswald M, Stefanini F, Sumislawska D, et al. A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128K synapses. Front Neurosci 2015;9:141.
[8] Indiveri G, Linares-Barranco B, Hamilton TJ, Schaik A, Etienne-Cummings R, Delbruck T, et al. Neuromorphic silicon neuron circuits. Front Neurosci 2011;5..
[9] Yu S, Gao B, Fang Z, Yu H, Kang J, Wong HP. A neuromorphic visual system using RRAM synaptic devices with Sub-pJ energy and tolerance to variability: Experimental characterization and large-scale modeling. IEEE International Electron Devices Meeting (IEDM) 2012.
[10] Prezioso M, Merrikh-Bayat F, Hoskins BD, Adam GC, Likharev KK, Strukov DB. Training and operation of an integrated neuromorphic network based on metal-oxide memristors. Nature 2015;521:61–4.
[11] Bichler O, Suri M, Querlioz D, Vuillaume D, DeSalvo B, Gamrat C. Visual Pattern Extraction Using Energy-Efficient "2-PCM Synapse" Neuromorphic Architecture. IEEE Trans. on Electron Devices 2012;59(8):2206–14.
[12] Querlioz D, Bichler O, Dollfus P, Gamrat C. Immunity to device variations in a spiking neural network with memristive nanodevices. IEEE Trans Nanotechnol 2013;12(3):288–95.
[13] Diehl PU, Cook M. Unsupervised learning of digit recognition using spike-timing-dependent plasticity. Front Comput Neurosci 2015;9.
[14] Bartolozzi C, Nikolayeva O, Indiveri G. Implementing homeostatic plasticity in VLSI networks of spiking neurons. 15th IEEE International Conference on Electronics, Circuits and Systems. 2008. p. 682–5.
[15] Bartolozzi C, Indiveri G. Global scaling of synaptic efficacy: Homeostasis in silicon synapses. Neurocomputing 2009;72:726–31.
[16] Rovere G, Ning Q, Bartolozzi C, Indiveri G. Ultra Low Leakage Synaptic Scaling Circuits for Implementing Homeostatic Plasticity in Neuromorphic Architectures. IEEE Trans Biomed Circuits Syst 2017;11(6):2073–6.
[17] Qiao N, Indiveri G, Bartolozzi C. Automatic gain control of ultra-low leakage synaptic scaling homeostatic plasticity circuits. IEEE Biomedical Circuits and Systems Conference (BioCAS) 2016;156-159.
[18] Kim C-H, Lee S, Woo SY, Kang W-M, Lim S, Bae J-H, et al. Demonstration of Unsupervised Learning With Spike-Timing-Dependent Plasticity Using a TFT-Type NOR Flash Memory Array. IEEE Trans Electron Devices 2018;65(5):1774–80.
[19] Lee S, Kim C-H, Oh S, Park B-G, Lee J-H. Unsupervised Online Learning With Multiple Postsynaptic Neurons Based on Spike-Timing-Dependent Plasticity Using a TFT-Type NOR Flash Memory Array. J Nanosci Nanotechnol 2019;19(10):6050–4.

Sung Yun Woo received the B.S. degree in electrical engineering from Kyungpook National University, in 2014. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Seoul National University (SNU), Seoul, Korea. He is with the Inter-University Semiconductor Research Center, SNU. His current research interests include neuromorphic system and neural networks.

Kyu-Bong Choi received the B.S. degree in electrical engineering from Seoul National University (SNU), Seoul, Korea, in 2012, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering. He is with the Inter-University Semiconductor Research Center, SNU. His current research interests include FinFET and its application in neural network computing.

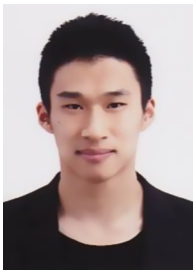
Jangsaeng Kim received the B.S. degree in electrical engineering from Seoul National University (SNU), Seoul, Korea, in 2018, where he is currently pursuing the M.S. degree with the Department of Electrical and Computer Engineering. He is with the Inter-University Semiconductor Research Center, SNU. His current research interests include neuromorphic system and its application in computing.



Won-Mook Kang received the B.S. degree in Electrical and Electronic Engineering from Yonsei University, Seoul, Korea, in 2014. He is currently pursuing the Ph. D. degree with the Department of Electrical and Computer Engineering, Seoul National University (SNU), Seoul, Korea. His research interests include neuromorphic system.

Chul-Heung Kim received the B.S. degree in electrical engineering from Seoul National University (SNU), Seoul, Korea, in 2013, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering. He is with the Inter-University Semiconductor Research Center, SNU. His current research interests include neuromorphic system and its application in computing.

Young-Tak Seo received the B.S. degree in electrical engineering from Seoul National University (SNU), Seoul, Korea, in 2016, where he is currently pursuing the Ph.D degree with the Department of Electrical and Computer Engineering. He is with the Inter-University Semiconductor Research Center, SNU. His current research interests include neuromorphic system and its application in computing.



Jong-Ho Bae received the B.S. degree in Electrical Engineering from Pohang University of Science and Technology (POSTECH), in 2011 and the Ph.D. degree in Electrical and Computer Engineering from Seoul National University (SNU), Seoul, Republic of Korea. He is currently with EECS, University of California, Berkeley. His current research interests include NCFET, FeFET, Sensor, and Neuromorphic Computing.

Byung-Gook Park (M'90) received the B.S. and M.S. degrees in electronics engineering from Seoul National University (SNU), Seoul, South Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 1990. He joined as an assistant professor with the Department of Electrical and Computer Engineering, SNU, in 1994, where he is currently a professor.

Jong-Ho Lee (SM'01-F'16) received the the Ph.D. degree from Seoul National University (SNU), Seoul, South Korea, in 1993, in electronic engineering. He was a Post-Doctoral Fellow with the Massachusetts Institute of Technology, Cambridge, MA, USA, from 1998 to 1999. He has been a professor with the School of Electrical and Computer Engineering, SNU, since 2009. He is a Lifetime Member of the Institute of Electronics Engineers of Korea (IEEK) and IEEE Fellow.