Macro modeling of ion sensitive field effect transistor with current drift

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Abstract

In terms of the application of the ion sensitive field effect transistor (ISFET) fabricated with top-down approached and CMOS-compatible back-end process to integrated circuits, the macro model of the ISFET is required. Although several models have been reported, there is no electrical model that reflects the time-dependent drain current (I d) change (drift effect). We propose the electrical model which can reflect the drift effect and can be expressed by the combination of electrical circuit components. In the proposed model, R1 represents the resistance of the electrolyte and the FET can be approximated by the capacitances C1 (capacitance of pure gate oxide in which hydrogen ions move very slowly) and C2 (capacitance by gate oxide with defects in which hydrogen ions move relatively faster). Furthermore, the movement of hydrogen ions in the defective oxide is represented by R2 and the current drift is modeled as the parallel combination of the C2 and the R2 because the drift effect is strongly related to hydrogen ion movement through defective gate oxide or Helmholtz layer. Consequently, the ISFET with the I d drift can be modeled by the series connection of the R1, the parallel combination of the C1 and the R2, and the C2. Also, the I d calculated by the proposed model is successfully fitted to the measured time-dependent I d of the ISFET.

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1. Introduction

As fabrication technology has continued to develop, various nano-size biomedical sensors have been widely researched since the size of biological entities, such as DNA, proteins, and viruses are similar to their size [1,2]. Especially, biomedical sensors using fluorescent labeling and parallel optical detection techniques have received much attention for high sensitivity [3]. However, they have a number of drawbacks such as expensive and time-consuming processes for sample preparation and data analysis. To overcome these limitations, silicon nanowire (SiNW) Ion Sensitive Field Effect Transistors (ISFET) have been proposed as one of the most promising biomedical sensors since it has good characteristics such as label-free, real-time detection, and excellent sensitivity caused by high surface-to-volume ratio [4].

In terms of the fabrication process, the early stage of SiNW biosensors had been studied through a bottom-up approach [5–8]. However, the bottom-up approach has serious disadvantages in the reproducibility of fabrication process and device design since it is difficult to control doping concentration and dimension parameters which affect the electrical performance of the device. Also, it is not suitable to be integrated with mature complementary metal-oxide semiconductor (CMOS) technology and circuitry because SiNWs fabricated by the bottom-up process cannot be well-aligned with electrodes. Meanwhile, a top-down approach can produce uniformly distributed and well-aligned NWs in predetermined orientation and position on substrate. Thus, many researchers have demonstrated CMOS-compatible biosensors by using top-down processed NWs [9–18]. Although the possibility of the integration with mature state-of-the-art CMOS technology and circuitry has been argued in the previous works on the top-down CMOS-compatible biosensors, the real integration of top-down approach SiNW biosensors with CMOS technology and circuit has been rarely reported. Furthermore, most previous works have adopted the lift-off process which is not compatible with the conventional CMOS back-end process. Thus, for assessing real advantages of SiNW-CMOS hybrid systems and expediting their wafer-scale mass-productions, the SiNW biosensors should be integrated with CMOS circuits by using the back-end process compatible with the conventional CMOS technology. Recently,
our group demonstrated a novel high-sensitive SiNW biosensor which was co-integrated with CMOS circuit by using top-down approached and CMOS-compatible back-end process simultaneously [19,20]. However, there are still challenges on the path to commercialization as chemical and biomedical sensors. Particularly, the current drift (change of drain current under a fixed bias as a function of measurement time) has been considered to be one of the critical obstacles because it is almost impossible to read precise current value within limited sensing time [21].

In the view point of the application of the co-integrated ISFET with CMOS circuit, the macro model of the ISFET including the current drift should be introduced to estimate the sensing performance of the ISFET-CMOS hybrid system as a function of time and to find a solution for the drift effect. A basic electrical model was demonstrated in [22] by considering only electrostatic state and thus the time dependence of sensing current (namely, current drift) cannot be expressed. The improved model considering the drift effect was reported in [23]. However, the drift model is based on a physical method. Therefore, in this study, we propose the electrical model which can explain the drift mechanism and can be expressed by the combination of electrical circuit components.

2. Experimental

To verify the proposed macro modeling including the drift effect, SiNW sensors were co-integrated with CMOS circuit by using top-down approached and CMOS-compatible back-end process. The detailed fabrication process is illustrated in Fig. 1(a). The proposed devices were fabricated on $4 \times 10^{15}$ cm$^{-2}$ boron-doped (100) silicon on insulator (SOI) wafer (top Si layer = 100 nm and buried oxide = 375 nm). Firstly, 1) The ion implantation was conducted on the Si layer thinned to 80 nm via thermal oxidation for channel doping, p-region (dopant: B$^+$, energy: 20 keV, dose: $5 \times 10^{13}$ cm$^{-2}$) and n-region (P$^+$ 40 keV 3 $\times 10^{13}$ cm$^{-2}$). Then, an annealing process was conducted at 950 $^\circ$C for 30 min for the uniform channel doping of the 80 nm thick silicon channel. 2) The active region was defined by mix-and-match process of e-beam and conventional photolithography on the silicon layer. 3) The silicon layer was dry-etched by HBr/O$_2$ inductively coupled plasma (ICP) for the active formation. 4) The 10 nm thick gate oxide was formed by dry-oxidation at 850 $^\circ$C. 5) The 100 nm thick poly-silicon was deposited at 630 $^\circ$C by low pressure CVD (LPCVD). The gate of the MOSFET was defined and the poly-silicon on the SiNW was removed by photolithography and ICP dry-etching. 6) By using photo resist (PR) mask which covers only the SiNW channel, the gate (G) of the MOSFET and source/drain (S/D) of both the SiNW and the MOSFET were doped by As$^+$ ion implantation for n-type S/D/G and BF$_2$$^+$ ion implantation for p-type S/D/G, respectively. A rapid thermal annealing (RTA) was implanted at 900 $^\circ$C for 10 seconds to activate the dopants. 7) Inter-layer dielectric oxide (ILD) was deposited by high density plasma CVD (HDP-CVD). 8) The contact holes were formed by photolithography and dry-etching. 9) The aluminum layer was formed on the ILD for metallization. 10) The tetraethyl orthosilicate layer was deposited for passivation. 11) The pads were opened by photolithography and dry-etching. 12) The oxide layer around the SiNW was removed by using a magnetically enhanced reactive ion etching technique in CHF$_3$/CF$_4$ plasma to define the sensing area. Finally, an alloying process was carried out. Fig. 1(b) shows the schematic of the fabricated SiNW sensor and the co-integrated MOSFET. Also, Fig. 1(c) shows the top-view SEM image of the fabricated SiNW sensor.

A polydimethylsiloxane (PDMS) fluidic channel was bonded on the fabricated chip for the fluidic transport of analyte solution as can be seen in Fig. 2(b) and (c). Then, the measurement system with tubing lines (inner diameter = 400 $\mu$m, outer diameter = 1.6 mm) on a probe station was setup as depicted in Fig. 2(d). The schematic diagram for the measurement setup using the PDMS fluidic channel is shown in Fig. 2(e). Here, the gate voltage ($V_{GC}$) of the SiNW sensor is applied to the liquid gate through the Ag/AgCl reference electrode (RE). The fabricated devices were functionalized using 3-aminopropyl-triethoxysilane (APTES) to obtain an amine (−NH$_2$) surface. 0.1 M potassium dihydrogen phosphate (KH$_2$PO$_4$) and potassium monohydrogen phosphate (K$_3$HPO$_4$) were used to control the buffer solutions with HCl and KOH.

3. Results and discussion

3.1. Mechanism of current drift

The fabricated SiNW sensor and MOSFET were characterized with a semiconductor parameter analyzer (4156C, Agilent) at room temperature. Fig. 3(a) and (b) show the drain current ($I_D$)−$V_{GC}$ curves of the n-type SiNW sensor and the $I_D$−gate voltage ($V_{GC}$) curves of the n-type/p-type MOSFETs, respectively. It is confirmed that the SiNW sensor is co-integrated successfully with the CMOS circuit by using top-down approached and CMOS-compatible back-end process.

Fig. 3(c) indicates the measured transfer characteristics of the SiNW sensor for different pH solutions. Through the measurements, the clear modulation of the $I_D$ with changing pH values is verified. Fig. 3(d) demonstrates that the threshold voltage shift ($\Delta V_{th}$) is obtained to be $\Delta V_{th} = -50 mV/pH$ for the n-type SiNW sensor, which confirms that the surface potential at the SiO$_2$/SiNW interface is well modulated by pH values. However, Fig. 4(b) and (c) show that the $I_D$ is increased (namely, $I_D$ drift) throughout the mea-
Fig. 2. (a) Fabricated PDMS channel master on 4-inch Si wafer. (b) Top view and (c) bird’s eye view of PDMS channel attached to fabricated chip. (d) Measurement setup with tube. (e) Schematic diagram of entire measurement system.

Fig. 3. Measured (a) drain current ($I_D$)-liquid gate voltage ($V_{LG}$) curves of n-type SiNW sensor and (b) $I_D$-gate voltage ($V_G$) curves of n-type/p-type MOSFETs, respectively. (c) Transfer characteristics of n-type SiNW sensor according to pH level. (d) Change of threshold voltage ($V_{th}$) by pH variation. All $V_{th}$s were extracted by constant current method at $1 \times 10^{-9}$ A.
measurement time \((T_M)\). The \(I_D\) increase rapidly in a few seconds at first (fast response). After that, the \(I_D\) increase slowly until \(-1700\) s (slow response). The biases of Fig. 4(a) were applied for the measurement of the \(I_D\) drift.

Considering 300 K was maintained during the entire measurement, the effect of temperature on the \(I_D\) drift can be ignored. To check if the RE potential drifts, two RES (main and auxiliary) were employed. A second (auxiliary) electrode was immersed inside the electrolyte of Fig. 2(e) with some distance from the reference electrode (main). The \(V_{LG}\) of Fig. 4(d) was applied to the main RE, and the electrolyte potential was measured through the auxiliary RE by high input impedance electrometer. Fig. 4(d) and (e) indicate that \(I_D\) still drifts although the potential of the electrolyte completely follows the bias voltage applied to the RE without any drift. Based on these results, it is clearly confirmed that the observed slow \(I_D\) drift should be attributed to the potential change at Helmholtz layer (HL) or the sensing oxide. The physical origin of the slow response can be explained by hydrogen ion \((H^+)\) injection into defective sensing oxide [21]. To clarify the correlation between the \(H^+\) injection and the \(I_D\) drift, the transient characteristics of \(I_D\) were measured at different \(V_{LG}\) and in various pH solutions. Fig. 4(b) demonstrates that \(I_D\) drifts more as the pH of the solution decreases (meaning that \(H^+\) concentration in the solution increases) at \(V_{LG}\) of 1 V. Also, as shown in Fig. 4(c), the \(I_D\) drift gets accelerated by the higher \(V_{LG}\) in pH 9 solution. These results strongly support that field enhanced \(H^+\) movement through the sensing insulator causes the \(I_D\) drift [24,25]. Furthermore, considering the diffusion constants of \(H^+\) \((D_{H+})\) in pure oxide and defective oxide, it can be simply noticed that the \(H^+\) movement mainly occurs in the defective oxide. The \(D_{H+}\) in pure oxide is much lower than that in oxide with defects \((D_{H+}^d)\) in defective oxide \(\approx 10^{-18}\) cm²/s, \(D_{H+}^d\) in pure oxide \(\approx 10^{-23}\) cm²/s). It means that \(H^+\) cannot move through the pure oxide (Diffusion length in pure oxide is 0.2 nm per a year), whereas \(H^+\) can be diffused in the defective oxide although the process is slow. Consequently, the \(I_D\) is continuously increased during the \(T_M\) because the penetration of \(H^+\) into the defective oxide is accelerated by \(V_{LG}\) and the injected \(H^+\) is diffused toward the channel of the n-type SiNW sensor as shown in Fig. 5(a). Additionally, Fig. 5(b) shows that the bi-layer of pure oxide and defective oxide can be formed in our fabricated SiNW sensor by the plasma damage during the sensing area open process of Fig. 1(a). As long as the sensing area is formed by a dry etching process, the formation of the defective oxide is inevitable. However, even if it is assumed that the defective oxide is not formed during the dry etching process, the interface of the sensing oxide become defective due to the chemical modification induced by the surface reaction between liquid gate and the sensing oxide [26,27].

### 3.2 Macro model of ISFET with current drift

To model the \(I_D\) drift induced by the \(H^+\) movement, we set up a simple circuit as shown in Fig. 6 where \(R_1\) represents the resistance of the electrolyte and the FET can be approximated as capacitances, \(C_1\) and \(C_2\). \(C_2\) is the capacitance by gate oxide with defects in which the hydrogen ions move relatively faster than those of pure oxide. \(C_1\) is the capacitance of the pure oxide in which the hydrogen ions move very slowly. \(R_2\) represents the ion movement through the defective oxide. The low diffusion constant in the oxide causes the bottleneck of the ion motion. The slow movement of hydrogen ions in the defective oxide is modeled as the parallel combination of the \(C_2\) and the large resistance \(R_2\). In the model, the \(V_{LG}\) is applied as a unit step function and the input loop is considered for the analysis of the response to the \(V_{LG}\).

According to Kirchhoff’s law, we can get the two equations, Eq. (1) and (2) about \(V_{LG}\) and current \((I)\) flowing from the liquid gate toward the gate oxide.

\[
V_{LG}(t) = R_1I + V_2 + \frac{1}{C_1} \int_0^t I dt \tag{1}
\]

\[
I = C_2 \frac{dV_2}{dt} + \frac{V_2}{R_2} \tag{2}
\]
where \( V_2 \) is the voltage across the defective oxide. As Eq. (2) is substituted into Eq. (1), the \( V_{LG} \) is expressed by the circuit components, \( C_1, C_2, R_1, R_2 \) and \( V_2 \). The expression is given by

\[
V_{LG}(t) = R_1 C_2 \frac{dV_2}{dt} + \frac{R_1}{R_2} V_2 + V_2 + \frac{C_2}{C_1} \int_{0}^{t} V_2 dt' \tag{3}
\]

By using Laplace transform for \( V_{LG}(t) = V_u(t) \), Eq. (3) is given by

\[
\frac{V}{s} = R_1 C_2 s V_2 + \frac{R_1}{R_2} V_2 + [C_1 + C_2] V_2 + \frac{1}{C_1 R_2} V_2 \tag{4}
\]

\[
C_1 R_2 V = [C_1 C_2 R_1 R_2^2 + (C_1 R_1 + C_2 R_2 + C_1 R_2 s + 1)] V_2 \tag{5}
\]

\[
V_2 = \frac{C_1 R_2}{C_1 C_2 R_1 R_2^2 + (C_1 R_1 + C_2 R_2 + C_1 R_2 s) + 1} V \tag{6}
\]

Furthermore, \( I \) can be expressed by Laplace transform of Eq. (2) as follows.

\[
I = (C_2 s + \frac{1}{R_2}) V_2 \tag{7}
\]

From the schematic model of Fig. 6, Laplace transformed Eq. (8) is obtained. As Eq. (6) and Eq. (7) are substituted into Eq. (8), the \( V_1 \) is expressed by Eq. (8.6) through the processes of Eqs. (8.3), (8.4), and (8.5).

\[
V_1 = \frac{V}{s} - R_1 I - V_2 = \frac{V}{s} - \left( C_2 R_1 s + \frac{R_1}{R_2} + 1 \right) V_2 \tag{8.1}
\]

\[
V = \frac{C_1 C_2 R_1 R_2 s + C_1 (R_1 + R_2)}{s + C_1 C_2 R_1 R_2 s + 1} V \tag{8.2}
\]

\[
V = \frac{C_1 (R_1 + R_2)}{(s + C_1 C_2 R_1 R_2 s + 1)} \tag{8.3}
\]

\[
V = \frac{V}{s} - \frac{1}{\alpha_1 - \alpha_2} \frac{(C_1 (R_1 + R_2))}{s - \alpha_1} V \tag{8.4}
\]

\[
\frac{C_1 (R_1 + R_2)}{C_1 C_2 R_1 R_2 s - \alpha_2} \tag{8.5}
\]

\[
V = \frac{1}{\alpha_1 - \alpha_2} \left[ C_1 (R_1 + R_2) \left( \frac{1}{s - \alpha_1} \right) \right] V \tag{8.6}
\]

By using inverse Laplace transform, Eq. (8.6) is given by

\[
V_1 = V_u(t) + \left[ \frac{1}{\alpha_1 - \alpha_2} \left( \frac{C_1 (R_1 + R_2)}{s - \alpha_1} \right) \right] e^{\alpha_1 t} \tag{9}
\]

Although \( a_1 \neq a_2 \) and \( a_1 a_2 \) are simply achievable from Eq. (8.3) as shown in Eq. (10), some approximation \((C_2 > C_1, R_2 > R_1, \text{and } a_2 > a_1)\) makes the solution much simpler.

\[
\alpha_1 + \alpha_2 = \frac{C_1 R_1 + C_2 R_2 + C_1 R_2}{C_1 C_2 R_1 R_2} \tag{10}
\]

\[
\alpha_1 + \alpha_2 = \frac{C_1 + C_2}{C_1 C_2 R_1 R_2} \alpha_1, \alpha_2 = \frac{1}{C_1 C_2 R_1 R_2} \tag{11}
\]

As the capacitance and resistance of drift term \((C_2, R_2)\) are much larger than that of rapid changing term \((C_1, R_1)\), \(a_1\) and \(a_2\) of Eq. (11) is obtained and the effective gate voltage of the gate node (\(V_G\) of Fig. 6) is expressed by Eq. (13) through Eq. (12).

\[
V_1 = V_u(t) + \frac{1}{\alpha_1 - \alpha_2} \left[ \frac{C_1 R_1 - C_2 R_2 e^{\alpha_1 t} - \frac{1}{C_1 C_2 R_1 R_2} e^{\alpha_2 t}}{\alpha_1 - \alpha_2} \right] V_u(t) \tag{12}
\]

\[
V_G = [1 - \frac{C_2}{C_1 + C_2} e^{-(C_1 + C_2)/(C_1 R_1)} - \frac{C_1 - C_2}{C_1 + C_2} e^{-(C_1 + C_2)/(C_1 R_2)}] V_u(t) \tag{13}
\]

The response of the \(V_G(t)\) to the step function input \(V_{LG} \) of \(t\), where \(u(t)\) is the unit step function \((u(t) = 1 \text{ for } t > 0 \text{ and } u(t) = 0 \text{ for } t < 0)\), is given as

\[
V_G(t) = [1 - A_1 e^{-\tau_1}, \tau_1] V_u(t) \tag{14}
\]

where \(A_1\) and \(\tau_1\) are constants determined by the circuit parameters \((R_1, R_2, C_1, \text{and } C_2)\). The exponentially decaying function with a long time constant \((\tau_1)\) is the cause of the current drift. As far as the slow drift of current is concerned, we can ignore the effect of the exponential function with the short time constant \((\tau_2)\) since it decays quickly. It will appear just like a part of the step function.

The physical meaning and notation of the parameters in Eq. (14) are summarized in tables of Fig. 7(a) and (b).

Although the drift effect is caused by the drift of the \(V_G\), it cannot be measured directly. Thus, the \(I_D\) calculated by the proposed model needs to be compared with the measured \(I_D\) to verify the validity of the proposed model. For the \(I_D\) calculation, the operation region of the SiNW sensor was first confirmed. Fig. 8(a) shows the output characteristics to find the operation region of the device. It is confirmed that the SiNW sensor is operated in saturation mode (\(V_G/V_0 = 1 \text{ V})\). In the saturation mode (\(V_G(t) - V_{th} < V_D\)), the \(I_D\) is given by

\[
I_D = \beta [V_G(t) - V_{th}]^2/2, \quad \text{for } V_G(t) - V_{th} > 0 \tag{15}
\]

where \(\beta\) and \(V_{th}\) represent the gain factor and threshold voltage of the FET, respectively. Fig. 8(b) shows that the \(I_D\)–\(V_G\) characteristic was measured with a long integration time of 15 s at each step to extract the saturated \(I_D\) (meaning the drift-free \(I_D\) because the \(I_D\) is measured after the \(I_D\) drift is finished) as a function of the \(V_G\).

By substituting the extracted relationship between the drift-free \(I_D\)

\[
\text{\footnotesize \(D_m(H^+): \sim 10^{-23} \text{ cm}^2/\text{s at 300K (pure oxide)}\)}
\]

\[
\text{\footnotesize \(D_m(H^+): \sim 10^{-18} \text{ cm}^2/\text{s at 300K (defective oxide)}\)}
\]

* \(R_2 \gg R_1\)
and the $V_{LC}$ into Eq. (15), we can obtain the constant $\beta = 32 \mu A/V^2$ as shown in Fig. 8(b).

The Eq. (16) demonstrates that the $V_C$ of Eq. (14) can be converted to the $I_D$ by substituting Eq. (14) into Eq. (15) with the calibrated $\beta$.

$$I_D = \beta [\{1 - A_1 e^{-t/\tau_1} - A_2 e^{-t/\tau_2}\} - V_{LB}(t)] = V_{LB}^2/2, \quad \text{for } V_C(t) - V_{LB} > 0$$

Moreover, $A_1$, $A_2$, $\tau_1$, and $\tau_2$ in Eq. (16) were determined by the optimized process. The $I_D$ with the drift is analyzed by fitting it using Eqs. (15) and (17), which models the increased current as the sum of pure single exponential terms [28]:

$$V_C(t) = [1 - \sum_{n=1}^N A_n \exp(-t/\tau_n)] V_{LC} u(t)$$

Each single exponential term means the change in the $I_D$ influenced by the $I_D$ drift with the time constant $\tau_n$. The fitting is performed to minimize the sum of $|\text{measured } I_D - \text{calculated } I_D|^2$ at the measured points. In this process, $A_n$’s are the fitting parameters to be evaluated, whereas $\tau_n$’s are the predefined constants. A total of 85 single exponential terms with time constants $\tau_n$, which are equally spaced logarithmically in time, are used for fitting the experimental result. Fig. 9 shows the extracted time-constant spectrum where 3 s and 300 s can be determined as $\tau_S$ and $\tau_L$, respectively. Also, the relation of $C_2 = 55C_1$ can be extracted from the amplitudes of the selected $\tau_S$ and $\tau_L$.

Consequently, Fig. 10 reveals that the proposed model consisting of only electrical circuit components reflects the drift effect related to the $H^+$ movement by using the calibrated parameters such as $\beta = 32 \mu A/V^2$, $C_2 = 55C_1$, $\tau_S = 3$ s, and $\tau_L = 300$ s.

4. Conclusions

In this study, the SiNW sensor was co-integrated with the CMOS circuit by using top-down approach and CMOS-compatible back-end process. To investigate the physical origin of the $I_D$ drift, the transient $I_D$ characteristics of the fabricated SiNW sensor were monitored with various $V_{LC}$ and pH values. It is revealed that the field-enhanced $H^+$ penetration through the defective sensing insulator causes the $I_D$ drift. For the application of the SiNW sensor to integrated circuits, we propose the electrical model which can reflect the drift effect and can be expressed only by the combination of electrical circuit components. In the proposed model, $R_2$ represents the resistance of the electrolyte and the FET can be approximated by the capacitances $C_1$ (capacitance of pure gate oxide in which hydrogen ions move very slowly) and $C_2$ (capacitance by gate oxide with defects in which hydrogen ions move relatively faster). Furthermore, the movement of $H^+$ in the defective oxide is represented by $R_3$ and the current drift is modeled as the parallel combination of the $C_2$ and the $R_3$ because the drift effect is strongly related to the $H^+$ movement through the defective gate oxide. Consequently, the SiNW sensor with the $I_D$ drift can be modeled by the series connection of the $R_1$, the parallel combination of the $C_2$ and the $R_2$, and the $C_1$. The calculated $I_D$ by the proposed model is successfully fitted to the measured time-dependent $I_D$ of the SiNW sensor.
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References


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